

# 2SK3461(L), 2SK3461(S)

Silicon N Channel MOS FET  
High Speed Power Switching

# HITACHI

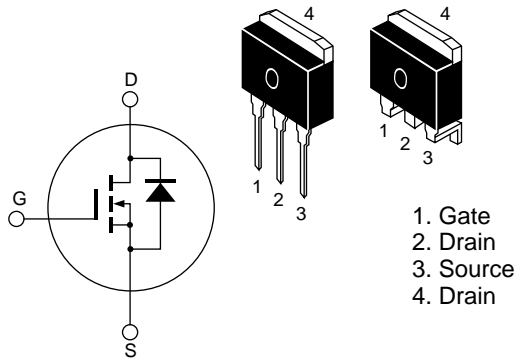
ADE-208-944 (Z)  
1st. Edition  
Mar. 2001

## Features

- Low on-resistance  
 $R_{DS(on)} = 4.3 \text{ m}$  typ.
- 4 V gate drive device
- High speed switching

## Outline

LDDPAK



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## 2SK3461(L), 2SK3461(S)

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### Absolute Maximum Ratings (Ta = 25°C)

Item	Symbol	Value	Unit
Drain to source voltage	$V_{DSS}$	60	V
Gate to source voltage	$V_{GSS}$	±20	V
Drain current	$I_D$	85	A
Drain peak current	$I_{D (pulse)}$ <sup>Note 1</sup>	340	A
Body-drain diode reverse drain current	$I_{DR}$	85	A
Avalanche current	$I_{AP}$ <sup>Note 3</sup>	60	A
Avalanche energy	$E_{AR}$ <sup>Note 3</sup>	308	mJ
Channel dissipation	$P_{ch}$ <sup>Note 2</sup>	110	W
Channel temperature	Tch	150	°C
Storage temperature	Tstg	-55 to +150	°C

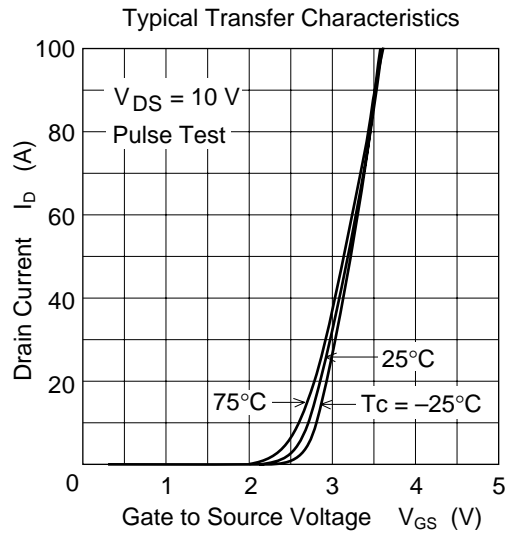
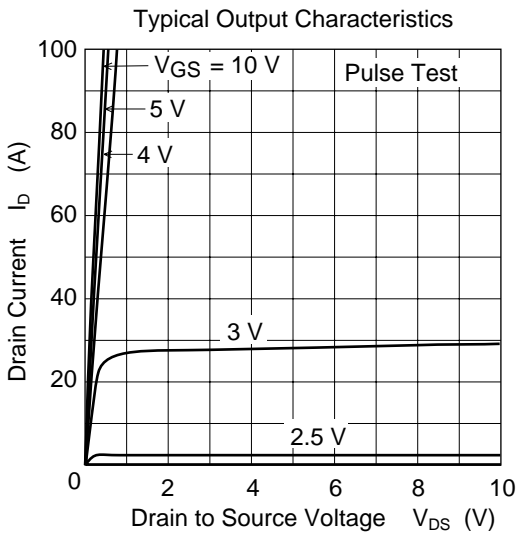
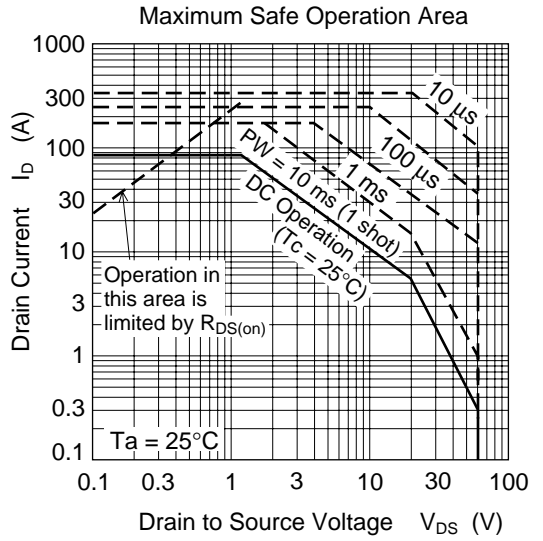
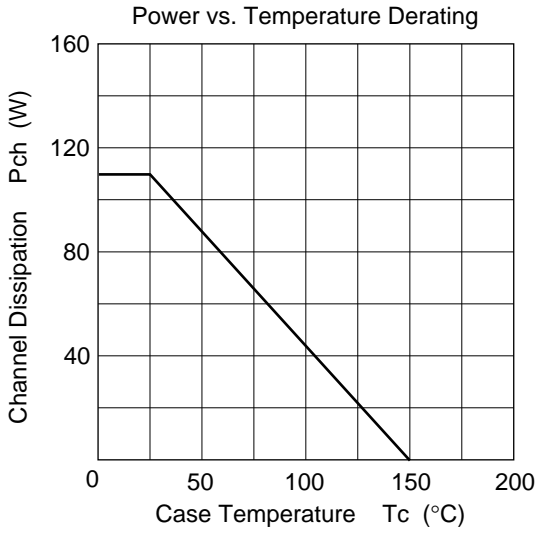
- Notes: 1.  $PW \leq 10 \mu s$ , duty cycle  $\leq 1\%$   
2. Value at  $T_c = 25^\circ C$   
3. Value at  $T_{ch} = 25^\circ C$ :  $R_g \geq 50 \Omega$

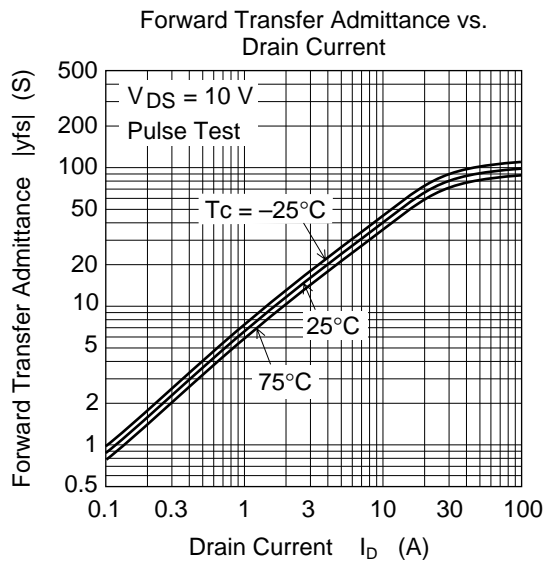
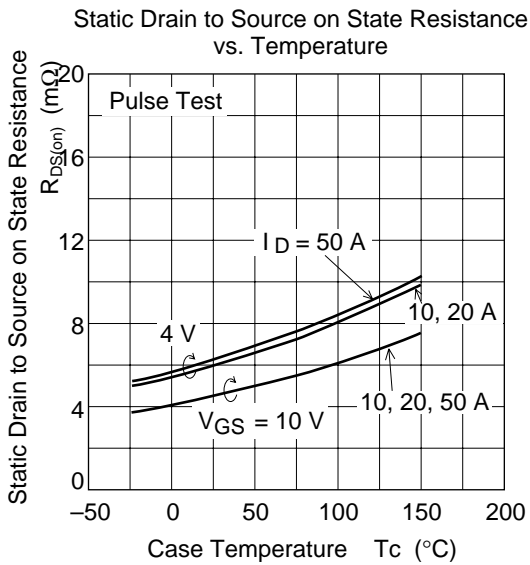
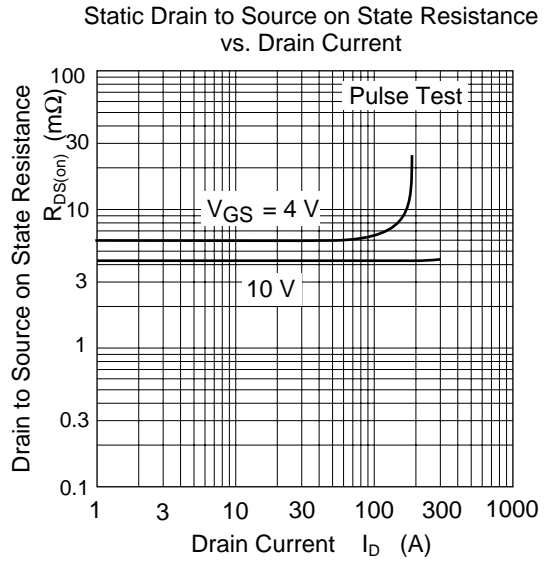
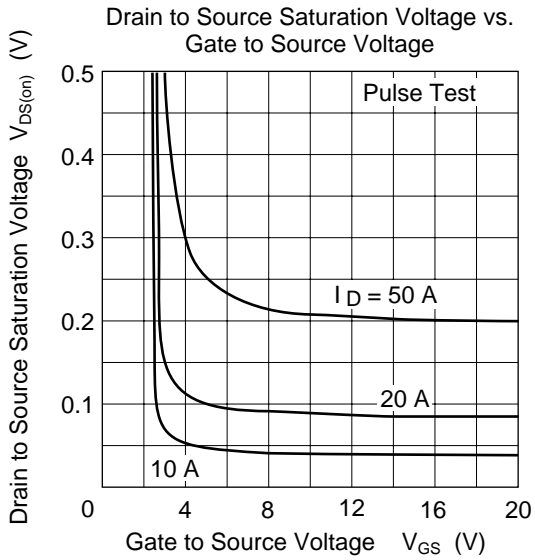
**Electrical Characteristics (Ta = 25°C)**

Item	Symbol	Min	Typ	Max	Unit	Test conditions
Drain to source breakdown voltage	$V_{(BR)DSS}$	60	—	—	V	$I_D = 10 \text{ mA}, V_{GS} = 0$
Gate to source leak current	$I_{DSS}$	—	—	10	$\mu\text{A}$	$V_{DS} = 60 \text{ V}, V_{GS} = 0$
Zero gate voltage drain current	$I_{GSS}$	—	—	$\pm 0.1$	$\mu\text{A}$	$V_{GS} = \pm 20 \text{ V}, V_{DS} = 0$
Gate to source cutoff voltage	$V_{GS(off)}$	1.0	—	2.5	V	$V_{DS} = 10 \text{ V}, I_D = 1 \text{ mA}$ <sup>Note 1</sup>
Forward transfer admittance	$ y_{fs} $	55	90	—	S	$I_D = 45 \text{ A}, V_{DS} = 10 \text{ V}$ <sup>Note 1</sup>
Static drain to source on state resistance	$R_{DS(on)}$	—	4.3	5.5	$\text{m}\Omega$	$I_D = 45 \text{ A}, V_{GS} = 10 \text{ V}$ <sup>Note 1</sup>
	$R_{DS(on)}$	—	6.0	9.0	$\text{m}\Omega$	$I_D = 45 \text{ A}, V_{GS} = 4 \text{ V}$ <sup>Note 1</sup>
Input capacitance	$C_{iss}$	—	9770	—	$\text{pF}$	$V_{DS} = 10 \text{ V}$
Output capacitance	$C_{oss}$	—	1340	—	$\text{pF}$	$V_{GS} = 0$
Reverse transfer capacitance	$C_{rss}$	—	470	—	$\text{pF}$	$f = 1 \text{ MHz}$
Total gate charge	$Q_g$	—	180	—	nc	$V_{DD} = 50 \text{ V}$
Gate to source charge	$Q_{gs}$	—	32	—	nc	$V_{GS} = 10 \text{ V}$
Gate to drain charge	$Q_{gd}$	—	36	—	nc	$I_D = 85 \text{ A}$
Turn-on delay time	$t_{d(on)}$	—	53	—	ns	$V_{GS} = 10 \text{ V}$
Rise time	$t_r$	—	320	—	ns	$I_D = 45 \text{ A}$
Turn-off delay time	$t_{d(off)}$	—	700	—	ns	$R_L = 0.67 \Omega$
Fall time	$t_f$	—	380	—	ns	
Body-drain diode forward voltage	$V_{DF}$	—	1.0	—	V	$I_F = 85 \text{ A}, V_{GS} = 0$
Body-drain diode reverse recovery time	$t_{rr}$	—	70	—	ns	$I_F = 85 \text{ A}, V_{GS} = 0$ $diF/dt = 50 \text{ A}/\mu\text{s}$

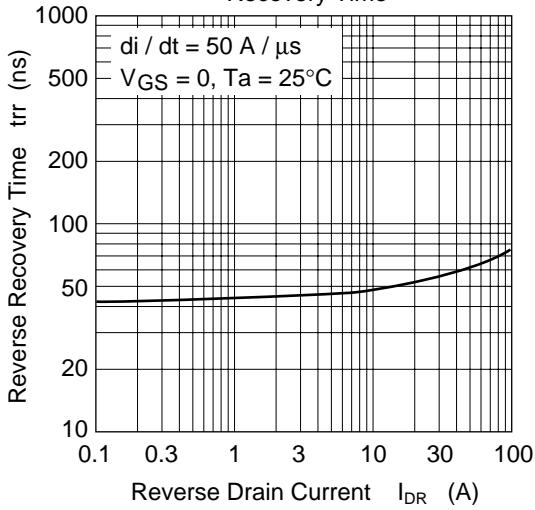
Note: 1. Pulse test

## Main Characteristics

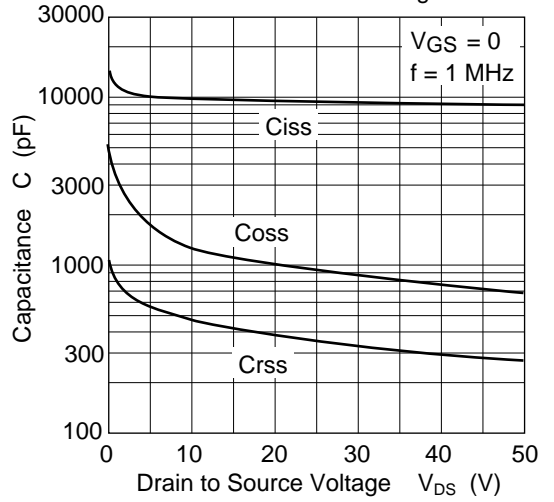




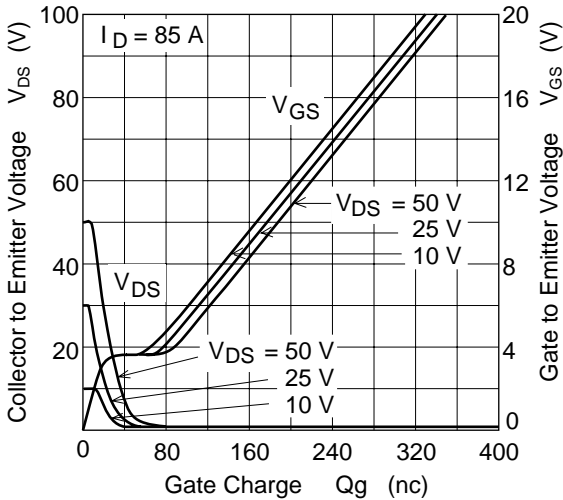
Body-Drain Diode Reverse Recovery Time



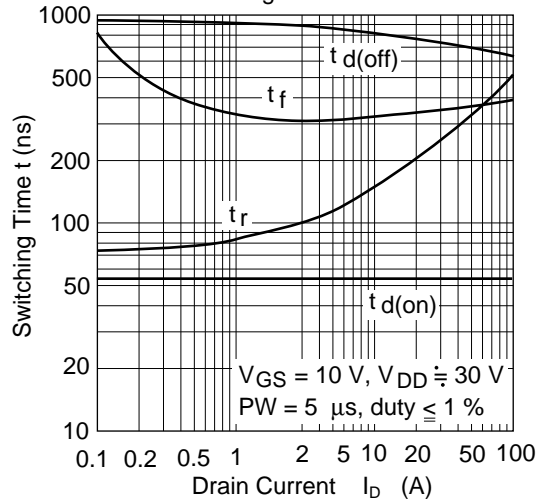
Typical Capacitance vs. Drain to Source Voltage

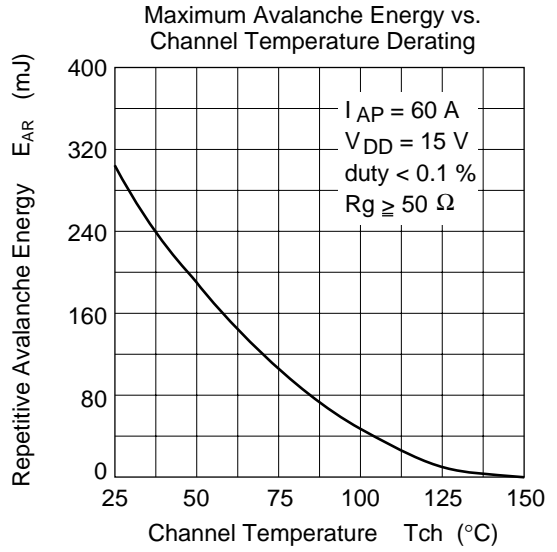
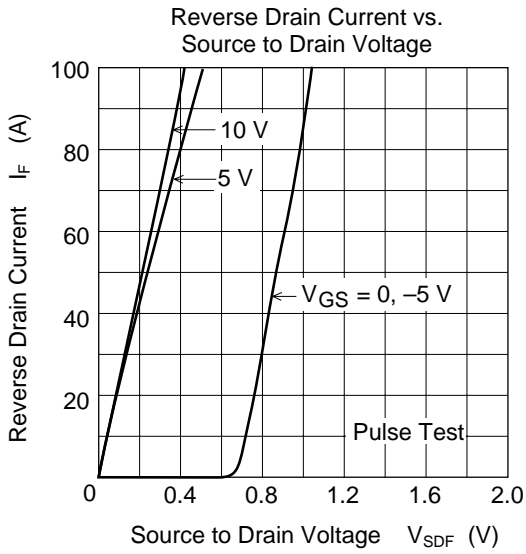


Dynamic Input Characteristics

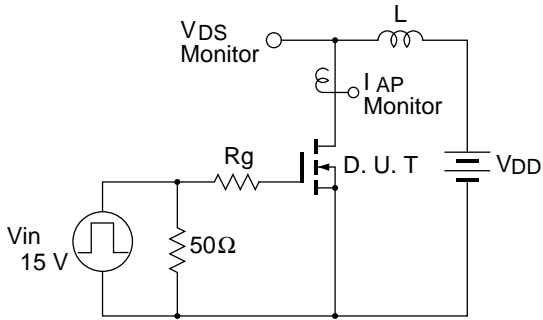


Switching Characteristics



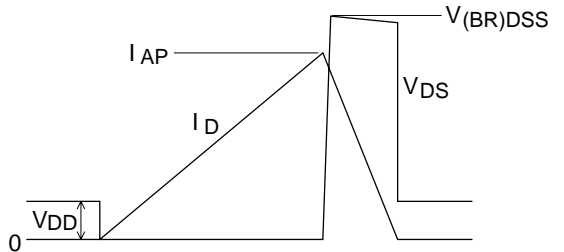


Avalanche Test Circuit

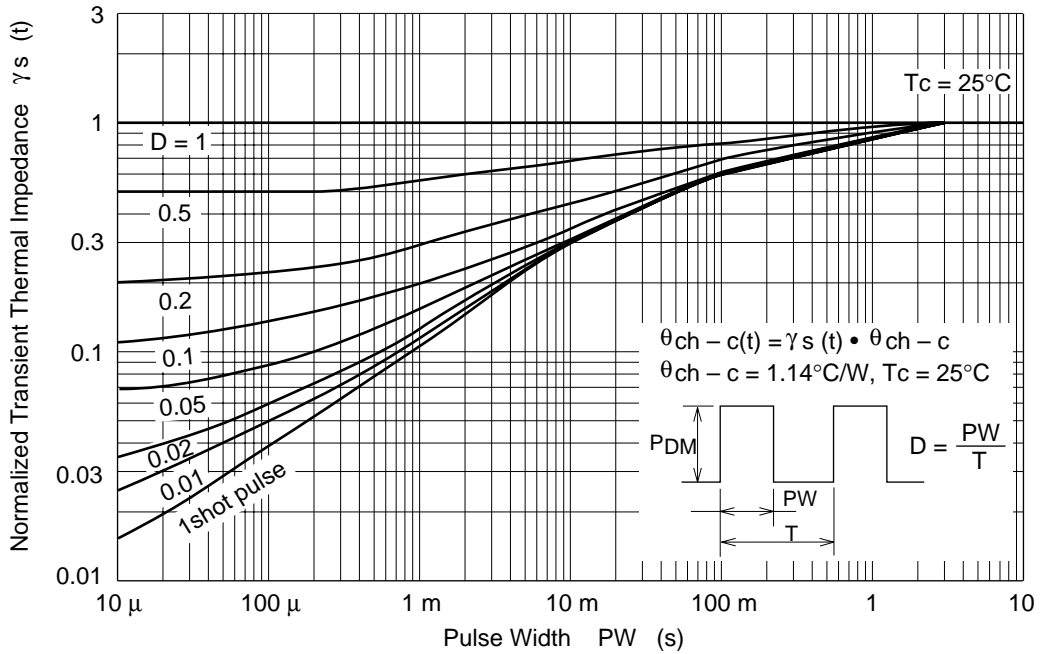


Avalanche Waveform

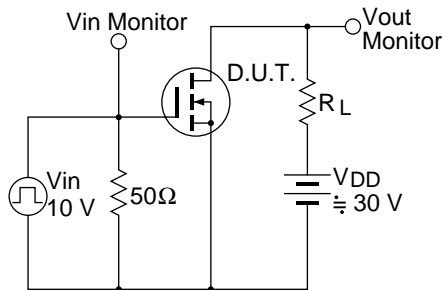
$$E_{AR} = \frac{1}{2} \cdot L \cdot I_{AP}^2 \cdot \frac{V_{DSS}}{V_{DSS} - V_{DD}}$$



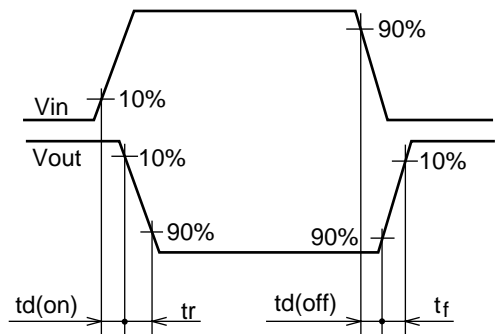
Normalized Transient Thermal Impedance vs. Pulse Width



Switching Time Test Circuit



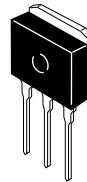
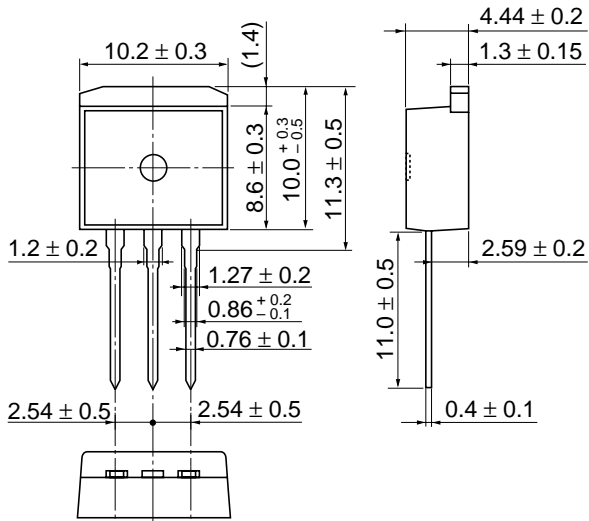
Waveform





Package Dimensions

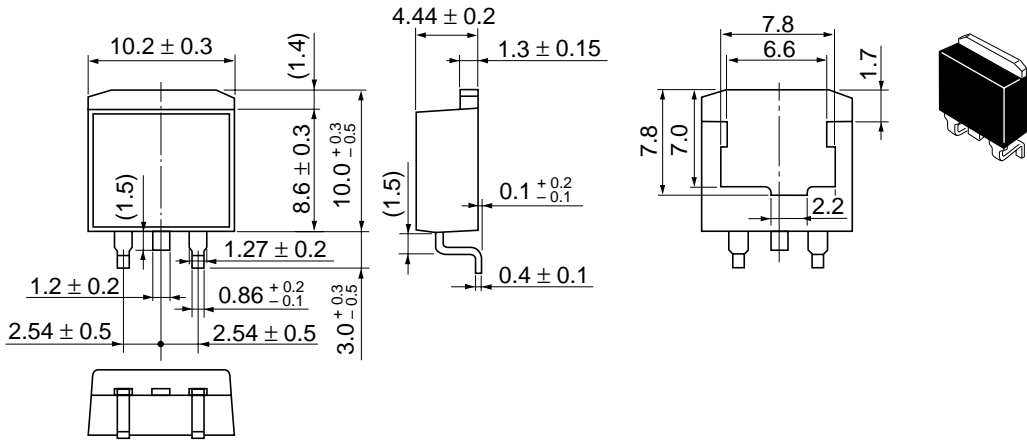
As of January, 2001  
Unit: mm



Hitachi Code	LDPAK (L)
JEDEC	—
EIAJ	—
Mass (reference value)	1.4 g

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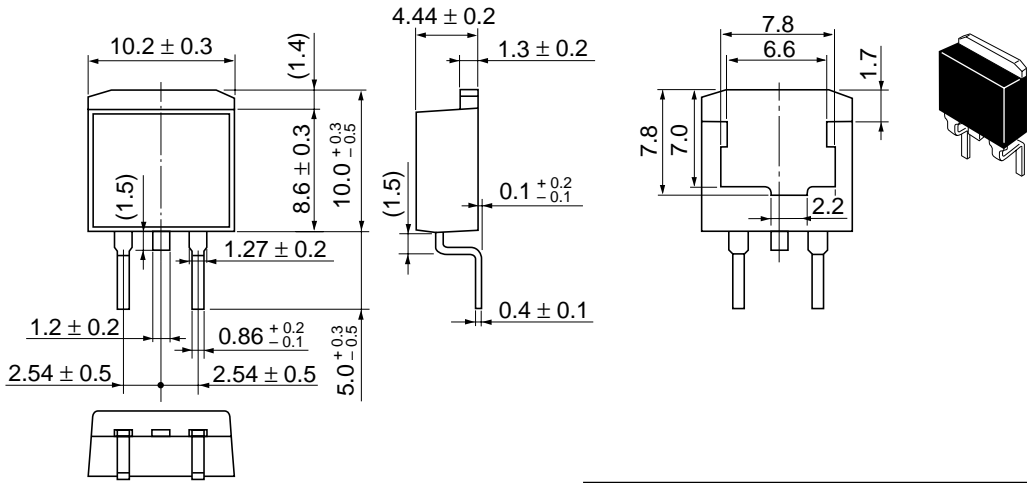
As of January, 2001  
Unit: mm



Hitachi Code	LDBAK (S)-(1)
JEDEC	—
EIAJ	—
Mass (reference value)	1.3 g

# 2SK3461(L), 2SK3461(S)

As of January, 2001  
Unit: mm



Hitachi Code	LDBAK (S)-(2)
JEDEC	—
EIAJ	—
Mass (reference value)	1.35 g

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