LED Drivers for LCD Backlights

# White Backlight LED Driver for Medium to Large LCD Panels (Switching Regulator Type)

Pb Free
ROHM Electronic Components

RoHS
Directive Compliance

### BD8119FM-M

No.10040EAT17

## ●Description

BD8119FM-M is a white LED driver with the capability of withstanding high input voltage (36V MAX).

This driver has 4ch constant-current drivers integrated in 1-chip, which each channel can draw up to 150mA max, so that high brightness LED driving can be realized.

Furthermore, a current-mode buck-boost DC/DC controller is also integrated to achieve stable operation against unstable car-battery voltage input and also to remove the constraint of the number of LEDs in series connection.

The brightness can be controlled by either PWM or VDAC techniques.

## ●Features

1) Input voltage range is 5.0 to 30 V
2) Integrated buck-boost current-mode DC/DC controller
3) Four integrated LED current driver channels (150mA max. each channel)
4) PWM Light Modulation (Minimum Pulse Width 25μs)
5) Built-in protection functions (UVLO, OVP, TSD, OCP, SCP)
6) Abnormal status detection function (OPEN/ SHORT)
7) HSOP-M28 package

## ●Applications

Backlight for car navigation, dashboard panels, etc.

(※ Recommended Component of Toshiba Matsushita Display Technology Co.,Ltd. )

## ●Absolute maximum ratings (Ta=25℃)

| Parameter | Symbol | Ratings | Unit |
|---|---|---|---|
| Power supply voltage | $V_{CC}$ | 36 | V |
| BOOT Voltage | $V_{BOOT}$ | 41 | V |
| SW,CS,OUTH Voltage | $V_{SW}$, $V_{CS}$, $V_{OUTH}$ | 36 | V |
| BOOT-SW Voltage | $V_{BOOT-SW}$ | 7 | V |
| LED output voltage | $V_{LED1\sim4}$ | 36 | V |
| VREG, OVP, OUTL, FAIL1, FAIL2, LEDEN1, LEDEN2, ISET, VDAC, PWM, SS, COMP, RT, SYNC, EN Voltage | $V_{VREG}$, $V_{OVP}$, $V_{OUTL}$, $V_{FAIL1}$, $V_{FAIL2}$, $V_{LEDEN1}$, $V_{LEDEN2}$, $V_{ISET}$, $V_{VDAC}$, $V_{PWM}$, $V_{SS}$, $V_{COMP}$, $V_{RT}$, $V_{SYNC}$, $V_{EN}$ | $-0.3\sim7 < V_{CC}$ | V |
| Power Consumption | Pd | 2.20 ※1 | W |
| Operating temperature range | Topr | $-40\sim+95$ | ℃ |
| Storage temperature range | Tstg | $-55\sim+150$ | ℃ |
| LED maximum output current | $I_{LED}$ | 150 ※2 ※3 | mA |

※1  IC mounted on glass epoxy board measuring 70mm×70mm×1.6mm, power dissipated at a rate of 17.6mw/℃ at temperatures above 25℃.
※2  Dispersion figures for LED maximum output current and $V_F$ are correlated. Please refer to data on separate sheet.
※3  Amount of current per channel.

## ●Operating conditions (Ta=25℃)

| Parameter | Symbol | Ratings | Unit |
|---|---|---|---|
| Power supply voltage | $V_{CC}$ | $5.0\sim30$ | V |
| Oscillating frequency range | $F_{OSC}$ | $250\sim550$ | kHz |
| External synchronization frequency range ※4 ※5 | $F_{SYNC}$ | $fosc\sim550$ | kHz |
| External synchronization pulse duty range | $F_{SDUTY}$ | $40\sim60$ | % |

※4  Connect SYNC to GND or OPEN when not using external frequency synchronization.
※5  Do not switch between internal and external synchronization when an external synchronization signal is input to the device.

2010.09 - Rev.A

●Electrical Characteristics (unless otherwise specified, $V_{CC}$=12V Ta=25°C)

| Parameter | Symbol | Limits | | | Unit | Conditions |
|---|---|---|---|---|---|---|
| | | Min | Typ | Max. | | |
| Circuit current | $I_{CC}$ | - | 7 | 14 | mA | EN=Hi, SYNC=Hi, RT=OPEN PWM=Low, ISET=OPEN, $C_{IN}$=10µF |
| Standby current | $I_{ST}$ | - | 4 | 8 | µA | EN=Low |
| **[VREG Block (VREG)]** | | | | | | |
| Reference voltage | $V_{REG}$ | 4.5 | 5 | 5.5 | V | $I_{REG}$=-5mA, $C_{REG}$=2.2µF |
| **[OUTH Block]** | | | | | | |
| OUTH high-side ON resistance | $R_{ONHH}$ | 1.0 | 3 | 4.5 | Ω | $I_{ON}$=-10mA |
| OUTH low-side ON resistance | $R_{ONHL}$ | 0.5 | 2 | 3.0 | Ω | $I_{ON}$=10mA |
| Over-current protection operating voltage | $V_{OLIMIT}$ | $V_{CC}$ -0.66 | $V_{CC}$ -0.6 | $V_{CC}$ -0.54 | V | |
| **[OUTL Block]** | | | | | | |
| OUTH high-side ON resistance | $R_{ONLH}$ | 1.0 | 3 | 4.5 | Ω | $I_{ON}$=-10mA |
| OUTH low -side ON resistance | $R_{ONLL}$ | 0.5 | 2 | 3.0 | Ω | $I_{ON}$=10mA |
| **[SW Block]** | | | | | | |
| SW low -side ON resistance | $R_{ON\_SW}$ | 1.0 | 2.0 | 4.0 | Ω | $I_{ON\_SW}$=10mA |
| **[Error Amplifie Block]** | | | | | | |
| LED    voltage | $V_{LED}$ | 0.9 | 1.0 | 1.1 | V | |
| COMP sink current | $I_{COMPSINK}$ | 15 | 25 | 35 | µA | $V_{LED}$=2V, Vcomp=1V |
| COMP source current | $I_{COMPSOURCE}$ | -35 | -25 | -15 | µA | $V_{LED}$=0V, Vcomp=1V |
| **[Oscillator Block]** | | | | | | |
| Oscillating frequency | $f_{OSC}$ | 250 | 300 | 350 | KHz | $R_T$=100kΩ |
| **[OVP Block]** | | | | | | |
| Over-voltage detection reference voltage | $V_{OVP}$ | 1.9 | 2.0 | 2.1 | V | $V_{OVP}$=Sweep up |
| OVP hysteresis width | $V_{OHYS}$ | 0.45 | 0.55 | 0.65 | V | $V_{OVP}$=Sweep down |
| SCP Latch OFF Delay Time | $T_{SCP}$ | 70 | 100 | 130 | ms | $R_T$=100kΩ |
| **[UVLO Block ]** | | | | | | |
| UVLO voltage | $V_{UVLO}$ | 4.0 | 4.3 | 4.6 | V | $V_{CC}$ : Sweep down |
| UVLO hysteresis width | $V_{UHYS}$ | 50 | 150 | 150 | mV | $V_{CC}$ : Sweep up |

◎ This product is not designed for use in radioactive environments.

●**Electrical Characteristics – Continued** (unless otherwise specified, VCC=12V Ta=25°C)

| Parameter | Symbol | Limits | | | Unit | Conditions |
|---|---|---|---|---|---|---|
| | | Min | Typ | Max. | | |
| **[LED Output Block]** | | | | | | |
| LED current relative dispersion width | $\triangle I_{LED1}$ | -3 | - | +3 | % | $I_{LED}$=50mA, $\triangle I_{LED1}$=($I_{LED}I_{LED\_AVG}$-1)×100 |
| LED current absolute dispersion width | $\triangle I_{LED2}$ | -5 | - | +5 | % | $I_{LED}$=50mA, $\triangle I_{LED2}$=($I_{LED}$50mA-1)×100 |
| ISET voltage | $V_{ISET}$ | 1.96 | 2.0 | 2.04 | V | RISET 1=120kΩ |
| PWM minimum pulse width | Tmin | 25 | - | - | µs | $F_{PWM}$=150Hz, $I_{LED}$=50mA |
| PWM maximum duty | Dmax | - | - | 100 | % | $F_{PWM}$=150Hz, $I_{LED}$=50mA |
| PWM frequency | $f_{PWM}$ | - | - | 20 | KHz | Duty=50%, $I_{LED}$=50mA |
| VDAC gain | $G_{VDAC}$ | - | 25 | - | mA/V | $V_{DAC}$=0～2V, $R_{ISET}$=120kΩ $I_{LED}$=VDAC÷$R_{ISET}$×Gain |
| Open detection voltage | $V_{OPEN}$ | 0.2 | 0.3 | 0.4 | V | $V_{LED}$= Sweep down |
| LED Short detection Voltage | $V_{SHORT}$ | 4.4 | 4.7 | 5.0 | V | $V_{OVP}$= Sweep up |
| LED Short Latch OFF Delay Time | $T_{SHORT}$ | 70 | 100 | 130 | ms | RT=100kΩ |
| PWM Latch OFF Delay Time | $T_{PWM}$ | 70 | 100 | 130 | ms | RT=100kΩ |
| **[Logic Inputs (EN, SYNC, PWM, LEDEN1, LEDEN2)]** | | | | | | |
| Input HIGH voltage | $V_{INH}$ | 2.1 | - | 5.5 | V | |
| Input LOW voltage | $V_{INL}$ | GND | - | 0.8 | V | |
| Input current 1 | $I_{IN}$ | 20 | 35 | 50 | µA | $V_{IN}$=5V (SYNC, PWM, LEDEN1, LEDEN2) |
| Input current 2 | $I_{EN}$ | 15 | 25 | 35 | µA | $V_{EN}$=5V (EN) |
| **[FAIL Output (open drain) ]** | | | | | | |
| FAIL LOW voltage | $V_{OL}$ | - | 0.1 | 0.2 | V | $I_{OL}$=0.1mA |

◎ This product is not designed for use in radioactive environments.

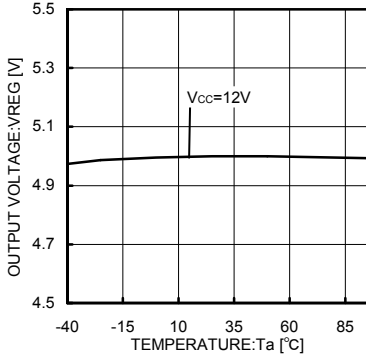●Reference data (unless otherwise specified, Ta=25℃)
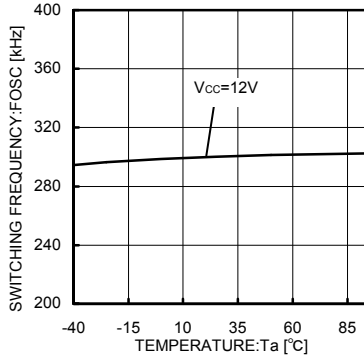


Fig.1 VREG
temperature characteristic



Fig.2 OSC
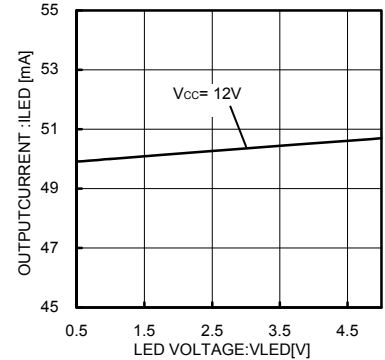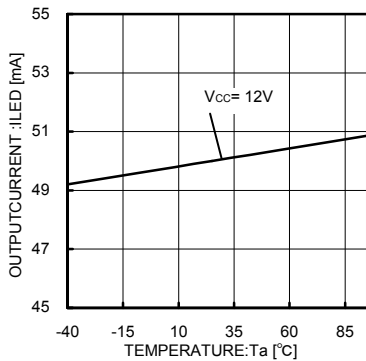temperature characteristic



Fig.3 ILED depend on VLED



Fig.4 ILED
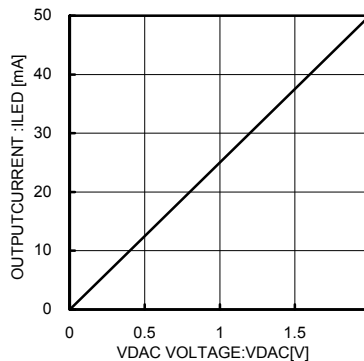temperature characteristic
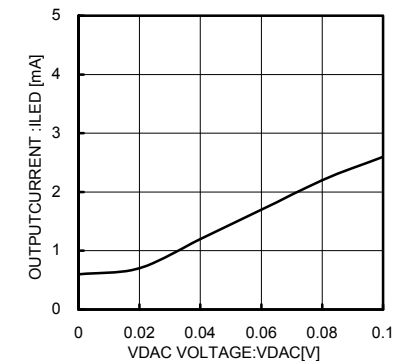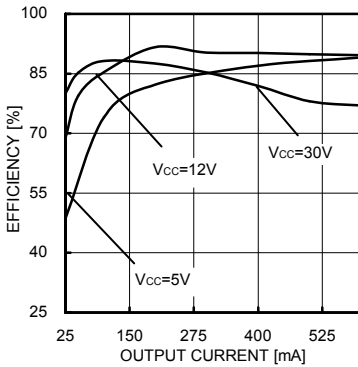


Fig.5 VDAC Gain①



Fig.6 VDAC Gain②
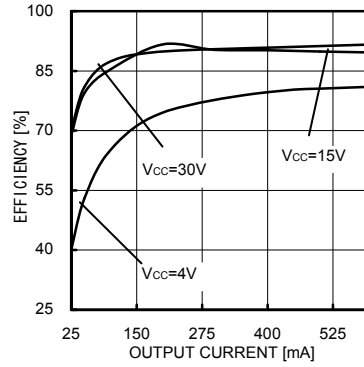


Fig.7 Efficiency
(Depend on input voltage)
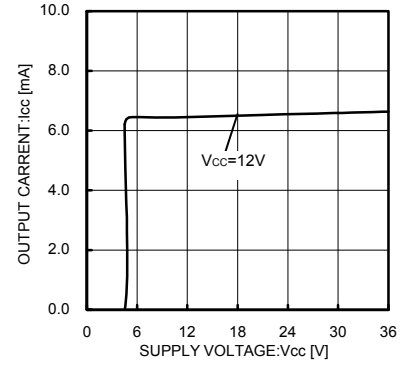


Fig.8 Efficiency
(Depend on output voltage)



Fig.9 Circuit Current
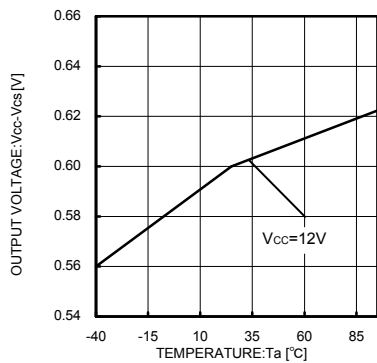(Switching OFF)



Fig.10 Overcurrent detecting
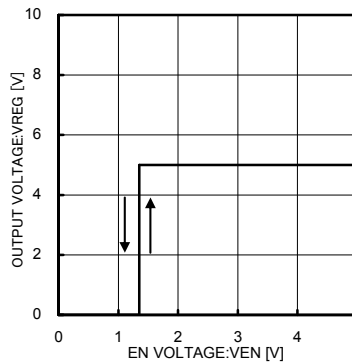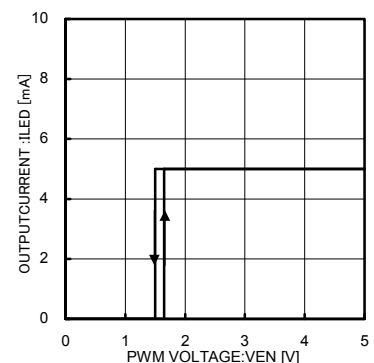voltage temperature characteristic



Fig.11 EN threshold voltage



Fig.12 PWM threshold voltage

●Block diagram


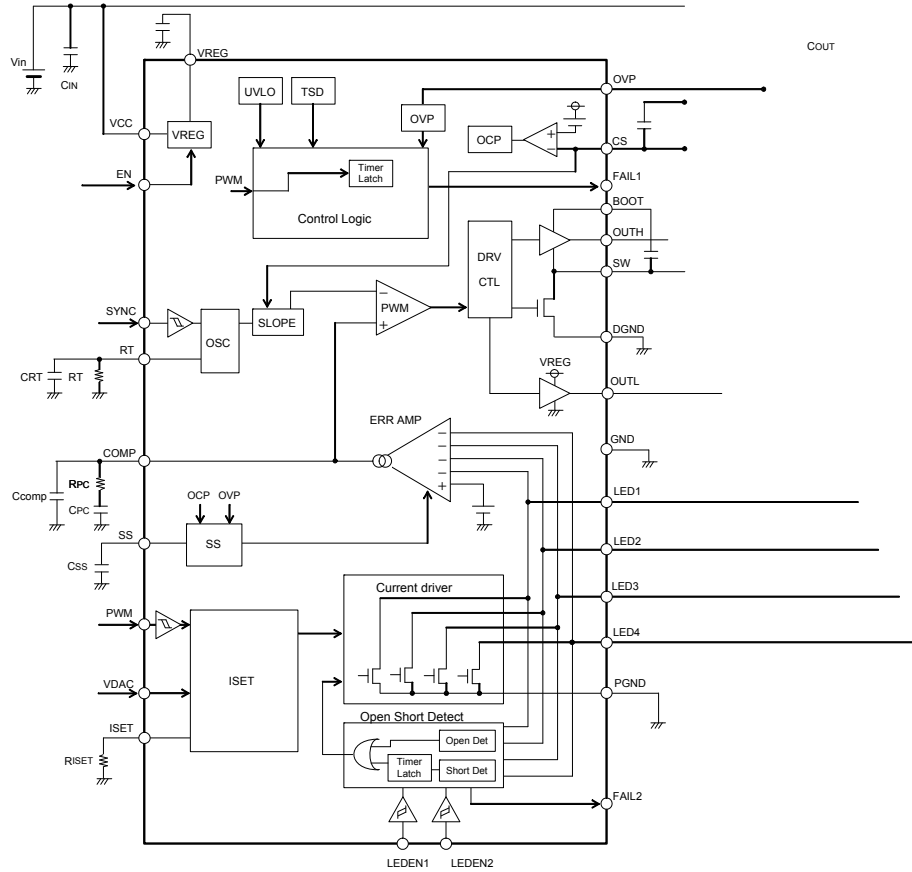
Fig.13

●Pin layout
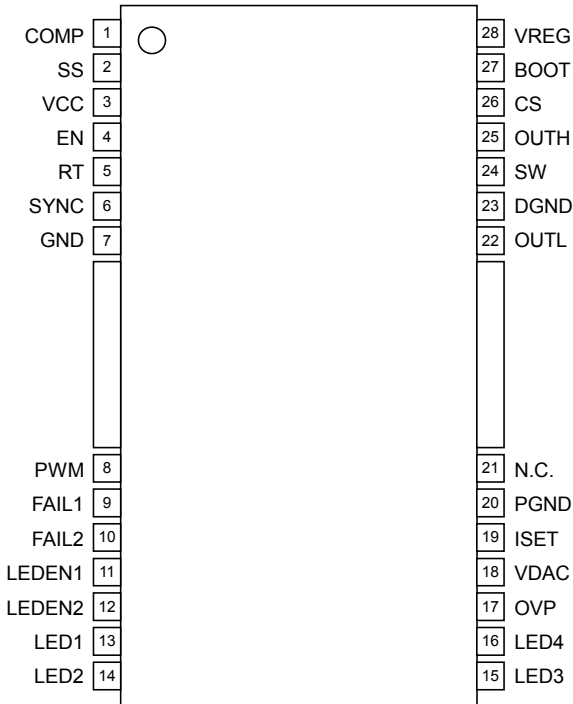


Fig.14

●Pin function table

| Pin | Symbol | Function |
|-----|--------|----------|
| 1 | COMP | Error amplifier output |
| 2 | SS | Soft start time-setting capacitance input |
| 3 | VCC | Input power supply |
| 4 | EN | Enable input |
| 5 | RT | Oscillation frequency-setting resistance input |
| 6 | SYNC | External synchronization signal input |
| 7 | GND | Small-signal GND |
| 8 | PWM | PWM light modulation input |
| 9 | FAIL1 | Failure signal output |
| 10 | FAIL2 | LED open/short detection signal output |
| 11 | LEDEN1 | LED output enable pin 1 |
| 12 | LEDEN2 | LED output enable pin 2 |
| 13 | LED1 | LED output 1 |
| 14 | LED2 | LED output 2 |
| 15 | LED3 | LED output 3 |
| 16 | LED4 | LED output 4 |
| 17 | OVP | Over-voltage detection input |
| 18 | VDAC | DC variable light modulation input |
| 19 | ISET | LED output current-setting resistance input |
| 20 | PGND | LED output GND |
| 21 | - | N.C. |
| 22 | OUTL | Low-side external MOSFET Gate Drive out put |
| 23 | DGND | Low-side internal MOSFET Source out put |
| 24 | SW | High-side external MOSFET Source pin |
| 25 | OUTH | High-side external MOSFET Gate Drive out pin |
| 26 | CS | DC/DC Current Sense Pin |
| 27 | BOOT | High-side MOSFET Power Supply pin |
| 28 | VREG | Internal reference voltage output |

● 5V voltage reference (VREG)

5V (Typ.) is generated from the $V_{CC}$ input voltage when the enable pin is set high. This voltage is used to power internal circuitry, as well as the voltage source for device pins that need to be fixed to a logical HIGH.

UVLO protection is integrated into the VREG pin. The voltage regulation circuitry operates uninterrupted for output voltages higher than 4.5 V (Typ.), but if output voltage drops to 4.3 V (Typ.) or lower, UVLO engages and turns the IC off.

Connect a capacitor (Creg = 2.2μF Typ.) to the VREG terminal for phase compensation. Operation may become unstable if Creg is not connected.

● Constant-current LED drivers

If less than four constant-current drivers are used, unused channels should be switched off via the LEDEN pin configuration. The truth table for these pins is shown below. If a driver output is enabled but not used (i.e. left open), the IC's open circuit-detection circuitry will operate. Please keep the unused pins open. The LEDEN terminals are pulled down internally in the IC, so if left open, the IC will recognize them as logic LO. However, they should be connected directly to VREG or fixed to a logic HI when in use.

| LED EN | | LED | | | |
|---|---|---|---|---|---|
| ⟨1⟩ | ⟨2⟩ | 1 | 2 | 3 | 4 |
| L | L | ON | ON | ON | ON |
| H | L | ON | ON | ON | OFF |
| L | H | ON | ON | OFF | OFF |
| H | H | ON | OFF | OFF | OFF |

· Output current setting

LED current is computed via the following equation:

$$I_{LED} = min[VDAC , VISET(=2.0V)] / RSET \times GAIN \text{ [A]}$$

(min[VDAC , 2.0V] = the smaller value of either VDAC or VISET; GAIN = set by internal circuitry.)

In applications where an external signal is used for output current control, a control voltage in the range of 0.1 to 2.0 V can be connected on the VDAC pin to control according to the above equation. If an external control signal is not used, connect the VDAC pin to VREG (do not leave the pin open as this may cause the IC to malfunction). Also, do not switch individual channels on or off via the LEDEN pin while operating in PWM mode.

The following diagram illustrates the relation between ILED and GAIN.

ILED vs GAIN
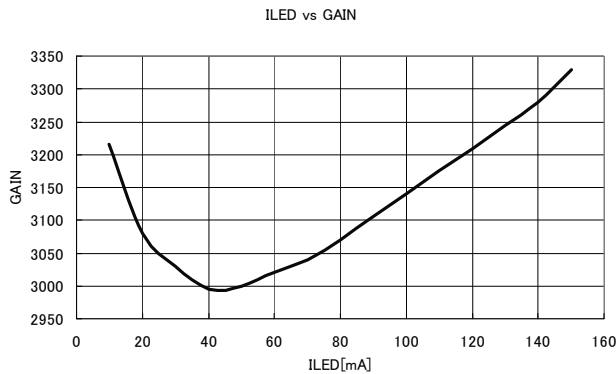


| ILED[mA] | GAIN |
|---|---|
| 10 | 3215 |
| 20 | 3080 |
| 30 | 3030 |
| 40 | 2995 |
| 50 | 3000 |
| 60 | 3020 |
| 70 | 3040 |
| 80 | 3070 |
| 90 | 3105 |
| 100 | 3140 |
| 110 | 3175 |
| 120 | 3210 |
| 130 | 3245 |
| 140 | 3280 |
| 150 | 3330 |

In PWM intensity control mode, the ON/OFF state of each current driver is controlled directly by the input signal on the PWM pin; thus, the duty ratio of the input signal on the PWM pin equals the duty ratio of the LED current. When not controlling intensity via PWM, fix the PWM terminal to a high voltage (100%). Output light intensity is greatest at 100% input.



PWM

ILED(50mA/div)

PWM=150Hz   Duty=0.38%



PWM

ILED

PWM=150Hz   Duty=50%
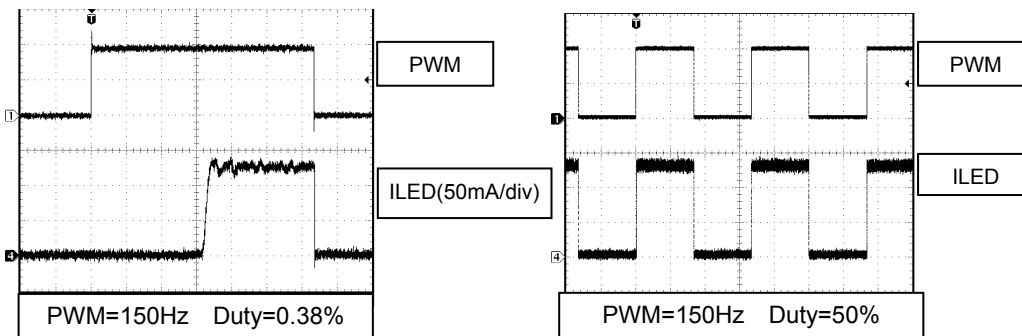
## ●Buck-Boost DC/DC controller

### ・Number of LEDs in series connection

Output voltage of the DCDC converter is controlled such that the forward voltage over each of the LEDs on the output is set to 1.0V (Typ.). DCDC operation is performed only when the LED output is operating. When two or more LED outputs are operating simultaneously, the LED voltage output is held at 1.0V (Typ.) per LED over the column of LEDs with the highest VF value.   The voltages of other LED outputs are increased only in relation to the fluctuation of voltage over this column.   Consideration should be given to the change in power dissipation due to variations in VF of the LEDs. Please determine the allowable maximum VF variance of the total LEDs in series by using the description as shown below:
VF variation allowable voltage 3.7V(Typ.) = short detecting voltage 4.7V(Typ.) - LED control voltage 1.0V(Typ.)
The number of LEDs that can be connected in series is limited due to the open-circuit protection circuit, which engages at 85% of the set OVP voltage.   Therefore, the maximum output voltage of the under normal operation becomes **30.6** V (= **36** V x **0.85**, where (**30.6** V – **1.0** V) / **VF** > **N** [maximum number of LEDs in series]).

### ・Over-voltage protection circuit (OVP)

The output of the DCDC converter should be connected to the OVP pin via a voltage divider.   In determining an appropriate trigger voltage of for OVP function, consider the total number of LEDs in series and the maximum variation in VF.   Also, bear in mind that over-current protection (OCP) is triggered at 0.85 x OVP trigger voltage.   If the OVP function engages, it will not release unless the DCDC voltage drops to 72.5% of the OVP trigger voltage.   For example, if ROVP1 (output voltage side), ROVP2 (GND side), and DCDC voltage VOUT are conditions for OVP, then:
**VOUT** ≥ (**ROVP1** + **ROVP2**) / **ROVP2** x **2.0** V.
OVP will engage when **VOUT** > **32** V if **ROVP1** = **330** kΩ and **ROVP2** = **22** kΩ.

### ・Buck-boost DC/DC converter oscillation frequency (FOSC)

The regulator's internal triangular wave oscillation frequency can be set via a resistor connected to the RT pin (pin 26). This resistor determines the charge/discharge current to the internal capacitor, thereby changing the oscillating frequency. Refer to the following theoretical formula when setting RT:

$$fosc = \frac{30 \times 10^6}{RT\,[\Omega]} \times \alpha \quad [kHz]$$

$30 \times 10^6$ (V/A/S) is a constant (±16.6%) determined by the internal circuitry, and α is a correction factor that varies in relation to RT: { RT: α = 50kΩ: 0.98, 60kΩ: 0.985, 70kΩ: 0.99, 80kΩ: 0.994, 90kΩ: 0.996, 100kΩ: 1.0, 50kΩ: 1.01, 200kΩ: 1.02, 300kΩ: 1.03, 400kΩ: 1.04, 500kΩ: 1.045 }
A resistor in the range of 62.6kΩ～523kΩ is recommended. Settings that deviate from the frequency range shown below may cause switching to stop, and proper operation cannot be guaranteed.
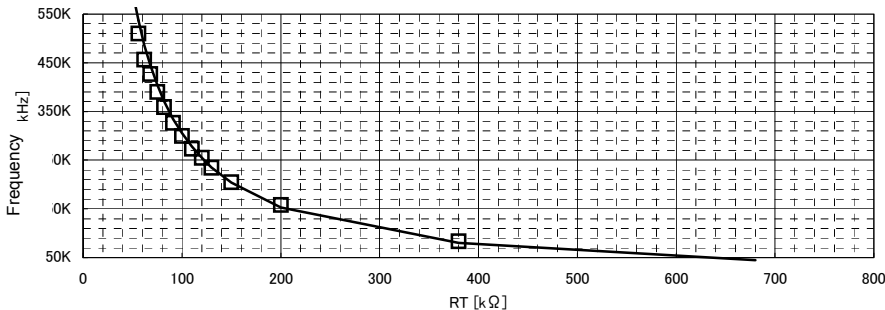


Fig.15 RT versus switching frequency

### ・External DC/DC converter oscillating frequency synchronization (FSYNC)

Do not switch from external to internal oscillation of the DC/DC converter if an external synchronization signal is present on the SYNC pin.   When the signal on the SYNC terminal is switched from high to low, a delay of about 30 µS (typ.) occurs before the internal oscillation circuitry starts to operate (only the rising edge of the input clock signal on the SYNC terminal is recognized).   Moreover, if external input frequency is less than the internal oscillation frequency, the internal oscillator will engage after the above-mentioned 30 µS (typ.) delay; thus, do not input a synchronization signal with a frequency less than the internal oscillation frequency.

・**Soft Start Function**
The soft-start (SS) limits the current and slows the rise-time of the output voltage during the start-up, and hence leads to prevention of the overshoot of the output voltage and the inrush current.

・**Self-diagnostic functions**
The operating status of the built-in protection circuitry is propagated to FAIL1 and FAIL2 pins (open-drain outputs). FAIL1 becomes low when UVLO, TSD, OVP, or SCP protection is engaged, whereas FAIL2 becomes low when open or short LED is detected.
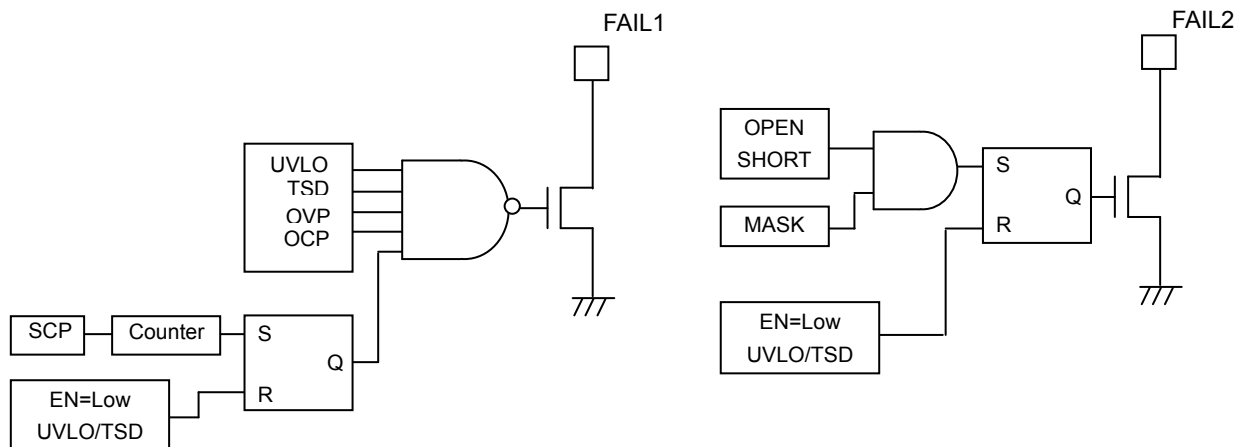


・**Operation of the Protection Circuitry**
・Under-Voltage Lock Out (UVLO)
The UVLO shuts down all the circuits other than REG when $VCC \leq 4.3V$ (TYP).
・Thermal Shut Down (TSD)
The TSD shuts down all the circuits other than REG when the Tj reaches 175℃ (TYP), and releases when the Tj becomes below 150℃ (TYP).
・Over Current Protection (OCP)
The OCP detects the current through the power-FET by monitoring the voltage of the high-side resistor, and activates when the CS voltage becomes less than VCC-0.6V (TYP).
When the OCP is activated, the external capacitor of the SS pin becomes discharged and the switching operation of the DCDC turns off.
・Over Voltage Protection (OVP)
The output voltage of the DCDC is detected with the OVP-pin voltage, and the protection activates when the OVP-pin voltage becomes greater than 2.0V (TYP).
When the OVP is activated, the external capacitor of the SS pin becomes discharged and the switching operation of the DCDC turns off.

・**Short Circuit Protection (SCP)**
When the LED-pin voltage becomes less than 0.3V (TYP), the internal counter starts operating and latches off the circuit approximately after 100ms (when FOSC = 300kHz). If the LED-pin voltage becomes over 0.3V before 100ms, then the counter resets.
When the LED anode (i.e. DCDC output voltage) is shorted to ground, then the LED current becomes off and the LED-pin voltage becomes low. Furthermore, the LED current also becomes off when the LED cathode is shorted to ground. Hence in summary, the SCP works with both cases of the LED anode and the cathode being shorted.

・**LED Open Detection**
When the LED-pin voltage $\leq 0.3V$ (TYP) as well as OVP-pin voltage $\geq 1.7V$ (TYP) simultaneously, the device detects as LED open and latches off that particular channel.

・LED Short Detection

When the LED-pin voltage ≥ 4.7V (TYP) as well as OVP-pin voltage ≤ 1.6V (TYP) simultaneously the internal counter starts operating, and approximately after 100ms (when FOSC = 300kHz) the only detected channel (as LED short) latches off. With the PWM brightness control, the detecting operation is processed only when PWM-pin = High. If the condition of the detection operation is released before 100ms (when FOSC = 300kHz), then the internal counter resets.

※ The counter frequency is the DCDC switching frequency determined by the RT. The latch proceeds at the count of 32770.

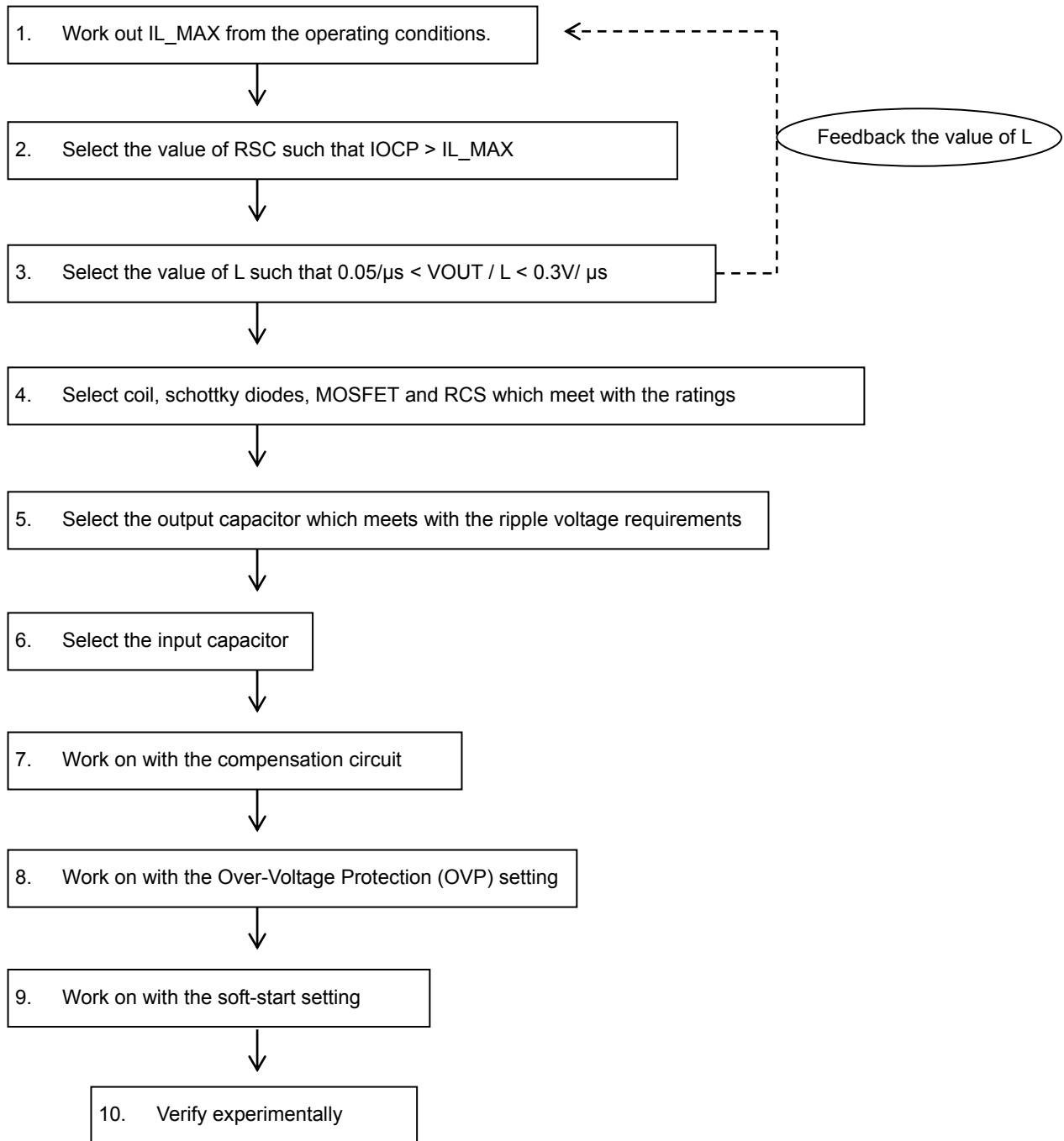| Protection | Detecting Condition | | Operation after detect |
|---|---|---|---|
| | [Detect] | [Release] | |
| UVLO | VREG<4.3V | VREG>4.5V | All blocks shut down |
| TSD | Tj>175℃ | Tj<150℃ | All blocks (but except REG) shut down |
| OVP | VOVP>2.0V | VOVP<1.45V | SS discharged |
| OCP | VCS≦VCC-0.6V | VCS>VCC-0.6V | SS discharged |
| SCP | VLED<0.3V (100ms delay when FOSC=300kHz) | EN or UVLO | Counter starts and then latches off all blocks (but except REG) |
| LED open | VLED<0.3V & VOVP>1.7V | EN or UVLO | The only detected channel latches off |
| LED short | VLED>4.7V & VOVP<1.6V (100ms delay when FOSC=300kHz) | EN or UVLO | The only detected channel latches off (after the counter sets) |

●Protection Sequence
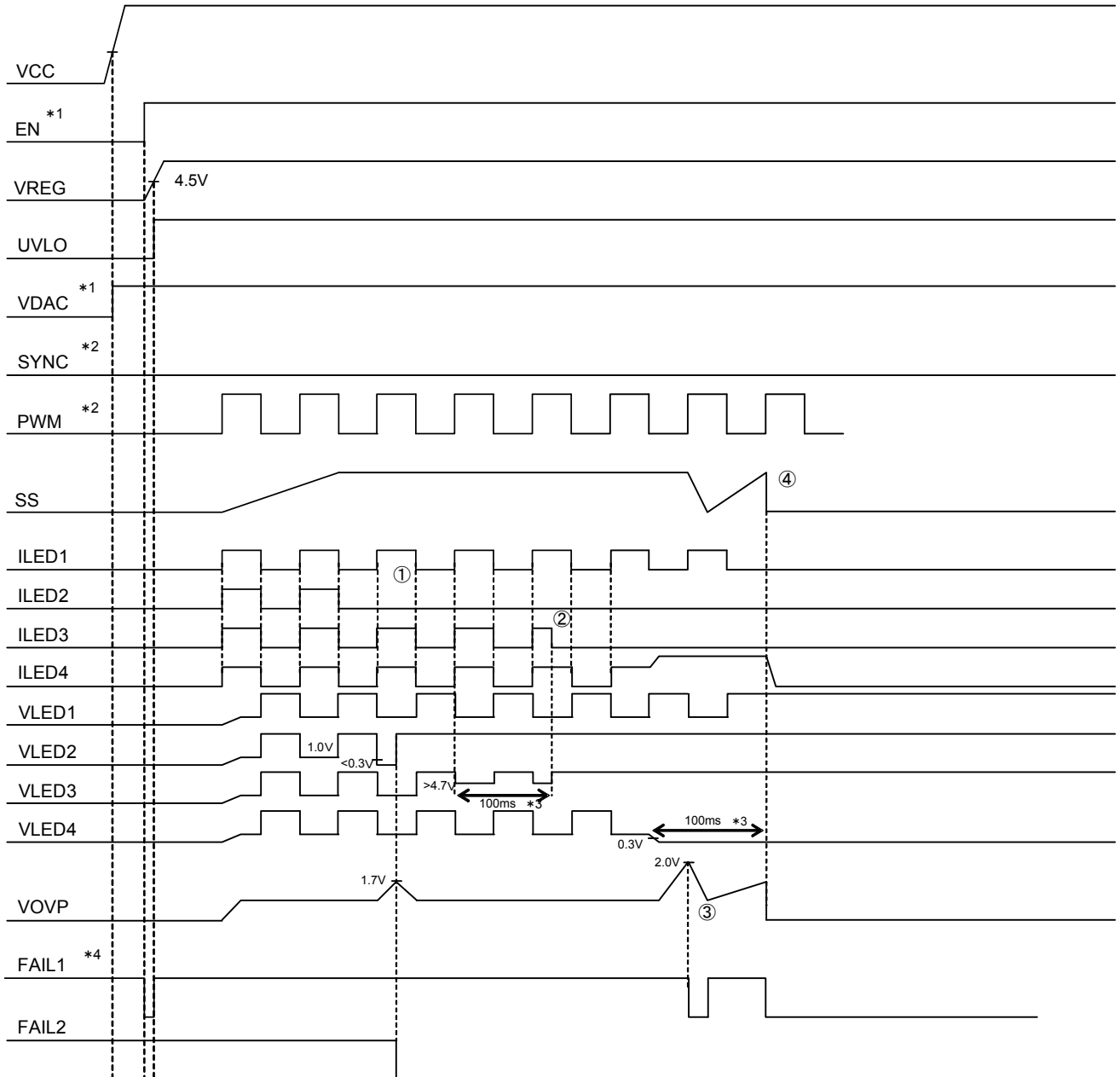


| | |
|---|---|
| *1 | Turn on the EN after the VCC is on |
| *2 | SYNC and PWM inputs are allowed to be on beforethe VCC is on |
| *3 | Aprox 100ms of delay when Fosc = 300kHz |

① Case for LED2 in open-mode
 When VLED2＜0.3V and VOVP＞1.7V simultaneously, then LED2 becomes off and FAIL2 becomes low
② Case for LED3 in short-mode
 When VLED3＞4.7V and VOVP＜1.6V simultaneously, then LED3 becomes off after 100ms approx
③ Case for LED4 in short to GND
 ③-1 DCDC output voltage increases, and then SS dichages and FAIL1 becomes low
 ③-2 Detects VLED4<0.3V and shuts down after 100ms approx

● Procedure for external components selection
    Follow the steps as shown below for selecting the external components

1.  Work out IL_MAX from the operating conditions.

Feedback the value of L

2.  Select the value of RSC such that IOCP > IL_MAX

3.  Select the value of L such that 0.05/μs < VOUT / L < 0.3V/ μs

4.  Select coil, schottky diodes, MOSFET and RCS which meet with the ratings

5.  Select the output capacitor which meets with the ripple voltage requirements

6.  Select the input capacitor

7.  Work on with the compensation circuit

8.  Work on with the Over-Voltage Protection (OVP) setting

9.  Work on with the soft-start setting

10.  Verify experimentally

1. Computation of the Input Peak Current and IL_MAX
   ① Calculation of the maximum output voltage (Vout_max)
   To calculate the Vout_max, it is necessary to take into account of the VF variation and the number of LED connection in series.
   Vout_max = (VF + ΔVF) × N + 1.0V          ΔVF: VF Variation    N: Number of LED connection in series

   ② Calculation of the output current Iout
   Iout = ILED × 1.05 × M          Number of LED connection in parallel

   ③ Calculation of the input peak current IL_MAX
   IL_MAX = IL_AVG + 1/2 ΔIL
   IL_AVG = (VIN + Vout) × Iout / (n × VIN)

   $$\Delta IL= \frac{VIN}{L} \times \frac{1}{Fosc} \times \frac{Vout}{VIN+Vout}$$          n: efficiency    Fosc: switching frequency

   ・The worst case scenario for VIN is when it is at the minimum, and thus the minimum value should be applied in the equation.
   ・The L value of 10μF ~ 47μF is recommended. The current-mode type of DC/DC conversion is adopted for BD8119FM-M, which is optimized with the use of the recommended L value in the design stage. This recommendation is based upon the efficiency as well as the stability. The L values outside this recommended range may cause irregular switching waveform and hence deteriorate stable operation.
   ・n (efficiency) is approximately 80%
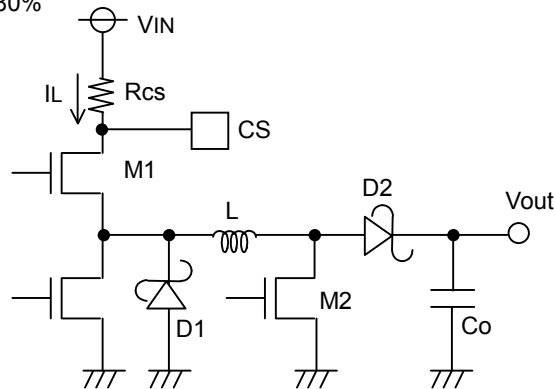


External Application Circuit

2. The setting of over-current protection
   Choose Rcs with the use of the equation Vocp_min (=0.54V) / Rcs > IL_MAX
   When investigating the margin, it is worth noting that the L value may vary by approximately ±30%.

3. The selection of the L
   In order to achieve stable operation of the current-mode DC/DC converter, we recommend selecting the L value in the range indicated below:

   $$0.05\ [V/\mu S] < \frac{Vout \times Rcs}{L} < 0.3\ [V/\mu S]$$

   The smaller $\frac{Vout \times Rcs}{L}$ allows stability improvement but slows down the response time.

4. Selection of coil L, diode D1 and D2, MOSFET M1 and M2, and Rcs

| | Current rating | Voltage rating | Heat loss |
|---|---|---|---|
| Coil L | > IL_MAX | — | |
| Diode D1 | > Iocp | > VIN_MAX | |
| Diode D2 | > Iocp | > Vout | |
| MOSFET M1 | > Iocp | > VIN_MAX | |
| MOSFET M2 | > Iocp | > Vout | |
| Rcs | — | — | > Iocp$^2$ × Rcs |

   ※ Allow some margin, such as the tolerance of the external components, when selecting.
   ※ In order to achieve fast switching, choose the MOSFETs with the smaller gate-capacitance.

5. Selection of the output capacitor
   Select the output capacitor Cout based on the requirement of the ripple voltage Vpp.

$$Vpp = \frac{Iout}{Cout} \times \frac{Vout}{Vout+VIN} \times \frac{1}{Fosc} + IL\_MIN \times RESR$$

   Choose Cout that allows the Vpp to settle within the requirement. Allow some margin also, such as the tolerance of the external components.

6. Selection of the input capacitor
   A capacitor at the input is also required as the peak current flows between the input and the output in DC/DC conversion. We recommend an input capacitor greater than 10µF with the ESR smaller than 100mΩ. The input capacitor outside of our recommendation may cause large ripple voltage at the input and hence lead to malfunction.

7. Phase Compensation Guidelines
   In general, the negative feedback loop is stable when the following condition is met:
   ・Overall gain of 1 (0dB) with a phase lag of less than 150º (i.e., a phase margin of 30º or more)
   However, as the DC/DC converter constantly samples the switching frequency, the gain-bandwidth (GBW) product of the entire series should be set to 1/10 the switching frequency of the system.   Therefore, the overall stability characteristics of the application are as follows:
   ・Overall gain of 1 (0dB) with a phase lag of less than 150º (i.e., a phase margin of 30º or more)
   ・GBW (frequency at gain 0dB) of 1/10 the switching frequency
   Thus, to improve response within the GBW product limits, the switching frequency must be increased.

   The key for achieving stability is to place fz near to the GBW.



$$\text{Phase-lead} \quad fz = \frac{1}{2\pi\,CpcRpc} \quad [Hz]$$

$$\text{Phase-lag} \quad fp1 = \frac{1}{2\pi\,RLCout} \quad [Hz]$$
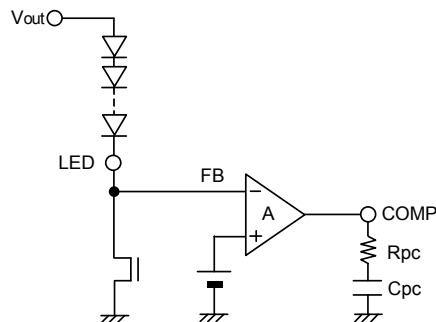
   Good stability would be obtained when the fz is set between 1kHz～10kHz.

   In buck-boost applications, Right-Hand-Plane (RHP) Zero exists. This Zero has no gain but a pole characteristic in terms of phase. As this Zero would cause instability when it is in the control loop, so it is necessary to bring this zero before the GBW.

$$fRHP = \frac{Vout+VIN/(Vout+VIN)}{2\pi\,I_{LOAD}L} \quad [Hz] \qquad I_{LOAD}: \text{Maximum Load Current}$$

   It is important to keep in mind that these are very loose guidelines, and adjustments may have to be made to ensure stability in the actual circuitry.   It is also important to note that stability characteristics can change greatly depending on factors such as substrate layout and load conditions.   Therefore, when designing for mass-production, stability should be thoroughly investigated and confirmed in the actual physical design.

8. Setting of the over-voltage protection
We recommend setting the over-voltage protection Vovp
1.2V to 1.5V greater than Vout which is adjusted by the
number of LEDs in series connection. Less than 1.2V may
cause unexpected detection of the LED open and short during
the PWM brightness control. For the Vovp greater than 1.5V,
the LED short detection may become invalid.
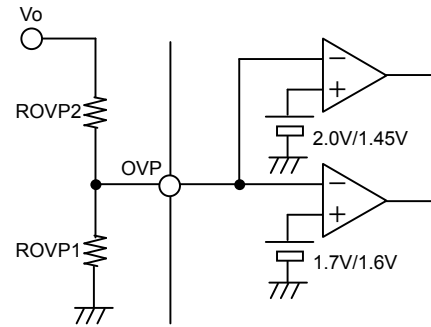


9. Setting of the soft-start
The soft-start allows minimization of the coil current as well as the overshoot of the output voltage at the start-up.

For the capacitance we recommend in the range of 0.001 ~ 0.1μF. For the capacitance less than 0.001μF may cause
overshoot of the output voltage. For the capacitance greater than 0.1μF may cause massive reverse current through the
parasitic elements of the IC and damage the whole device. In case it is necessary to use the capacitance greater than
0.1μF, ensure to have a reverse current protection diode at the Vcc or a bypass diode placed between the SS-pin and
the Vcc.

Soft-start time TSS

TSS = CSSX0.7V / 5μA [s]                    CSS: The capacitance at the SS-pin

10 Verification of the operation by taking measurements
The overall characteristic may change by load current, input voltage, output voltage, inductance, load capacitance,
switching frequency, and the PCB layout. We strongly recommend verifying your design by taking the actual
measurements.

## ●Power Dissipation Calculation

Power dissipation can be calculated as follows:

**Pc(N) = ICC\*VCC + 2\*Ciss\*VREG\*Fsw\*Vcc+[VLED\*N+△Vf\*(N-1)]\*ILED**

$I_{CC}$     Maximum circuit current
$V_{CC}$     Supply power voltage
$C_{iss}$     External FET capacitance
$V_{sw}$     SW gate voltage
$F_{sw}$     SE frequency
$V_{LED}$     LED control voltage
$N$     LED parallel numeral
$\Delta V_f$     LED $V_f$ fluctuation
$I_{LED}$     LED output current

Sample Calculation:

Pc(4) = 10mA × 30V + 500pF × 5V × 300kHz × 30V + [1.0V × 4 + △Vf × 3] × 100mA
△Vf = 3.0V, Pc (4) = 322.5mW + 1.3W = 1622.5mW
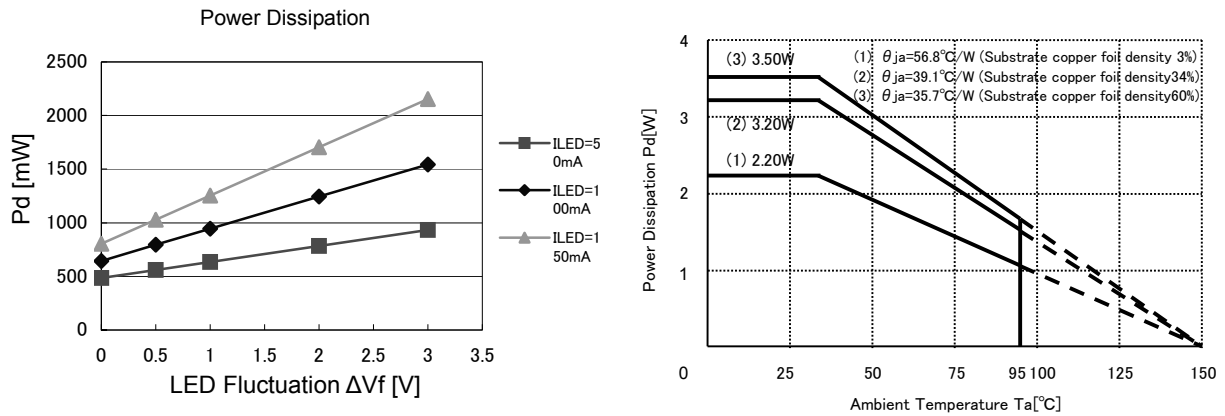


Fig.16

Note 1: Power dissipation calculated when mounted on 70mm X 70mm X 1.6mm glass epoxy substrate (1-layer platform/copper thickness 18μm)
Note 2: Power dissipation changes with the copper foil density of the board.
    The area of the copper foil becomes the total area of the heat radiation fin and the foot pattern (connected directly with IC) of this IC.
    This value represents only observed values, not guaranteed values.

Pd=2200mW ( 968mW): Substrate copper foil density   3%
Pd=3200mW (1408mW): Substrate copper foil density 34%
Pd=3500mW (1540mW): Substrate copper foil density 60% (Value within parentheses represents power dissipation when Ta=95℃)

Note 3: Please design so that ambient temperature + self-generation of heat may become 150℃ or less because this IC is Tj=150℃.
Note 4: Please note the heat design because there is a possibility that thermal resistance rises from the examination result of the temperature cycle
    by 20% or less.
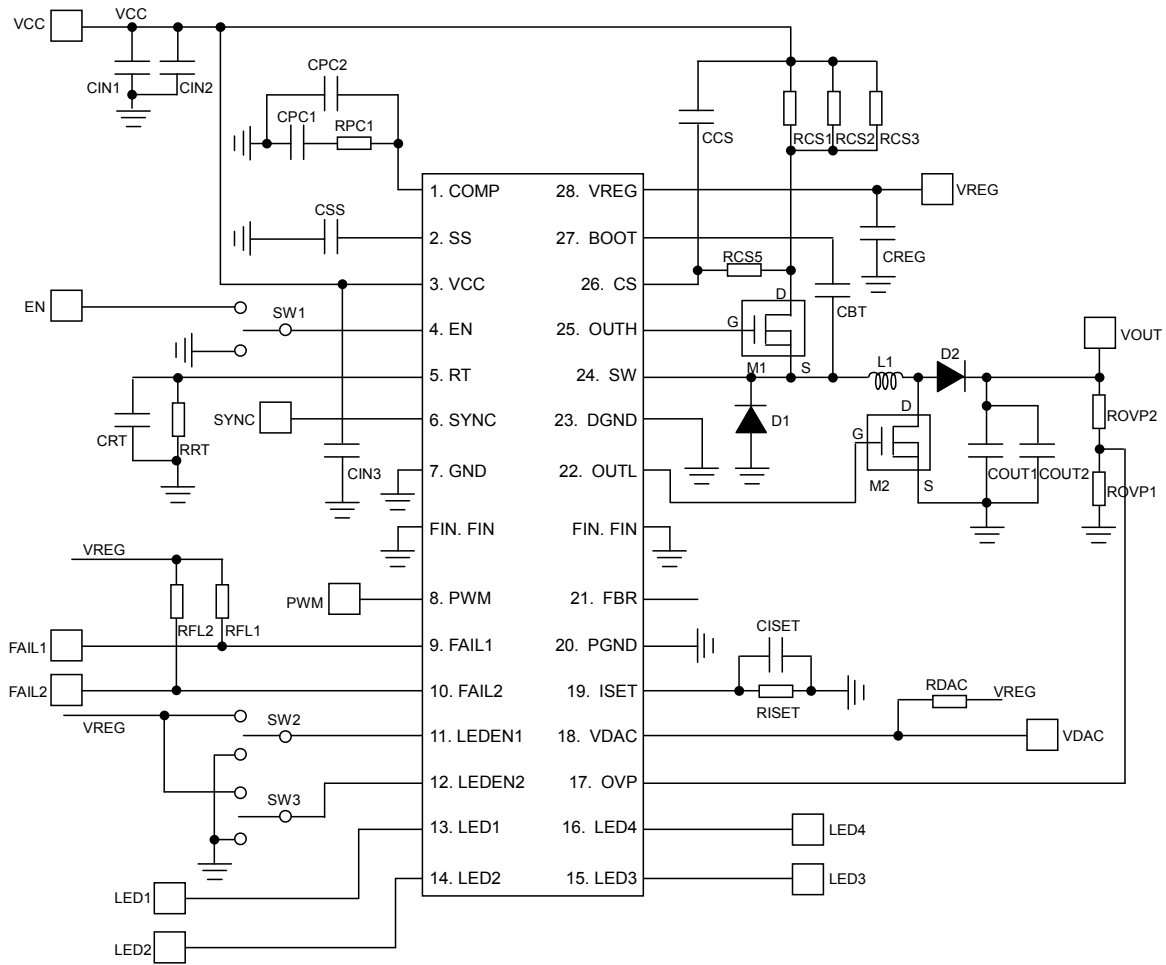
- The coupling capacitors CVCC and CREG should be mounted as close as possible to the IC's pins.
- Large currents may pass through DGND and PGND, so each should have its own low-impedance routing to the system ground.
- Noise should be minimized as much as possible on pins VDAC, ISET,RT and COMP.
- PWM, SYNC and LED1-4 carry switching signals, so ensure during layout that surrounding traces are not affected by crosstalk.

●Application Board Part List

| serial No. | component name | component value | product name | Manufacturer |
|---|---|---|---|---|
| 1 | CIN1 | 10μF | GRM31CB31E106KA75B | murata |
| 2 | CIN2 | — | | |
| 3 | CIN3 | — | | |
| 4 | CPC1 | 0.1μF | | |
| 5 | CPC2 | — | | murata |
| 6 | RPC1 | 510Ω | | |
| 7 | CSS | 0.1μF | GRM188B31H104KA92 | murata |
| 8 | RRT | 100kΩ | MCR03 Series | Rohm |
| 9 | CRT | — | | |
| 10 | RFL1 | 100kΩ | MCR03 Series | Rohm |
| 11 | RFL2 | 100kΩ | MCR03 Series | Rohm |
| 12 | CCS | — | | |
| 13 | RCS1 | 620mΩ | MCR100JZHFSR620 | Rohm |
| 14 | RCS2 | 620mΩ | MCR100JZHFSR620 | Rohm |
| 15 | RCS3 | — | | |
| 16 | RCS5 | 0Ω | | |
| 17 | CREG | 2.2μF | GRM188B31A225KE33 | murata |
| 18 | CBT | 0.1μF | GRM188B31H104KA92 | murata |
| 19 | M1 | — | RSS070N05 | Rohm |
| 20 | M2 | — | RSS070N05 | Rohm |
| 21 | D1 | — | RB050L-40 | Rohm |
| 22 | D2 | — | RF201L2S | Rohm |
| 23 | L1 | 33μH | CDRH105R330 | Sumida |
| 24 | COUT1 | 10μF | GRM31CB31E106KA75B | murata |
| 25 | COUT2 | 10μF | GRM31CB31E106KA75B | murata |
| 26 | ROVP1 | 30kΩ | MCR03 Series | Rohm |
| 27 | ROVP2 | 360kΩ | MCR03 Series | Rohm |
| 28 | RISET | 120kΩ | MCR03 Series | Rohm |
| 29 | CISET | — | | |
| 30 | RDAC | 0Ω | | |

‧The above values are fixed numbers for confirmed operation with the following conditions: $V_{CC}$ = 12V, four parallel channels of five series-connected LEDs, and ILED=50mA.
‧Optimal values of external components depend on the actual application; these values should only be used as guidelines and should be adjusted to fit the operating conditions of the actual application.

When performing open/short tests of the external components, the open condition of D1 or D2 may cause permanent damage to the driver and/or the external components. In order to prevent this, we recommend having parallel connections for D1 and D2.

● Input/output Equivalent Circuits (terminal name follows pin number)

| 1. COMP | 2. SS | 4. EN |
|---|---|---|
| VREG, VREG, 2K, 2K, COMP | VREG, Vcc, 1K, SS | Vcc, 10k, 175k, 135k, EN |
| **5. RT** | **6. SYNC, 8. PWM** | **9. FAIL1, 10. FAIL2** |
| VREG, 167, RT | 3.3V, 10K, 150K, SYNC PWM | 1K, FAIL1 FAIL2 |
| **11. LEDEN1, 12. LEDEN2** | **13. LED1, 14. LED2, 15. LED3, 16. LED4** | **17. OVP** |
| 3.3V, 10K, 10K, 150K, LEDEN1 LEDEN2 | 5K, 2.5K, LED1~4 | Vcc, 10K, 5K, OVP |
| **18. VDAC** | **19. ISET** | **22. OUTL** |
| VREG, Vcc, 500, VDAC | VREG, Vcc, 500, 12.5, ISET | VREG, VREG, 100K, OUTL |
| **24. SW** | **25. OUTH** | **26. CS** |
| Vcc, SW | BOOT, BOOT, 100K, OUTH, SW SW SW | Vcc, 5K, CS |
| **27. BOOT** | **28. VREG** | **21.** |
| VREG, BOOT, SW | VREG, Vcc, VREG, 205K, 100K | N.C.  N.C. = no connection (open) |

※All values typical.

●Notes for use

1) Absolute maximum ratings
Use of the IC in excess of absolute maximum ratings (such as the input voltage or operating temperature range) may result in damage to the IC. Assumptions should not be made regarding the state of the IC (e.g., short mode or open mode) when such damage is suffered. If operational values are expected to exceed the maximum ratings for the device, consider adding protective circuitry (such as fuses) to eliminate the risk of damaging the IC.

2) GND potential
Ensure that the GND pin is held at the minimum potential in all operating conditions.

3) Thermal Design
Use a thermal design that allows for a sufficient margin for power dissipation (Pd) under actual operating conditions.

4) Inter-pin shorts and mounting errors
Use caution when orienting and positioning the IC for mounting on printed circuit boards. Improper mounting may result in damage to the IC. Shorts between output pins or between output pins and the power supply and GND pins caused by poor soldering or foreign objects may result in damage to the IC.

5) Operation in strong electromagnetic fields
Exercise caution when using the IC in the presence of strong electromagnetic fields as doing so may cause the IC to malfunction.

6) Testing on application boards
When testing the IC on an application board, connecting a capacitor directly to a low-impedance pin may subject the IC to stress. Always discharge capacitors completely after each process or step. The IC's power supply should always be turned off completely before connecting or removing it from a jig or fixture during the evaluation process.  To prevent damage from static discharge, ground the IC during assembly and use similar precautions during transport and storage.

7) Ground wiring patterns
When using both small-signal and large-current GND traces, the two ground traces should be routed separately but connected to a single ground potential within the application in order to avoid variations in the small-signal ground caused by large currents.   Also ensure that the GND traces of external components do not cause variations on GND voltage.

8) IC input pins and parasitic elements
This monolithic IC contains P+ isolation and P substrate layers between adjacent elements in order to keep them isolated. PN junctions are formed at the intersection of these P layers with the N layers of other elements, creating parasitic diodes and/or transistors.   For example (refer to the figure below):



Example of IC Structure
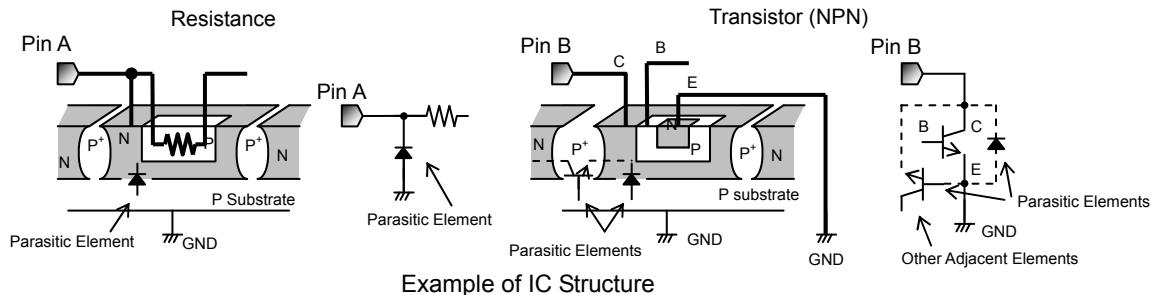
・ When GND > Pin A and GND > Pin B, the PN junction operates as a parasitic diode
・ When GND > Pin B, the PN junction operates as a parasitic transistor

Parasitic diodes occur inevitably in the structure of the IC, and the operation of these parasitic diodes can result in mutual interference among circuits, operational faults, or physical damage.   Accordingly, conditions that cause these diodes to operate, such as applying a voltage lower than the GND voltage to an input pin (and thus to the P substrate) should be avoided.
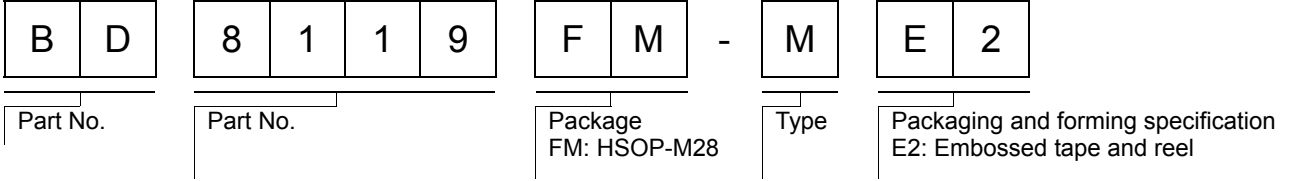
9) Over-current protection circuits
An over-current protection circuit (designed according to the output current) is integrated into the IC to prevent damage in the event of load shorting. This protection circuit is effective in preventing damage due to sudden and unexpected overloads on the output. However, the IC should not be used in applications where operation of the OCP function is anticipated or assumed
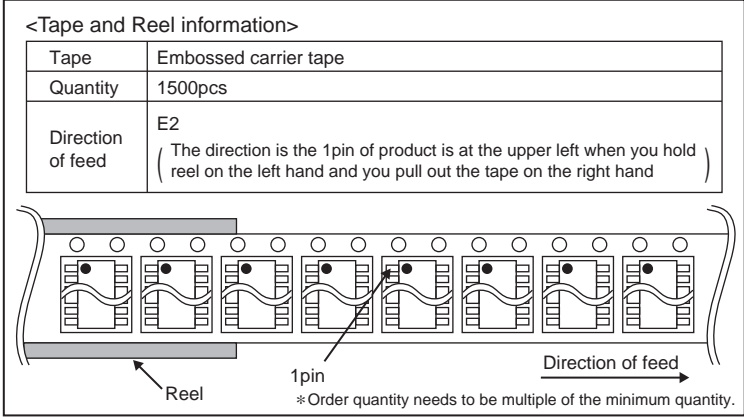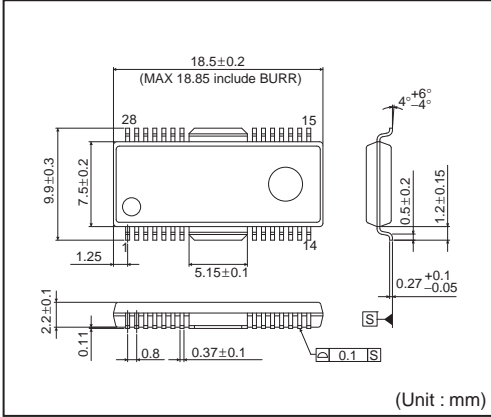
10) Thermal shutdown circuit (TSD)
This IC also incorporates a built-in TSD circuit for the protection from thermal destruction. The IC should be used within the specified power dissipation range. However, in the event that the IC continues to be operated in excess of its power dissipation limits, the rise in the chip's junction temperature $T_j$ will trigger the TSD circuit, shutting off all output power elements. The circuit automatically resets itself once the junction temperature $T_j$ drops down to normal operating temperatures.   The TSD protection will only engage when the IC's absolute maximum ratings have been exceeded; therefore, application designs should never attempt to purposely make use of the TSD function.

●Ordering part number

| B | D | | 8 | 1 | 1 | 9 | | F | M | - | M | | E | 2 |

Part No.    Part No.                    Package      Type    Packaging and forming specification
                                        FM: HSOP-M28          E2: Embossed tape and reel

**HSOP-M28**



18.5±0.2
(MAX 18.85 include BURR)

28          15

9.9±0.3   7.5±0.2

1.25    1          14
       5.15±0.1

2.2±0.1

0.11    0.8    0.37±0.1

4°⁺⁶°₋₄°

0.5±0.2   1.2±0.15

0.27⁺⁰·¹₋₀.₀₅

S

0.1  S

(Unit : mm)

<Tape and Reel information>

| Tape | Embossed carrier tape |
|---|---|
| Quantity | 1500pcs |
| Direction of feed | E2<br>( The direction is the 1pin of product is at the upper left when you hold reel on the left hand and you pull out the tape on the right hand ) |



Reel          1pin          Direction of feed
         ＊Order quantity needs to be multiple of the minimum quantity.

Thank you for your accessing to ROHM product informations.
More detail product informations and catalogs are available, please contact us.

## ROHM  Customer Support System

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