

# HD-15531

# CMOS Manchester **Encoder-Decoder**

### Features

- Support of MIL-STD-1553
- 2.5 Megabit/Sec Data Rate (15531B)
- 1.25 Megabit/Sec Data Rate (15531)
- Sync identification and Lock-in
- Clock Recovery
- Variable Frame Length to 32-Bits
- · Manchester II Encode, Decode
- . Separate Encode and Decode
- Low Operating Power......50mW @ 5 Volts
- Full -55°C to +125°C Temperature Range Operation

### Description

The Harris HD-15531 is a high performance CMOS device intended to service the requirements of MIL-STD-1553 and similar Manchester II encoded, time division multiplexed serial data protocols. This LSI chip is divided into two sections, an Encoder and a Decoder. These sections operate independently of each other, except for the master reset and word length functions.

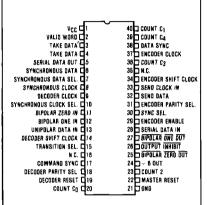
This circuit provides many of the requirements of MIL-STD-1553. The Encoder produces the sync pulse and the parity bit as well as the encoding of the data bits. The Decoder recognizes the sync pulse and identifies it as well as decoding the data bits and checking parity.

The HD-15531 also surpasses the requirements of MIL-STD-1553 by allowing the word length to be programmable (from 2 to 28 data bits). A frame consists of three bits for sync followed by the data word (2 to 28 data bits) followed by one bit of parity, thus the frame length will vary from 6 to 32 bit periods. This chip also allows selection of either even or odd parity for the Encoder and Decoder separately.

This integrated circuit is fully guaranteed to support the 1MHz data rate of MIL-STD-1553 over both temperature and voltage. For high speed applications the 15531B will support a 2.5 Megabit/sec data rate.

The HD-15531 can also be used in many party line digital data communications applications, such as a local area network or an environmental control system driven from a single twisted pair of fiber optic cable throughout a building.

### Pinout TOP VIEW



### **Block Diagrams**

### ENCODER DECODER 21 > GND SYNCHRONOUS DATA 22 MASTER RESET 26 OUTPUT SEND CLOCK IN BIPOLAR ONE IN COMMAND SYNC TRANSITION - 6 OUT DATA SYNC CHARACTER BIPOLAR ZERO IN 26 BIPOLAR ZERO OUT SERIAL DATA OUT DECODER > 37 > ENCODER VALID WORD CLOCK SYNCHRONIZE SELECT 18 PARITY SELECT DECODER > SYNCHRONOUS CLOCK BIT COUNTER 14 DECODER SHIFT SYNCHRONOUS CLOCK SELECT 20 40 23 36 39 Co C1 C2 C3 C4 3 TAKE DATA BIT COUNTER ENCORER ENCORER ENCORER ENABLE

Caution. These devices are sensitive to electronic discharge. Proger I.C. handling procedures should be followed

### Specifications HD-15531

### Absolute Maximum Ratings Supply Voltage..... .....+7.0 Volts θ<sub>ia</sub>......45°C/W (CERDIP package), 50°C/W (LCC package) Input, Output or I/O Voltage Applied ......GND -0.3V to VCC +0.3V Gate Count 456 Gates Storage Temperature Range .....-65°C to +150°C Junction Temperature.....+150°C Lead Temperature (Soldering, Ten Seconds)..... θ<sub>ic</sub>......17°C/W (CERDIP package), 23°C/W (LCC package) CAUTION: Stresses above those listed in the "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Operating Conditions Operating Voltage Range ......+4.5V to +5.5V Operating Temperature Range -40°C to +85°C HD-15531-2/-8 .....-55°C to +125°C **Electrical Specifciations** $T_A = -40^{\circ}\text{C}$ to +85°C (HD-15531-9), $T_A = -55^{\circ}\text{C}$ to +125°C (HD-15531-2/-8) SYMBOL PARAMETER MIN TYP MAX UNITS **TEST CONDITIONS** Logical "1" Input Voltage 70% VCC Logical "0" Input Voltage $v_{\mathsf{IL}}$ 20% V<sub>CC</sub> v Logical "1" Input Voltage (Clock) v VIHC VCC -0.5 VILC Logical "0" Input Voltage (Clock) GND +0.5 Input Leakage -10 +1.0 μΑ V<sub>IN</sub> = V<sub>CC</sub> or GND, DIP Pins 6-13, 15, 18, 19, 20, 22, 23, 26, 28-31, 33, 36 IOH = -3mA IOL = 1.8mA VIN = VCC = 5.5V Outputs Open Logical "1" Output Voltage Logical "0" Output Voltage 2.4 VOH VOL D.C. 0.4 <sup>I</sup>CCSB Supply Current Standby 0.5 20 mΑ V<sub>CC</sub> = 5.5V f = 15MHz Supply Current Operating 8.0 10.0 ICCOP CIN mΑ Input Capacitance All measurements are 10 рF referenced to device $c_0$ Output Capacitance 14 pF GND, T<sub>A</sub> = +25°C, F = 1MHz \*Guaranteed and sampled but not 100% tested ENCODER TIMING VCC - $5.0V \pm 10\%$ (1) FEC Encoder Clock Frequency MHz $C_I = 50pF$ (2) FESC Send Clock Frequency 0 2.5 MHz (3) TECR Encoder Clock Rise Time ns (4) TECF Encoder Clock Fall Time ns (5) F<sub>ED</sub> Data Rate n 1.25 MHz Master Reset Pulse Width (6) TMR 150 ns (7) T<sub>E1</sub> Shift Clock Delay 125 ns (8) T<sub>E2</sub> Serial Data Setup 75 ns (9) TE3 (10) TE4 Serial Data Hold 75 ns A.C. Enable Setup 90 ns (11)T<sub>E5</sub> Enable Pulse Width 100 ns (12)TF6 Sync Setup 55 ns Sync Pulse Width (13)TE7 150 ns (14)TE8 Send Data Delay 0 50 ns (15)TE9 Bipolar Ouput Delay 130 ns (16)TE10 10 Enable Hold ns Sync Hold 95 (17)TE11 ns VCC = 5.0V ± 10% DECODER TIMING (18) F<sub>DC</sub> C<sub>L</sub> = 50pF Decoder Clock Frequency 0 15 MHz (19) FDS Decoder Sync Clock 2.5 MHz (20) TDCR Decoder Clock Rise Time ns (21)TDCF Decoder Clock Fall Time ns (22)FDD 1.25 MHz Data Rate (23)TDR (24)TDBS Decoder Reset Pulse Width 150 ns Decoder Reset Setup Time 75 ns (25)TDRH Decoder Reset Hold Time 10 ns (26)TMR Master Reset Pulse 150 ns (27)T<sub>D1</sub> Bipolar Data Pulse Width T<sub>DC</sub> +10 ns (Note 1) 18T<sub>DC</sub> (28)TD2 Sync Transition Span ns (Note 1) (29)T<sub>D3</sub> A.C. One Zero Overlap TDC -10 (Note 1) ns 6T<sub>DC</sub> Short Data Transition Span ns (Note 1) (30)TD4 (31)T<sub>D5</sub> Long Data Transition Span 12TDC ns (Note 1) (32)TD6 Sync Delay (ON) -20 110 ns Take Data Delay (ON) (33)TD7 0 110 ns (34)T<sub>D8</sub> Serial Data Out Delay 80 ns n Sync Delay (OFF) 110 (35)TD9 ns Take Data Delay (OFF) (36)T<sub>D10</sub> 0 110 ns (37)T<sub>D11</sub> Valid Word Delay 0 110 ns Sync Clock to Shift Clock Delay $(38)T_{D12}$ 75 ns (39)T<sub>D13</sub> Sync Data Setup NOTE 1. TDC = Decoder Clock Period = (These parameters are guaranteed but not 100% tested) FDC

### Specifications HD-15531B

### **Absolute Maximum Ratings**

 $\begin{array}{llll} \theta_{\rm ja} & 45^{\rm o}{\rm C/W} \; ({\rm CERDIP} \; {\rm package}), & 50^{\rm o}{\rm C/W} \; ({\rm LCC} \; {\rm package}) \\ {\rm Gate} \; & 456 \; {\rm Gates} \\ {\rm Junction} \; & 155^{\rm o}{\rm C} \\ {\rm Lead} \; {\rm Temperature} & 155^{\rm o}{\rm C} \\ {\rm Lead} \; {\rm Temperature} \; & 275^{\rm o}{\rm C} \\ \end{array}$ 

CAUTION: Stresses above those listed in the "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied.

### **Operating Conditions**

 Operating Voltage Range
 +4.5V to +5.5V

 Operating Temperature Range
 -40°C to +85°C

 HD-15531B-9
 -55°C to +125°C

### **Electrical Specifications** $T_A = -40^{\circ}\text{C} \text{ to } +85^{\circ}\text{C} \text{ (HD-15531B-9)}, T_A = -55^{\circ}\text{C} \text{ to } +125^{\circ}\text{C} \text{ (HD-15531B-2/-8)}$

ļ	SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS	TEST CONDITIONS	
	VIH VIL VIHC VILC	Logical "1" Input Voltage Logical "0" Input Voltage Logical "1" Input Voltage (Clock) Logical "0" Input Voltage (Clock) Input Leakage	70% V <sub>CC</sub> V <sub>CC</sub> -0.5 -1.0		20% VCC GND +0.5 +1.0	V V V μΑ	V <sub>IN</sub> = V <sub>CC</sub> or GND, DIP Pins 6-13, 15, 18, 19, 20, 22, 23, 26, 28-31, 33, 36, 37, 39, 40	
s.	VOH VOL ICCSB	Logical "1" Output Voltage Logical "0" Output Voltage Supply Current Standby	2.4	0.5	0.4 2.0	V V mA	I <sub>OH</sub> = -3mA I <sub>OL</sub> = 1.8mA V <sub>IN</sub> = V <sub>CC</sub> = 5.5V Outputs Open	
	CCOP C <sub>IN</sub>	Supply Current Operating* Input Capacitance		8.0 10	10.0	mA pF	V <sub>CC</sub> = 5.5V f = 15MHz All measurements are referenced to device	
	c <sub>0</sub>	Output Capacitance *Guaranteed	and sampled b	14 ut not 100%	tested	ρF	GND, T <sub>A</sub> = +25 <sup>0</sup> C, F = 1MHz	
l	ENCODER TIME	NG VCC = 5.0V ± 10%						
	(1) FEC (2) FESC (3) TECR	Encoder Clock Frequency Send Clock Frequency Encoder Clock Rise Time	0		30 5.0 8 8	MHz MHz ns	C <sub>L</sub> = 50pF	
	(4) TECF (5) FED (6) TMR	Encoder Clock Fall Time Data Rate Master Reset Pulse Width Shift Clock Delay	0 150		2.5	ns MHz ns ns		
;.	(7) TE1 (8) TE2 (9) TE3 (10) TE4 (11) TE5	Serial Data Setup Serial Data Hold Enable Setup Enable Pulse Width Sync Setup	50 50 90 100 55		30	ns ns ns ns		
	(12) TE6 (13) TE7 (14) TE8 (15) TE9 (16) TE10 (17) TE11	Sync Pulse Width Send Data Delay Bipolar Ouput Delay Enable Hold Sync Hold	150 0 10 95		50 130	ns ns ns ns		
		NG VCC = 5.0V ± 10%	1 33			113	<u> </u>	
				I	20	MUZ	C 50pE	
c.	(18)FDC (19)FDS (20)TDCR (21)TDCF (22)FDD (23)TDR (24)TDRS (25)TDRH (26)TMR (27)TD1 (28)TD2 (29)TD3 (30)TD4 (31)TD5 (32)TD6 (33)TD7 (34)TD8 (35)TD9 (36)TD10 (36)TD10 (37)TD11	Decoder Clock Frequency Decoder Sync Clock Decoder Sync Clock Decoder Clock Rise Time Decoder Clock Fall Time Data Rate Decoder Reset Pulse Width Decoder Reset Setup Time Decoder Reset Hold Time Master Reset Pulse Bipolar Data Pulse Width Sync Transition Span One Zero Overlap Short Data Transition Span Long Data Transition Span Long Data Transition Span Sync Delay (ON) Take Data Delay (ON) Serial Data Out Delay Sync Delay (OFF) Take Data Delay (OFF) Valid Word Delay	0 0 150 75 10 150 7 DC +10	18TDC 6TDC 12TDC	30 5.0 8 8 2.50 TDC -10	MHz MHz MHz ns	(Note 1) (Note 1) (Note 1) (Note 1) (Note 1) (Note 1)	
	(38)T <sub>D12</sub> (39)T <sub>D13</sub>	Sync Clock to Shift Clock Delay Sync Data Setup	75		75	ns ns		

# Pin Description

2 O VALID WORD 3 O TAKE DATA Decoder 1 TAKE DATA Decoder 2 TAKE DATA Decoder 3 O TAKE DATA Decoder 4 O TAKE DATA Decoder 5 O SERIAL DATA OUT 5 O SERIAL DATA OUT 6 I SYNCHRONOUS DATA 7 I SYNCHRONOUS DATA 8 LECT 8 O SYNCHRONOUS DATA 8 LECT 9 DATA SELECT 8 I SYNCHRONOUS DATA 9 LECODER CLOCK 9 I DECODER CLOCK 9 I DECODER CLOCK 9 I DECODER CLOCK 9 I DECODER SHIFT 1 SYNCHRONOUS CLOCK 9 I DECODER SHIFT 1 SYNCHRONOUS CLOCK SELECT 1 SYNCHRONOUS CLOCK 9 I DECODER CLOCK 1 DECODER SHIFT 2 DECODER SHIFT 2 DECODER SHIFT 2 DECODER SHIFT 2 DECODER SHIFT 3 I DECODER SHIFT 2 DECODER SHIFT 3 I DECODER SHIFT 3 DECODER SHIFT 3 DECODER SHIFT 4 DECODER SHIFT 5 DECODER SHIFT 6 DECODER SHIFT 7 DECODER SHIFT 8 DECODER	PIN NUMBER	TYPE	NAME	SECTION	DESCRIPTION
2   VALID WORD   O TAKE DATA	1		Vcc	Both	Positive supply pin A 0 1 pF decoupling capacitor from VCC (pin 1) to GROUND (pin 21) in
A communus, free nummy signal provided for host liming or data handing. When a vision call to take data	2	0	VALID WORD	Decoder	
present on the flux, finis signal will de synchronized to the incoming date and wiserscal to take data.  Decoder SERIAL DATA OUT Decoder SYNCHRONOUS DATA SELECT DATA SYNCHRONOUS DATA SELECT DATA SELECT SYNCHRONOUS DATA SELECT SYNCHRONOUS DATA SELECT SYNCHRONOUS DATA SELECT DATA SELECT SYNCHRONOUS CLOCK SELECT SYNCHRONOUS CLOC	3	0	TAKE DATA		
Decomposition   Serial Data Out   Decomposition   Decomposit				200000	present on the bus, this signal will be synchronized to the incoming data and will b
SYNCHRONOUS DATA   Decoder DATA	4	0	TAKE DATA	Decoder	Output is high during receipt of data after identification of a valid sync pulse and two valid Manchester bits.
DATA SELECT must be heldingh to use this imput. If not used this pile must be held in high sitter allows the synchronous data to enter the character identification logic. In in high sitter allows the synchronous data.  I SYNO-IRONOUS CLOCK  DECODER SHIFT  CLOCK  CLOCK  DECODER SHIFT  CLOCK  TRANSITION SELECT  DECODER SHIFT  CLOCK  DECODER SHIFT  DE	5	0	SERIAL DATA OUT	Decoder	Delivers received data in correct NRZ format.
DATA SELECT   Decoder	6	1		Decoder	Input presents Manchester data directly to character identification logic SYNCHRONOUS DATA SELECT must be held high to use this input. If not used this pin must be held high
CLOCK   DECODER CLOCK   Decoder	7	1		Decoder	In high state allows the synchronous data to enter the character identification logic. Tie thi input low for asynchronous data
SYNCHRONOUS   CLOCK SELECT   Decoder   In high state directs the SYNCHRONOUS CLOCK to control the decoder chain dentification logic A low state selects the DECODER CLOCK   Decoder   In high state directs the SYNCHRONOUS CLOCK to control the decoder chain identification logic A low state selects the DECODER CLOCK   Angh input should be applied when the bus is in its positive state. This pin must be help when the unpolar input is used.   With pin 11 mgh and pin 12 low, this pin enters unipolar data into the transition from the current if the unpolar input is used.   With pin 11 mgh and pin 12 low, this pin enters unipolar data into the transition from the current if the unpolar input is used.   With pin 11 mgh and pin 12 low, this pin enters unipolar data into the transition from the current if the unpolar input is used.   With pin 11 mgh and pin 12 low, this pin enters unipolar data into the transition from the unpolar input is used.   With pin 11 mgh and pin 12 low, this pin enters unipolar data into the transition from the unpolar input must be net low.   Output which delivers a frequency (DECODER CLOCK + 12) synchronous by recovered serial data stream.   A high input to this pin causes the transition finder to synchronous on transitions.   A high input to this pin causes the transition finder to synchronous on transitions.   A high input to this pin causes the transition finder to synchronous on transitions.   A high input to this pin causes the transition finder to synchronous on transitions.   A high input to this pin output causes the transition finder to synchronous on transitions.   A high input to this pin pin to causes the transition finder to synchronous on transitions.   A high input to this pin pin transitions.   A high input to this pin output data.   A high input to the pin pin transition finder to synchronous on transitions.   A high input to this pin output synchronous on transitions.   A high input to this pin for situate, which is a final pin pin the pin	8	I		Decoder	Input provides externally synchronized clock to the decoder, for use when receiving synchronous data. This input must be tied high when not in use
CLOCK SELECT   BIPOLAR ZERO IN   Decoder   A high input should be applied when the bus is in its negative state. This pin must be high when the unpolar input is used.   A high input should be applied when the bus is in its negative state. This pin must be high when the unpolar input is used.   A high input should be applied when the bus is in its negative state. This pin must be high when the unpolar input is used.   A high input should be applied when the bus is in its negative state. This pin must be high when the unpolar input is used.   With pin 11 nigh and pin 12 low, this pin enters unipolar data into the transition from the final time.   With pin 11 nigh and pin 12 low, this pin enters unipolar data into the transition finder to concern the pin of the	9	ł	DECODER CLOCK	Decoder	input drives the transition finder, and the synchronizer which in turn supplies the clock to the balance of the decoder. Input a frequency equal to 12X the data rate
high when the unipoter input is used A high input should be applied when the bus is in its positive state. This prin must be hele when the unipoter input is used. With pin 11 ingh and pin 12 low, this pin enters unipotar data into the transition for circuit. If not used this input must be neid low.  DECODER SHIFT CLOCK THANSITION SELECT THANSITION SELE	10	ı		Decoder	In high state directs the SYNCHRONOUS CLOCK to control the decoder characte identification logic. A low state selects the DECODER CLOCK.
when the unpolar input is used.  With pin 11 ingh and pin 12 low, this pin enters unipolar data into the transition for crown if indicated this input must be neid low  Obcoder SHIFT CLOCK TRANSITION SELECT  Decoder CLOCK  I TRANSITION SELECT  Decoder CLOCK  Blank  N C Blank  N C Blank  N C OOMMAND SYNC  Decoder Select An input to this pin causes the transition funder to synchronize on every transition input data. A low input causes the transition funder to synchronize on every transition input data. A low input causes the transition funder to synchronize on every transition input to this pin causes the transition funder to synchronize on every transition input to transition funder to synchronize on every transition input to transition funder to synchronize on every transition input to transition funder to synchronize on every transition input data. A low input causes the transition funder to synchronize on every transition input data. A low input causes the transition funder to synchronize on every transition input data. A low input causes the transition funder to synchronize on every transition input data. A low input causes the transition funder to synchronize on every transition input data. A low input causes the transition funder to synchronize on every transition input data. A low input causes the transition funder to synchronize on every transition input data. A low input data stream  A high input to this pin causes the transition funder to synchronize on every transition input data. A low input data stream input funder to synchronize on every transition input data. A low input data stream input funder to synchronize on every transition input funder to synchronize on every transition of the command lor status synchronize on every transition input to the funder transition funder to synchronize on every transition input funder to synchronize on every transition input to the funder funder funder to synchronize on every transition funder to synchronize on every transition funder to synchronize on every transi	11	1	BIPOLAR ZERO IN	Decoder	A high input should be applied when the bus is in its negative state. This pin must be heli- high when the unipolar input is used.
O DECODER SHIFT CLOCK  TRANSITION SELECT  Decoder  N C  Blank N C  Decoder  Decoder  N C  Decoder  N C  Decoder  Decoder  Decoder  N C  Decoder  De	12	1	BIPOLAR ONE IN	Decoder	A high input should be applied when the bus is in its positive state. This pin must be held low when the unipolar input is used.
recovered serial data stream.  A high input to this pin causes the transition finder to synchronize on every transition fundation.  N C Blank Not connected.  Output of a high from this pin occurs during output of decoded data which was preceded a Command (or Status) synchronizing character.  A high input to this pin occurs during output of decoded data which was preceded a Command (or Status) synchronizing character.  An input for parity sense, calling for even parity with input high and odd parity with 10w.  A high input to this pin during a rising edge of DECODER SHIFT CLOCK resets the decidence of the country of the binary inputs which establish the total bit count to be encoded or decoded a Command (or Status) synchronizing character.  COUNT Co Both NaSTER RESET Decoder or five binary inputs which establish the total bit count to be encoded or decoded and the property of the circuit.  COUNT Co Both Supply pin A high on his pin clears 2.1 counters in both encoder and decoder, and resets the circuit.  COUNT Co BIPOLAR ZERO OUT Encoder.  COUNT Co BIPOLAR ZERO OUT Encoder.  SERIAL DATA IN Encoder.  SERIAL DATA IN Encoder.  SERIAL DATA IN Encoder.  SERIAL DATA IN Encoder.  An active low output designed to drive the zero or negative sense of a bipolar line of A low on this pin forces pin 25 and 27 high, the inactive states.  An active low output designed to drive the one or positive sense of a bipolar line of A low on this pin initiates the encode cycle. (Subject to the preceding cycle bit complete.)  A high on this pin initiates the encode cycle. (Subject to the preceding cycle bit complete.)  A low on this pin initiates the encode cycle. (Subject to the preceding cycle bit complete.)  A low on this pin initiates the encoder cycle. (Subject to the preceding cycle bit complete.)  A low on this pin initiates the encoder cycle. (Subject to the preceding cycle bit cycle bits and cycle bits.  COUNT Co Both Cock IN Encoder.  Sets transmit parity odd for a hig	13	1	UNIPOLAR DATA IN	Decoder	With pin 11 high and pin 12 low, this pin enters unipolar data into the transition finde circuit. If not used this input must be held low.
input data. A low input causes the transition finder to synchronize only on mitransitions  N.C. Blank N.C. COMMAND SYNC. Decoder SELECT DECODER PARITY SELECT  19	14	0		Decoder	Output which delivers a frequency (DECODER CLOCK $\dot{\tau}$ 12) synchronous by th recovered serial data stream.
Output of a high number of this pin occurs during output of decoded data which was preceded a Command (or Status) synchronizing character  I DECODER RESET Decoder An input for parity sense, calling for even parity with input high and odd parity with low.  A high input to this pin during a rising edge of DECODER SHIFT CLOCK resets the decided output of the pin input to this pin during a rising edge of DECODER SHIFT CLOCK resets the decided output of the pin input to this pin during a rising edge of DECODER SHIFT CLOCK resets the decided output of the pin input to this pin during a rising edge of DECODER SHIFT CLOCK resets the decided output of the pin input to this pin during a rising edge of DECODER SHIFT CLOCK resets the decided output of the pin input to this pin during a rising edge of DECODER SHIFT CLOCK resets the decided output of the pin input to this pin of the pin input to the pin of the pin	15	i	TRANSITION SELECT	Decoder	A high input to this pin causes the transition finder to synchronize on every transition of input data. A low input causes the transition finder to synchronize only on mid-bit transitions
a Command (or Status) synchronizing character  An input for parity sense, calling for even parity with input high and odd parity within 1999. In DECODER RESET  Decoder Select  Decoder A high input to this pin during arising edge of DECODER SHIFT CLOCK resets the decont counting logic to a condition ready for a new word.  One of five binary inputs which establish the total bit count to be encoded or decoded and resets the circuit.  Decoder A high input to this pin during arising edge of DECODER SHIFT CLOCK resets the decont counting logic to a condition ready for a new word.  One of five binary inputs which establish the total bit count to be encoded or decoded and resets the circuit.  See pin 20.  COUNT C2 Both See pin 20.  Disposal TERO OUT County Inhibits  COUTPUT INHIBIT Encoder  An active low output designed to drive the zero or negative sense of a bipolar line of a high on this pin forces pin 25 and 27 high, the inactive states  Encoder An active low output designed to drive the one or positive sense of a bipolar line of a high on this pin initiates the encode cycle. (Subject to the preceding cycle by complete.)  SERIAL DATA IN Encoder Sets transmit parity odd for a high input even for a low input sets and a data rate equal to ENCODER SHIFT CLOCK in the Encoder Sets transmit parity odd for a high input even for a low input SELECT CLOCK in CLOCK	16		NC	Blank	Not connected.
SELECT   Decoder   A high input to this pin during a rising edge of DECODER SHIFT CLOCK resets the decoder of the counting logic to a condition ready for a new word.	17	0	COMMAND SYNC	Decoder	Output of a high from this pin occurs during output of decoded data which was preceded b a Command (or Status) synchronizing character
bit counting logic to a condition ready for a new word.  COUNT Co Both GROUND Both Both GROUND Both Both A righ on this pin clears 2.1 counters in both encoder and decoder, and resets the circuit.  COUNT Co Both A righ on this pin clears 2.1 counters in both encoder and decoder, and resets the circuit.  COUNT Co BIPOLAR ZERO OUT Encoder Encoder BIPOLAR ONE OUT Encoder BIPOLAR ONE OUT Encoder BIPOLAR ONE OUT Encoder Counters in both encoder and decoder, and resets the circuit.  COUTPUT INHIBIT Encoder BIPOLAR ONE OUT Encoder Counters in both encoder and decoder, and resets the circuit.  COUTPUT INHIBIT Encoder Counters in both encoder and decoder, and resets the circuit.  COUTPUT INHIBIT Encoder Counters in both encoder and decoder, and resets the circuit.  COUTPUT INHIBIT Encoder Counters in both encoder and decoder, and resets the circuit.  COUTPUT INHIBIT Encoder Counters in both encoder and decoder, and resets the circuit.  COUTPUT INHIBIT Encoder Counters in both encoder and decoder, and resets the circuit.  COUTPUT INHIBIT Encoder Counters in both encoder and decoder, and resets the circuit.  COUTPUT INHIBIT Encoder Counters in both encoder and decoder, and resets the circuit.  COUTPUT INHIBIT Encoder Counters in both encoder and decoder, and resets the circuit.  COUTPUT INHIBIT Encoder Counters in both encoder and decoder, and resets the circuit.  Counter inhibit pin clears 2.1 counters in both encoder and decoder, and resets the circuit.  Counter inhibit pin clears 2.1 counters in both encoder and decoder, and resets the circuit.  Counter inhibit pin or this pin clears 2.1 counters in both encoder and decoder, and resets the circuit.  Counter inhibit pin or this pin clears 2.1 counters in both encoder and decoder. A capture by the ENCODER CLOCK  A nactive low output designed to drive the zero or negative sense of a bipolar line of a low output designed to drive the zero or negative sense of a bipolar line of a low output designed to drive the zero or negative sense of a bipolar line of a low output desig	18	ı		Decoder	An input for parity sense, calling for even parity with input high and odd parity with inputow
GROUND   Both   Both   A nigh on this pin clears 2.1 counters in both encoder and decoder, and resets the circuit.	19	1	DECODER RESET	Decoder	A high input to this pin during a rising edge of DECODER SHIFT CLOCK resets the decode bit counting logic to a condition ready for a new word.
A nigh on this pin clears 2.1 counters in both encoder and decoder, and resets the circuit.  Both COUNT C2  Both See pin 20.  OUTPUT INHIBIT Encoder BIPOLAR ONE OUT SERIAL DATA IN Encoder ENCODER ENABLE Encoder BISYNC SELECT Encoder ENCODER PARITY SELECT  O SEND DATA Encoder Encoder SEND CLOCK IN Encoder Encoder COUNT C3  I SEND CLOCK IN Encoder En	20	-1	COUNT CO	Both	One of five binary inputs which establish the total bit count to be encoded or decoded.
CITCUIT.  COUNT C2  Both See pin 20.  OUTPUT INHIBIT  Fincoder Serial DATA IN Encoder Serial data stream at a data rate equal to ENCODER SHIFT CLOCATED COMPLET.  SYNC SELECT Encoder Sets transmit parity odd for a high input, even for a low input serial data.  SEND DATA Encoder Clock IN Encoder Clock IN C ENCODER SHIFT CLOCK  SEND DATA Encoder Clock IN Encoder Clock IN C ENCODER SHIFT CLOCK IN C Encoder Clock IN C Encoder Clock IN C Encoder Clock IN C Encoder Clock Input at a frequency equal to the data rate X2, usually driven by ÷ 6 output.  Set input to the 6:1 divider, a frequency equal to 12 times the data rate is usually input. Input of a data which was preceded a data synchronizing character.  COUNT C3 Encoder Clock IN See pin 20.  I COUNT C4 Both See pin 20  CITCUIT.  See pin 20.  Output from 6:1 divider which is driven by the ENCODER CLOCK  A nactive low output designed to drive the one or positive sense of a bipolar line of a clow output designed to drive the one or positive sense of a bipolar line of a clow output designed to drive the one or positive sense of a bipolar line of a clow output designed to drive the one or positive sense of a bipolar line of a clow output designed to drive the one or positive sense of a bipolar line of a clow output designed to drive the one or positive sense of a bipolar line of a clow output designed to drive the encoder or positive sense of a bipolar line of a clow output designed to drive the encoder of a complete in an active low output designed to drive the encoder of a clow output designed to drive the encoder of a clow output designed to drive the encoder of a clow output designed to drive the encoder of a clow output designed to drive the encoder of a clow output designed to drive the encoder of a clow output designed to drive the encoder of a clow output designed to drive the encoder of a clow output designed to drive the one or positive sense of a bipolar line of a clow output designed to drive the one or positive sense of a bipolar line of a clow output design	21		GROUND	Both	Supply pin
Output from 6:1 divider which is driven by the ENCODER CLOCK  BIPOLAR ZERO OUT  BIPOLAR ONE OUT  BIPOLAR ZERO OUT  An active low output designed to drive the one or positive sense of a bipolar line of a low on this pin forces pin 25 and 27 high, the inactive sense of a bipolar line of a low on this pin forces pin 25 and 27 high, the inactive sense of a bipolar line of a low on this pin forces pin 25 and 27 high, the inactive sense of a bipolar line of a low on this pin forces pin 25 and 27 high, the inactive sense of a bipolar line of a low on this pin forces pin 25 and 27 high, the inactive states  An active low output designed to drive the per or positive sense of a bipolar line of a low on this pin forces pin 25 and 27 high, the inactive states  An active low output designed to drive the per or positive sense of a bipolar line of a low on this pin forces pin 25 and 27 high, the inactive states  An active low output designed to drive the one or positive sense of a bipolar line of a low or or the sense of a bipolar line of a low or or the end of or positive sense of a bipolar line of a low or or the end of a bipolar line of a low or	22	ı	MASTER RESET	Both	A high on this pin clears 2.1 counters in both encoder and decoder, and resets the $\div$ circuit.
Description of Encoder Sensitive Sense of a bipolar line of the sense of a bipolar line of th	23	-1	COUNT C2	Both	See pin 20.
26   I OUTPUT INHIBIT   Encoder   A low on this pin forces pin 25 and 27 high, the inactive states   27   O BIPOLAR ONE OUT   Encoder   SERIAL DATA IN   Encoder   Encoder   Encoder   Encoder   Encoder   A high on this pin initiates the encode cycle. (Subject to the preceding cycle be complete.) 30   I SYNC SELECT   Encoder   Accepts a serial data stream at a data rate equal to ENCODER SHIFT CLC   A high on this pin initiates the encode cycle. (Subject to the preceding cycle be complete.) 31   I SYNC SELECT   Encoder   Actuates a Command sync for an input high and Data sync for an input low   Sets transmit parity odd for a high input, even for a low input   Is an active high output which enables the external source of serial data. 33   I SEND CLOCK IN   Encoder   Clock input at a frequency equal to the data rate X2, usually driven by ÷ 6 output. 34   O ENCODER SHIFT   Encoder   Clock input at a frequency equal to the data rate X2, usually driven by ÷ 6 output. 35   N C   Blank   Not connected   See pin 20. 36   I COUNT C3   Both   See pin 20. 37   I ENCODER CLOCK   Encoder   Cutput of a high from this pin occurs during output of decoded data which was preceded a data synchronizing character   See pin 20.	24	0	÷ 6 OUT	Encoder	Output from 6:1 divider which is driven by the ENCODER CLOCK
27 O BIPOLAR ONE OUT SERIAL DATA IN Encoder SERIAL DATA IN Encoder Complete.)  28 I SERIAL DATA IN Encoder ENCODER ENABLE Encoder A high on this pin initiates the encode cycle. (Subject to the preceding cycle browners)  30 I SYNC SELECT Encoder A command sync for an input high and Data sync for an input low SELECT Encoder Sets transmit parity odd for a high input, even for a low input Is an active night output which enables the external source of serial data.  31 I SEND CLOCK IN Encoder Clock input at a frequency equal to the data rate X2, usually driven by ÷ 6 output.  32 O SEND DATA Encoder Clock input at a frequency equal to the data rate X2, usually driven by ÷ 6 output.  33 I SEND CLOCK IN Encoder Clock input at a frequency equal to the Encoder samples SDI pin-28 or low-to-high transition of ESC.  34 O COUNT C3 Blank See pin 20.  35 I ENCODER CLOCK Encoder Couput of a high input to the 6.1 divider, a frequency equal to 12 times the data rate is usually input to the 6.1 divider, a frequency equal to 12 times the data rate is usually input to data synchronizing character.  39 II COUNT C4 Both See pin 20	25	0	BIPOLAR ZERO OUT	Encoder	An active low output designed to drive the zero or negative sense of a bipolar line driver
28 : SERIAL DATA IN 29   1 ENCODER ENABLE 29   1 ENCODER ENABLE 29   1 ENCODER ENABLE 29   1 ENCODER ENABLE 20   2 SYNC SELECT 30   30   1 ENCODER PARITY 31   1 ENCODER PARITY 32   COUNT C3   COUNT C3   COUNT C4   COUNT C5   COUNT C5   COUNT C6   COUNT C7   COUNT	26	1	OUTPUT INHIBIT	Encoder	A low on this pin forces pin 25 and 27 high, the inactive states
29   I ENCODER ENABLE   Encoder complete.) 30   I SYNC SELECT   Encoder Encoder Sets transmit parity odd for a high input, even for a low input set in put to the data rate X2, usually driven by ÷ 6 output. 31   SEND DATA   Encoder Send DATA   Encoder Clock input at a frequency equal to the data rate X2, usually driven by ÷ 6 output. 31   SEND CLOCK IN Encoder CLOCK   Encoder Clock input at a frequency equal to the data rate X2, usually driven by ÷ 6 output. 32   O SEND CLOCK IN Encoder Clock input at a frequency equal to the Encoder. The Encoder samples SDI pin-28 or low-to-high transition of ESC. 33   I COUNT C3   Both See pin 20. 34   O DATA SYNC   Decoder Cutput of a high input ceven for a low input sync for an input high and Data sync for an input low. 35   SEND DATA   Encoder Clock input at a frequency equal to the data rate X2, usually driven by ÷ 6 output. 36   I COUNT C3   Both See pin 20. 37   I ENCODER CLOCK   Encoder Clock input to the 6:1 divider, a frequency equal to 12 times the data rate is usually input inp	27	0	BIPOLAR ONE OUT	Encoder	An active low output designed to drive the one or positive sense of a bipolar line drive
complete.)  SYNC SELECT  Encoder Sets transmit parity odd for a high input, even for a low input set in put low sets transmit parity odd for a high input, even for a low input set input to the data rate X2, usually driven by ÷ 6 output.  SEND DATA Encoder Is an active nigh output which enables the external source of serial data.  SEND CLOCK IN Encoder Clock input at a frequency equal to the data rate X2, usually driven by ÷ 6 output.  SEND CLOCK Encoder Clock input at a frequency equal to the Encoder. The Encoder samples SDI pin-28 or low-to-high transition of ESC.  NC Blank Not connected  See pin 20.  DATA SYNC Decoder Cuptur of a high input cours during output of decoded data which was preceded a data synchronizing character.	28	1	SERIAL DATA IN	Encoder	Accepts a serial data stream at a data rate equal to ENCODER SHIFT CLOCK
31 I ENCODER PARITY SELECT 32 O SEND DATA Encoder Sets transmit parity odd for a high input, even for a low input 33 I SEND CLOCK IN Encoder Clock input at a frequency equal to the data rate X2, usually driven by ÷ 6 output. 34 O ENCODER SHIFT CLOCK 35 N C Blank Not connected 36 I COUNT C3 Both See pin 20. 37 I ENCODER CLOCK Encoder 38 O DATA SYNC Decoder 39 II COUNT C4 Both See pin 20	29	1	ENCODER ENABLE	Encoder	A high on this pin initiates the encode cycle, (Subject to the preceding cycle being complete.)
SELECT  SEND DATA  SEND CLOCK IN  SEND CLOCK IN  SEND CLOCK IN  CLOCK  N C  SEND CLOCK  Blank  Not connected  See pin 20.  DATA SYNC  DECOMPT C4  Both  COUNT C4  Both  See pin 20.  SELECT  Is an active high output which enables the external source of serial data.  Clock input at a frequency equal to the data rate X2, usually driven by ÷ 6 output.  Clock input at a frequency equal to the data rate X2, usually driven by ÷ 6 output.  Clock input at a frequency equal to the data rate X2, usually driven by ÷ 6 output.  Clock input at a frequency equal to the data rate X2, usually driven by ÷ 6 output.  See pin 20.  Blank  Not connected  See pin 20.  Input to the 6.1 divider, a frequency equal to 12 times the data rate is usually input I data synchronizing character  See pin 20.	30	1	SYNC SELECT	Encoder	Actuates a Command sync for an input high and Data sync for an input low
33 I SEND CLOCK IN Encoder Clock input at a frequency equal to the data rate X2, usually driven by ÷ 6 output.  34 O ENCODER SHIFT CLOCK  35 N C Blank Not connected  36 I COUNT C3  37 I ENCODER CLOCK  38 O DATA SYNC Decoder  39 I COUNT C4 Both See pin 20  39 I COUNT C4 Both See pin 20	31	1		Encoder	Sets transmit parity odd for a high input, even for a low input
O ENCODER SHIFT CLOCK  Standard Country Countr	32	0	SEND DATA	Encoder	Is an active high output which enables the external source of serial data.
O ENCODER SHIFT CLOCK  Standard Tourish Transition of ESC.  OUT TO Blank  O DATA SYNC  Decoder  Output for shifting data into the Encoder. The Encoder samples SDI pin-28 or low-to-high transition of ESC.  Not connected  See pin 20.  Data SYNC  Decoder  Output for shifting data into the Encoder. The Encoder samples SDI pin-28 or low-to-high transition of ESC.  Not connected  See pin 20.  The Encoder samples SDI pin-28 or low-to-high transition of ESC.  Not connected  See pin 20.  The Encoder samples SDI pin-28 or low-to-high transition of ESC.  Not connected  See pin 20.  The Encoder samples SDI pin-28 or low-to-high transition of ESC.  Not connected  See pin 20.  The Encoder samples SDI pin-28 or low-to-high transition of ESC.  Not connected  See pin 20.	33	1	SEND CLOCK IN	Encoder	Clock input at a frequency equal to the data rate X2, usually driven by $\div$ 6 output.
36 I COUNT C3 Both See pin 20. 37 I ENCODER CLOCK Encoder 38 O DATA SYNC Decoder Output of a high from this pin occurs during output of decoded data which was preceded a data synchronizing character 39 I COUNT C4 Both See pin 20.	34	0		Encoder	Output for shifting data into the Encoder. The Encoder samples SDI pin-28 on th low-to-high transition of ESC.
37 I ENCODER CLOCK Encoder Input to the 6.1 divider, a frequency equal to 12 times the data rate is usually input to 38 O DATA SYNC Decoder Output of a high from this plin occurs during output of decoded data which was preceded a data synchronizing character  39 I COUNT C4 Both See pin 20	35		N C	Blank	Not connected
38 C DATA SYNC Decoder Cutput of a high from this plin occurs during output of decoded data which was preceded a data synchronizing character  39 I COUNT C4 Both See pin 20	36	1	COUNT C3	Both	See pin 20.
38 C DATA SYNC Decoder Cutput of a high from this plin occurs during output of decoded data which was preceded a data synchronizing character  39 I COUNT C4 Both See pin 20	1	1			Input to the 6:1 divider, a frequency equal to 12 times the data rate is usually input here
	- 1	0			Output of a high from this pin occurs during output of decoded data which was preceded b
40 L COUNT C1 Roth See p.p. 20	39	1	COUNT C4	Both	See pin 20
TO I LOCUMENT DOME LOCE DINES	40	1 1	COUNT C1	Both	See pin 20

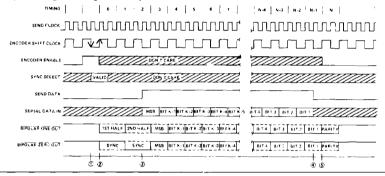
### **Encoder Operation**

The Encoder requires a single clock with a frequency of twice the desired data rate applied at the SEND CLOCK input. An auxiliary divide by six counter is provided on chip which can be utilized to produce the SEND CLOCK by dividing the DECODER CLOCK. The frame length is set by programming the COUNT inputs. Parity is selected by programming ENCODER PARITY SELECT high for odd parity or low for even parity.

The Encoder's cycle begins when ENCODER ENABLE is high during a falling edge of ENCODER SHIFT CLOCK ①. This cycle lasts for one word length or K + 4 ENCODER SHIFT CLOCK periods, where K is the number of bits to be sent. At the next low-to-high transition of the ENCODER SHIFT CLOCK, a high SYNC SELECT input actuates a Command sync or a low will produce a Data sync for the word ③. When the Encoder is ready to accept data, the SEND DATA output will go high for K ENCODER SHIFT CLOCK periods ④. During these K periods the

data should be clocked into the SERIAL DATA input with every high-to-low transition of the ENCODER SHIFT CLOCK ① - ④ so it can be sampled on the low-to-high transition. After the sync and Manchester II encoded data are transmitted through the BIPOLAR ONE and BIPOLAR ZERO outputs, the Encoder adds on an additional bit with the parity for that word ③. If ENCODER ENABLE is held high continuously, consecutive words will be encoded without an interframe gap. ENCODER ENABLE must go low by time ③ (as shown) to prevent a consecutive word from being encoded. At any time a low on OUTPUT INHIBIT input will force both bipolar outputs to a high state but will not affect the Encoder in any other way.

To abort the Encoder transmission a positive pulse must be applied at MASTER RESET. Any time after or during this pulse, a low-to-high transition on SEND CLOCK clears the internal counters and initializes the Encoder for a new word.



### **Decoder Operation**

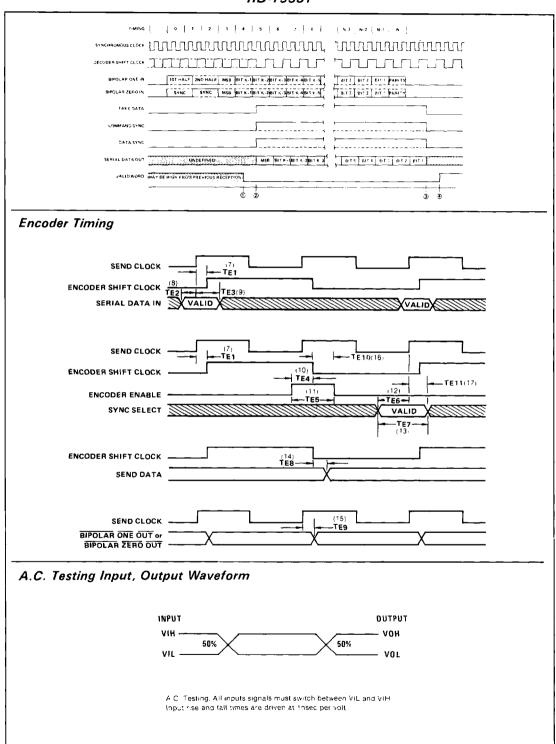
To operate the Decoder asynchronously requires a single clock with a frequency of 12 times the desired data rate applied at the DECODER CLOCK input. To operate the Decoder synchronously requires a SYNCHRONOUS CLOCK at a frequency 2 times the data rate which is synchronized with the data at every high-to-low transition applied to the SYNCHRONOUS CLK input. The Manchester II coded data can be presented to the Decoder asynchronously in one of two ways. The BIPOLAR ONE and BIPOLAR ZERO inputs will accept data from a comparator sensed transformer coupled bus as specified in Military Spec 1553. The UNIPOLAR DATA input can only accept noninverted Manchester II coded data. (e.g. from BIPOLAR ONE OUT on an Encoder through an inverter to Unipolar Data Input).

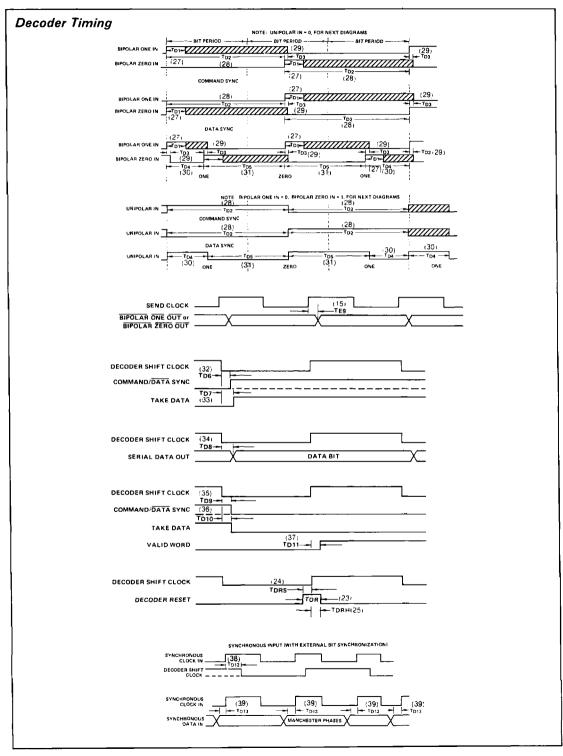
The Decoder is free running and continuously monitors its data input lines for a valid sync character and two valid Manchester data bits to start an output cycle. When a valid sync is recognized ①, the type of sync is indicated by a high level at either COMMAND SYNC or DATA SYNC output. If the sync character was a command sync the COMMAND SYNC output will go high ② and remain high for K SHIFT CLOCK periods ①, where K is the number of bits to be received. If the sync character was a data sync the DATA SYNC output will go high. The TAKE DATA

output will go high and remain high ② - ③ while the Decoder is transmitting the decoded data through SERIAL DATA OUT. The decoded data available at SERIAL DATA OUT is in NRZ format. The DECODER SHIFT CLOCK is provided so that the decoded bits can get shifted into an external register on every low-to-high transition of this clock ② - ③. Note that DECODER SHIFT CLOCK may adjust its phase up until the time that TAKE DATA goes high.

After all K decoded bits have been transmitted ③ the data is checked for parity. A high input on DECODER PARITY SELECT will set the Decoder to check for even parity or a low input will set the Decoder to check for odd parity. A high on VALID WORD output ④ indicates a successful reception of a word without any Manchester or parity errors. At this time the Decoder is looking for a new sync character to start another output sequence. VALID WORD will go low approximately K + 4 DECODER SHIFT CLOCK periods after it goes high if not reset low sooner by a valid sync and two valid Manchester bits as shown ①.

At any time in the above sequence a high input on DECODER RESET during a low-to-high transition of DECODER SHIFT CLOCK will abort transmission and initialize the Decoder to start looking for a new sync character.





Frame Counter

	FRAME LENGTH	PIN WORD						
DATA BITS	(BIT PERIODS)	C <sub>4</sub>	C <sub>3</sub>	C <sub>2</sub>	C <sub>1</sub>	C <sub>0</sub>		
2	6	L	L	I	L	н		
2 3	7	L	L	н	н	L		
4	8	L	L	н	Ħ	н		
5	9	L	н	L	L	L		
6	10	L .	н	L	L	н		
7	11	L	н	L	Н	L		
8	12	L	H	L	Н	н		
9	13	L	н	н	L	L		
10	14	L	н	н	L	Н		
11	15	L	l H	н	H	L		
12	16	L	Н	н	н	н		
13	17	H	L	L	L	L		
14	18	н	L	L	L	н		
15	19	H	L	L	н	L		

	FRAME LENGTH (BIT PERIODS)	PIN WORD						
DATA BITS		C4	C <sub>3</sub>	C <sub>2</sub>	C <sub>1</sub>	C <sub>0</sub>		
16 17 18 19 20 21 22 23 24 25 26 27 28	20 21 22 23 24 25 26 27 28 29 30 31					H		

The above Table demonstrates all possible combinations of frame lengths ranging from 6 to 32 bits. The pin word described here is common to both the Encoder and Decoder.

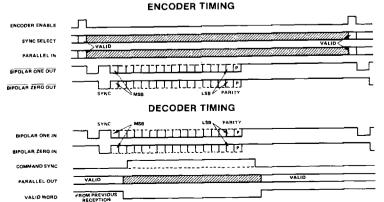
# How to Make Our MTU Look Like a Manchester Encoded UART Value word SYNC GALA SYNC GALA SYNC GALA BEGGAR GEORGE GEORG

74164

PARALLEL OUT

74164

Typical Timing Diagram for a Manchester Encoded UART



### MIL-STD-1553

The 1553 standard defines a time division multiplexed data bus for application within aircraft. The bus is defined to be bipolar, and encoded in a Manchester II format, so no DC component appears on the bus. This allows transformer coupling and excellent isolation among systems and their environment.

The HD-15531 supports the full bipolar configuration, assuming a bus driver configuration similar to that in Figure 1. Bipolar inputs from the bus, like Figure 2, are also accommodated.

The signaling format in MIL-STD-1553 is specified on the assumption that the network of 32 or fewer terminals are controlled by a central control unit by means of Command Words, and Data. Terminals respond with Status Words, and Data. Each word is preceded by a

synchronizing pulse, and followed by parity bit, occupying a total of  $20\mu$  sec. The word formats are shown in Figure 4. The special abbreviations are as follows:

- P Parity, which is defined to be odd, taken across all 17 bits.
- R/T Receive on logical zero, transmit on ONE.
- ME Message Error if logical 1.
- TF Terminal Flag, if set, calls for controller to request self-test data.

The paragraphs above are intended only to suggest the content of MIL-STD-1553, and do not completely describe its bus requirements, timing or protocols.

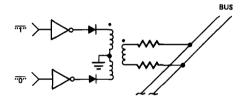


FIGURE 1. SIMPLIFIED MIL-STD-1553 DRIVER

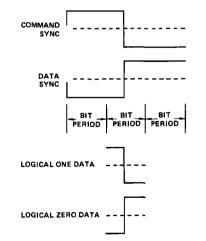


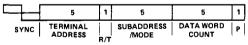
FIGURE 3. MIL-STD-1553 CHARACTER FORMATS

"1" REF
"0" REF

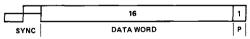
FIGURE 2, SIMPLIFIED MIL-STD-1553 RECEIVER

0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19

COMMAND WORD (FROM CONTROLLER TO TERMINAL)



DATA WORD (SENT EITHER DIRECTION)



STATUS WORD (FROM TERMINAL TO CONTROLLER)

	5	1	9	1	1
SYNC	TERMINAL ADDRESS	ME	CODE FOR FAILURE MODES	TF	P

FIGURE 4. MIL-STD-1553 WORD FORMATS

NOTE: This page is a summary of MIL-STD-1553 and is not intended to describe the operation of the HD-15531