4.0 Electrical Specifications

Electrical specifications in this chapter are valid for both the BL486DX and the clock-doubled BL486DX2. The BL486DX2 differs from the BL486DX in that the BL486DX2 internal CPU core operates at twice the frequency of the bus interface.

4.1 Electrical Connections

4.1.1 Power and Ground Connections and Decoupling

Due to the high frequency of operation of the BL486DX/DX2, it is necessary to install and test this device using standard high frequency techniques. The high clock frequencies used in the BL486DX/DX2 and its output buffer circuits can cause transient power surges when several output buffers switch output levels simultaneously. These effects can be minimized by filtering the DC power leads with low-inductance decoupling capacitors, using low impedance wiring, and by utilizing all of the V_{CC} and GND pins.

4.1.2 Pull-Up/Pull-Down Resisters

Table 4-1 lists the input pins which are internally connected to pull-up and pull-down resistors. The pull-up resistors are connected to V_{CC} and the pull-down resistors are connected to V_{SS}. When unused, these inputs do not require connection to external pull-up or pull-down resistors. The SUSP# pin is unique in that it is connected to a pull-up resistor only when SUSP# is not asserted.

Table 4-1. Pins Connected to Internal Pull-Up and Pull-Down Resistors

SIGNAL	RESISTOR
A20M#	20-kΩ pull-up
AHOLD	20-kΩ pull-down
BOFF#	20-kΩ pull-up
BS16#	20-kΩ pull-up
BS8#	20-kΩ pull-up
BRDY#	20-kΩ pull-up
EADS#	20-kΩ pull-up
FLUSH#	20-kΩ pull-up
IGNNE#	20-kΩ pull-up
INVAL	20-kΩ pull-up
KEN#	20-kΩ pull-up
RDY#	20-kΩ pull-up
UP#	20-kΩ pull-up
SUSP#	20-kΩ pull-up
WM_RST	20-kΩ pull-down

It is recommended that the ADS#, LOCK# and SMI# output pins be connected to pull-up resistors, as indicated in Table 4-2. The external pull-ups guarantee that the signals remain negated during hold acknowledge states.

Table 4-2. Pins Requiring External Pull-Up Resistors

SIGNAL	EXTERNAL RESISTOR
ADS#	20-kΩ pull-up
LOCK#	20-kΩ pull-up
SMI#	20-kΩ pull-up

4.1.3 Unused Input Pins

All inputs not used by the system designer and not listed in Table 4-1 should be connected either to ground or to V_{CC}. Connect active-high inputs to ground through a 20 kΩ (± 10%) pull-down resistor and active-low inputs to V_{CC} through a 20 kΩ (± 10%) pull-up resistor to prevent possible spurious operation.

4.1.4 NC Designated Pins

Pins designated NC should be left disconnected. Connecting an NC pin to a pull-up resistor, pull-down resistor, or an active signal could cause unexpected results and possible circuit malfunctions.

4.2 Absolute Maximum Ratings

The following table lists absolute maximum ratings for the BL486DX/DX2 microprocessors. Stresses beyond those listed under Table 4-3 limits may cause permanent damage to the device. These are stress ratings only and do not imply that operation under any conditions other than those listed under "Recommended Operating Conditions" Table 4-4 is possible. Exposure to conditions beyond Table 4-3 may (1) reduce device reliability and (2) result in premature failure even when there is no immediately apparent sign of failure. Prolonged exposure to conditions at or near the absolute maximum ratings (Table 4-3) may also result in reduced useful life and reliability.

Table 4-3. Absolute Maximum Ratings

PARAMETER	BL486DX/DX2		BL486DX/DX2-V		UNITS	NOTES
	MIN	MAX	MIN	MAX		
Case Temperature	-65°	+110°	-65°	+110°	C	Power Applied
Storage Temperature	-65°	+150°	-65°	+150°	C	No Bias
Supply Voltage, V_{CC}	-0.5	6.5	-0.5	4.0	V	With Respect to V_{SS}
Voltage On Any Pin	-0.5	V_{CC} + 0.5	-0.5	6.0*	V	With Respect to V_{SS}
Input Clamp Current, I_{IK}		10		10	mA	Power Applied
Output Clamp Current, I_{OK}		25		25	mA	Power Applied

*Note: The maximum "Voltage On Any Pin" for BL486DX/DX2-V devices with a stepping ID of 0xh is V_{CC}+0.5 volts; for devices with stepping IDs of 1xh and above the maximum voltage is 6.0 volts, as shown. (The stepping ID for a BL486DX/DX2-V CPU can be found by reading the DIR1 configuration register.)

4.3 Recommended Operating Conditions

Table 4-4 presents the recommended operating conditions for the BL486DX/DX2 device.

Table 4-4. Recommended Operating Conditions

PARAMETER	BL486DX/DX2		BL486DX/DX2-V		UNITS	NOTES
	MIN	MAX	MIN	MAX		
T_C Case Temperature	0°	+85°	0°	+85°	C	Power Applied
V_{CC} Supply Voltage	4.75	5.25	3.0	3.6	V	With Respect to V_{ss}
V_{IH} High Level Input	2.0	V_{CC}+0.3	2.0	5.5	V	See note.
V_{IL} Low Level Input	-0.3	0.8	-0.3	0.6	V	
I_{OH} Output Current (High)		-1.0		-1.0	mA	$V_{OH}=V_{OH(MIN)}$
I_{OL} Output Current (Low)		5.0		3.0	mA	$V_{OL}=V_{OL(MAX)}$

Note: VIH specification shown for the BL486DX/DX2-V applies to devices with stepping IDs of 1xh and greater (DIR1 configuration register). BL486DX/DX2-V devices with a stepping ID of 0xh require a VIH(max) = V_{CC}+0.3 volts.

4.4 DC Characteristics

Table 4-5. DC Characteristics (at Recommended Operating Conditions)

PARAMETER	BL486DX/DX2		BL486DX/DX2-V		UNITS	NOTES
	MIN	MAX	MIN	MAX		
V_{OL} Output Low Voltage I_{OL} = 5 mA		0.45		0.35	V	
V_{OH} Output High Voltage I_{OH} = -1 mA	2.4		2.4		V	
I_{LI} Input Leakage Current For all pins except those listed in Table 4-1.		±15		±15	µA	$0 < V_{IN} < V_{CC}$
I_{IH} Input Leakage Current For all pins with internal pull-downs.		200		200	µA	V_{IH} = 2.4 V See Table 4-1
I_{IL} Input Leakage Current For all pins with internal pull-ups.		-400		-400	µA	V_{IL} = 0.45 V See Table 4-1
I_{CC} Active I_{CC}	Typical:		Typical:			Note 1
33 MHz	610	925	420	640	mA	
40 MHz	685	1025	450	680		
50 MHz	765	1170	495	750		
66 MHz	860	1325	560	850		
80 MHz			630	950		
I_{CCSM} Suspend Mode I_{CC}	Typical:		Typical:			Note 1, 3
33 MHz	12.5	24.5	9	20	mA	
40 MHz	13.5	27	10	23		
50 MHz	15.5	31	12	26		
66 MHz	18	35	14	30		
80 MHz			16	34		
I_{CCSS} Standby I_{CC}	Typical:		Typical:			
0 MHz (Suspended/CLK Stopped)	0.45	1.1	0.45	1.1	mA	Note 4
C_{IN} Input Capacitance		20		20	pF	fc = 1 MHz (Note 2)
C_{OUT} Output or I/O Capacitance		20		20	pF	fc = 1 MHz (Note 2)
C_{CLK} CLK Capacitance		20		20	pF	fc = 1 MHz (Note 2)

Notes:

1. MHz ratings refer to internal clock frequency.
2. Not 100% tested.
3. All inputs at 0.4 or V_{CC} - 0.4 (CMOS levels). All inputs held static except clock and all outputs unloaded (static I_{OUT} = 0 mA). Specification also valid for UP# = 0.
4. All inputs at 0.4 or V_{CC} - 0.4 (CMOS levels). All inputs held static and all outputs unloaded (static I_{OUT} = 0 mA).

4.5 AC Characteristics

Table 4-7 through 4-12 (Pages 4-7 through 4-12) list the AC characteristics including output delays, input setup requirements, input hold requirements and output float delays. These measurements are based on the measurement points identified in Figure 4-1 (Page 4-6) and Figure 4-2 (Page 4-6). The rising clock edge reference level V_{REF} and other reference levels are shown in Table 4-6 below for the BL486DX/DX2. Input or output signals must cross these levels during testing.

Figure 4-1 (Page 4-6) shows output delay (A and B) and input setup and hold times (C and D). Input setup and hold times (C and D) are specified minimums, defining the smallest acceptable sampling window a synchronous input signal must be stable for correct operation.

Table 4-6. Drive Level and Measurement Points for Switching Characteristics

SYMBOL	BL486DX/DX2	BL486DX/DX2-V	UNITS
V_{REF}	1.5	1.5	V
V_{IHD}	3	2.3	V
V_{ILD}	0	0	V

Note: Refer to Figure 4-1.

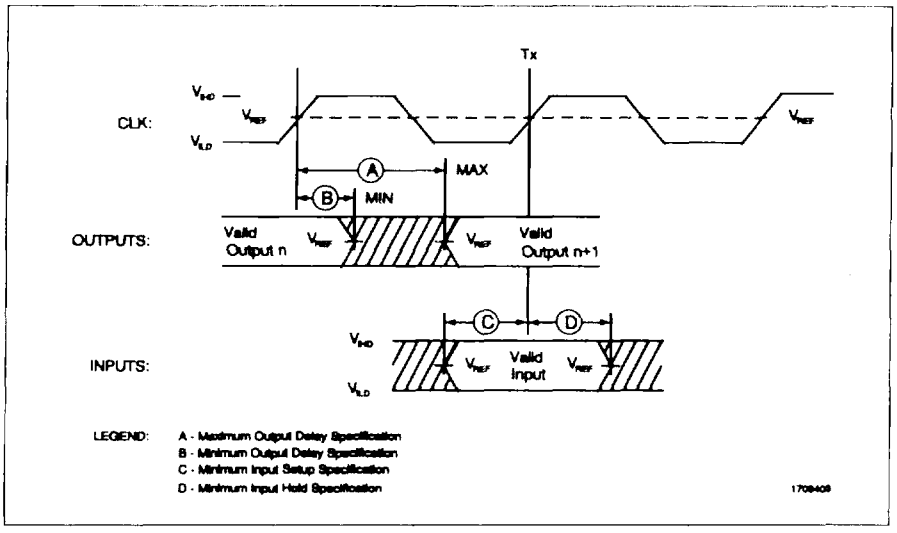

Figure 4-1. Drive Level and Measurement Points for Switching Characteristics

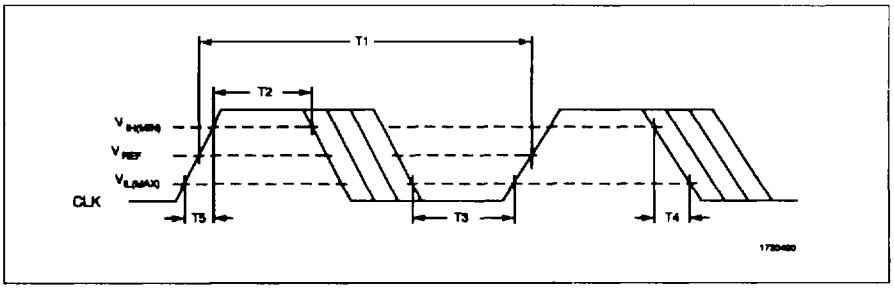

Figure 4-2. CLK Timing Measurement Points

Table 4-7. AC Characteristics for BL486DX2-50
V_{CC} = 5.0 V ±5%, T_{CASE} = 0° to 85° C, C_L = 50pF
External CLK = 25 MHz (Max.)

SYMBOL	PARAMETERS	MIN (ns)	MAX (ns)	FIGURE	NOTES
T1	CLK Period	40		4-2	
T2	CLK High Time	14		4-2	At 2 V
T3	CLK Low Time	14		4-2	$V_{IL(MAX)}$
T4	CLK Fall Time		4	4-2	2 V to $V_{IL(MAX)}$
T5	CLK Rise Time		4	4-2	$V_{IL(MAX)}$ to 2 V
T6	A31-A2, ADS#, BE3#-BE0#, BREQ, D/C#, HLDA, FERR#, LOCK#, M/IO#, PCD, PWT, W/R# Valid Delay	3	19	4-6	
T6a	SMADS#, SMI# Valid Delay	3	19	4-6	
T7	A31-A2, ADS#, BE3#-BE0#, BREQ, D/C#, HLDA, LOCK#, M/IO#, PCD, PWT, W/R# Float Delay		28	4-7	Note 1
T7a	SMADS#, SMI# Float Delay		28	4-7	Note 1
T8	PCHK# Valid Delay	3	24	4-5	
T8a	BLAST#, PLOCK# Valid Delay	3	24	4-6	
T8b	HITM#, RPLSET(1-0), RPLVAL#, SUSPA# Valid Delay	3	24	4-6	
T9	BLAST#, PLOCK# Float Delay		28	4-7	Note 1
T9a	RPLSET(1-0), RPLVAL# Float Delay		28	4-7	Note 1
T10	D31-D0, DP3-DP0 Write Data Valid Delay	3	20	4-6	
T11	D31-D0, DP3-DP0 Write Data Float Delay		28	4-7	Note 1
T12	EADS# Setup Time	8		4-3	
T12a	INVAL Setup Time	8		4-3	
T13	EADS# Hold Time	3		4-3	
T13a	INVAL Hold Time	3		4-3	
T14	BS16#, BS8#, KEN# Setup Time	8		4-3	
T15	BS16#, BS8#, KEN# Hold Time	3		4-3	
T16	BRDY#, RDY# Setup Time	8		4-4	
T17	BRDY#, RDY# Hold Time	3		4-4	
T18	AHOLD, HOLD Setup Time	10		4-3	
T18a	BOFF# Setup Time	10		4-3	
T19	AHOLD, BOFF#, HOLD Hold Time	3		4-3	
T20	A20M#, FLUSH#, IGNNE#, INTR, NMI, RESET Setup Time	10		4-3	
T20a	SMI#, SUSP#, WM_RST Setup Time	10		4-3	
T21	A20M#, FLUSH#, INTR, IGNNE#, NMI, RESET Hold Time	3		4-3	
T21a	SMI#, SUSP#, WM_RST Hold Time	3		4-3	
T22	A31-A4, D31-D0, DP3-DP0 Read Setup Time	5		4-3, 4-4	
T23	A31-A4, D31-D0, DP3-DP0 Read Hold Time	3		4-3, 4-4	

Note 1: Not 100% tested

Table 4-8. AC Characteristics for BL486DX-33, BL486DX2-66
V_{CC} = 5.0 V ±5%, T_{CASE} = 0° to 85° C, C_L = 50pF
External CLK = 33 MHz (Max.)

SYMBOL	PARAMETERS	MIN (ns)	MAX (ns)	FIGURE	NOTES
T1	CLK Period	30		4-2	
T2	CLK High Time	11		4-2	At 2 V
T3	CLK Low Time	11		4-2	$V_{IL(MAX)}$
T4	CLK Fall Time		3	4-2	2 V to $V_{IL(MAX)}$
T5	CLK Rise Time		3	4-2	$V_{IL(MAX)}$ to 2 V
T6	A31-A2, ADS#, BE3#-BE0#, BREQ, D/C#, FERR#, HLDA, LOCK#, M/IO#, PCD, PWT, W/R# Valid Delay	3	16	4-6	
T6a	SMADS#, SMI# Valid Delay	3	16	4-6	
T7	A31-A2, ADS#, BE3#-BE0#, BREQ, D/C#, HLDA, LOCK#, M/IO#, PCD, PWT, W/R# Float Delay		20	4-7	Note 1
T7a	SMADS#, SMI# Float Delay		20	4-7	Note 1
T8	PCHK# Valid Delay	3	22	4-5	
T8a	BLAST#, PLOCK# Valid Delay	3	20	4-6	
T8b	HITM#, RPLSET(1-0), RPLVAL#, SUSPA# Valid Delay	3	20	4-6	
T9	BLAST#, PLOCK# Float Delay		20	4-7	Note 1
T9a	RPLSET(1-0), RPLVAL# Float Delay		20	4-7	Note 1
T10	D31-D0, DP3-DP0 Write Data Valid Delay	3	18	4-6	
T11	D31-D0, DP3-DP0 Write Data Float Delay		20	4-7	Note 1
T12	EADS# Setup Time	5		4-3	
T12a	INVAL Setup Time	5		4-3	
T13	EADS# Hold Time	3		4-3	
T13a	INVAL Hold Time	3		4-3	
T14	BS16#, BS8#, KEN# Setup Time	5		4-3	
T15	BS16#, BS8#, KEN# Hold Time	3		4-3	
T16	BRDY#, RDY# Setup Time	5		4-4	
T17	BRDY#, RDY# Hold Time	3		4-4	
T18	AHOLD, HOLD Setup Time	6		4-3	
T18a	BOFF# Setup Time	8		4-3	
T19	AHOLD, BOFF#, HOLD Hold Time	3		4-3	
T20	A20M#, FLUSH#, IGNNE#, INTR, NMI, RESET Setup Time	5		4-3	
T20a	SMI#, SUSP#, WM_RST Setup Time	5		4-3	
T21	A20M#, FLUSH#, IGNNE#, INTR, NMI, RESET Hold Time	3		4-3	
T21a	SMI#, SUSP#, WM_RST Hold Time	3		4-3	
T22	A31-A4, D31-D0, DP3-DP0 Read Setup Time	5		4-3, 4-4	
T23	A31-A4, D31-D0, DP3-DP0 Read Hold Time	3		4-3, 4-4	

Note 1: Not 100% tested.

Table 4-9. AC Characteristics for BL486DX-40
V_{CC} = 5.0 V ±5%, T_{CASE} = 0° to 85° C, C_L = 50pF
External CLK = 40 MHz (Max.)

SYMBOL	PARAMETERS	MIN (ns)	MAX (ns)	FIGURE	NOTES
T1	CLK Period	25		4-2	
T2	CLK High Time	9		4-2	At 2 V
T3	CLK Low Time	9		4-2	$V_{IL(MAX)}$
T4	CLK Fall Time		3	4-2	2 V to $V_{IL(MAX)}$
T5	CLK Rise Time		3	4-2	$V_{IL(MAX)}$ to 2 V
T6	A31-A2, ADS#, BE3#-BE0#, BREQ, D/C#, FERR#, HLDA, LOCK#, M/IO#, PCD, PWT, W/R# Valid Delay	3	14	4-6	
T6a	SMADS#, SMI# Valid Delay	3	14	4-6	
T7	A31-A2, ADS#, BE3#-BE0#, BREQ, D/C#, FERR#, HLDA, LOCK#, M/IO#, PCD, PWT, W/R# Float Delay		19	4-7	Note 1
T7a	SMADS#, SMI# Float Delay		19	4-7	Note 1
T8	PCHK# Valid Delay	3	18	4-5	
T8a	BLAST#, PLOCK# Valid Delay	3	16	4-6	
T8b	HITM#, RPLSET(1-0), RPLVAL#, SUSPA# Valid Delay	3	16	4-6	
T9	BLAST#, PLOCK# Float Delay		19	4-7	Note 1
T9a	RPLSET(1-0), RPLVAL# Float Delay		19	4-7	Note 1
T10	D31-D0, DP3-DP0 Write Data Valid Delay	3	16	4-6	
T11	D31-D0, DP3-DP0 Write Data Float Delay		19	4-7	Note 1
T12	EADS# Setup Time	5		4-3	
T12a	INVAL Setup Time	5		4-3	
T13	EADS# Hold Time	3		4-3	
T13a	INVAL Hold Time	3		4-3	
T14	BS16#, BS8#, KEN# Setup Time	5		4-3	
T15	BS16#, BS8#, KEN# Hold Time	3		4-3	
T16	BRDY#, RDY# Setup Time	5		4-4	
T17	BRDY#, RDY# Hold Time	3		4-4	
T18	AHOLD, HOLD Setup Time	5		4-3	
T18a	BOFF# Setup Time	6		4-3	
T19	AHOLD, BOFF#, HOLD Hold Time	3		4-3	
T20	A20M#, FLUSH#, IGNNE#, INTR, NMI, RESET Setup Time	5		4-3	
T20a	SMI#, SUSP#, WM_RST Setup Time	5		4-3	
T21	A20M#, FLUSH#, IGNNE#, INTR, NMI, RESET Hold Time	3		4-3	
T21a	SMI#, SUSP#, WM_RST Hold Time	3		4-3	
T22	A31-A4, D31-D0, DP3-DP0 Read Setup Time	5		4-3, 4-4	
T23	A31-A4, D31-D0, DP3-DP0 Read Hold Time	3		4-3, 4-4	

Note 1 Not 100% tested.

Table 4-10. AC Characteristics for BL486DX-50
V_{CC} = 5.0 V ± 5%, T_{CASE} = 0° to 85° C, C_L = 50pF
External CLK = 50 MHz (Max.)

SYMBOL	PARAMETERS	MIN (ns)	MAX (ns)	FIGURE	NOTES
T1	CLK Period	20		4-2	
T2	CLK High Time	7		4-2	At 2 V
T3	CLK Low Time	7		4-2	$V_{IL(MAX)}$
T4	CLK Fall Time		2	4-2	2 V to $V_{IL(MAX)}$
T5	CLK Rise Time		2	4-2	$V_{IL(MAX)}$ to 2 V
T6	A31-A2, ADS#, BE3#-BE0#, BREQ, D/C#, FERR#, HLDA, LOCK#, M/IO#, PCD, PWT, W/R# Valid Delay	3	12	4-6	
T6a	SMADS#, SMI# Valid Delay	3	12	4-6	
T7	A31-A2, ADS#, BE3#-BE0#, BREQ, D/C#, HLDA, LOCK#, M/IO#, PCD, PWT, W/R# Float Delay		18	4-7	Note 1
T7a	SMADS#, SMI# Float Delay		18	4-7	Note 1
T8	PCHK# Valid Delay	3	14	4-5	
T8a	BLAST#, PLOCK# Valid Delay	3	12	4-6	
T8b	HITM#, RPLSET(1-0), RPLVAL#, SUSPA# Valid Delay	3	14	4-6	
T9	BLAST#, PLOCK# Float Delay		18	4-7	Note 1
T9a	RPLSET(1-0), RPLVAL# Float Delay		18	4-7	Note 1
T10	D31-D0, DP3-DP0 Write Data Valid Delay	3	12	4-6	
T11	D31-D0, DP3-DP0 Write Data Float Delay		18	4-7	Note 1
T12	EADS# Setup Time	5		4-3	
T12a	INVAL Setup Time	5		4-3	
T13	EADS# Hold Time	2		4-3	
T13a	INVAL Hold Time	2		4-3	
T14	BS16#, BS8#, KEN# Setup Time	5		4-3	
T15	BS16#, BS8#, KEN# Hold Time	2		4-3	
T16	BRDY#, RDY# Setup Time	5		4-4	
T17	BRDY#, RDY# Hold Time	2		4-4	
T18	AHOLD, HOLD Setup Time	5		4-3	
T18a	BOFF# Setup Time	5		4-3	
T19	AHOLD, BOFF#, HOLD Hold Time	2		4-3	
T20	A20M#, FLUSH#, IGNNE#, INTR, NMI, RESET Setup Time	5		4-3	
T20a	SMI#, SUSP#, WM_RST Setup Time	5		4-3	
T21	A20M#, FLUSH#, IGNNE#, INTR, NMI, RESET Hold Time	2		4-3	
T21a	SMI#, SUSP#, WM_RST Hold Time	2		4-3	
T22	A31-A4, D31-D0, DP3-DP0 Read Setup Time	4		4-3, 4-4	
T23	A31-A4, D31-D0, DP3-DP0 Read Hold Time	2		4-3, 4-4	

Note 1: Not 100% tested.

Table 4-11. AC Characteristics for BL486DX2-V50
V_{CC} = 3.0 to 3.6 V, T_{CASE} = 0° to 85° C, C_L = 50pF
External CLK = 25 MHz (Max.)

SYMBOL	PARAMETERS	MIN (ns)	MAX (ns)	FIGURE	NOTES
T1	CLK Period	40		4-2	
T2	CLK High Time	14		4-2	At 2 V
T3	CLK Low Time	14		4-2	$V_{IL(MAX)}$
T4	CLK Fall Time		4	4-2	2 V to $V_{IL(MAX)}$
T5	CLK Rise Time		4	4-2	$V_{IL(MAX)}$ to 2 V
T6	A31-A2, ADS#, BE3#-BE0#, BREQ, D/C#, HLDA, FERR#, LOCK#, M/IO#, PCD, PWT, W/R# Valid Delay	3	19	4-6	
T6a	SMADS#, SMI# Valid Delay	3	19	4-6	
T7	A31-A2, ADS#, BE3#-BE0#, BREQ, D/C#, HLDA, LOCK#, M/IO#, PCD, PWT, W/R# Float Delay		28	4-7	Note 1
T7a	SMADS#, SMI# Float Delay		28	4-7	Note 1
T8	PCHK# Valid Delay	3	24	4-5	
T8a	BLAST#, PLOCK# Valid Delay	3	24	4-6	
T8b	HITM#, RPLSET(1-0), RPLVAL#, SUSPA# Valid Delay	3	24	4-6	
T9	BLAST#, PLOCK# Float Delay		28	4-7	Note 1
T9a	RPLSET(1-0), RPLVAL# Float Delay		28	4-7	Note 1
T10	D31-D0, DP3-DP0 Write Data Valid Delay	3	20	4-6	
T11	D31-D0, DP3-DP0 Write Data Float Delay		28	4-7	Note 1
T12	EADS# Setup Time	8		4-3	
T12a	INVAL Setup Time	8		4-3	
T13	EADS# Hold Time	3		4-3	
T13a	INVAL Hold Time	3		4-3	
T14	BS16#, BS8#, KEN# Setup Time	8		4-3	
T15	BS16#, BS8#, KEN# Hold Time	3		4-3	
T16	BRDY#, RDY# Setup Time	8		4-4	
T17	BRDY#, RDY# Hold Time	3		4-4	
T18	AHOLD, HOLD Setup Time	10		4-3	
T18a	BOFF# Setup Time	10		4-3	
T19	AHOLD, BOFF#, HOLD Hold Time	3		4-3	
T20	A20M#, FLUSH#, IGNNE#, INTR, NMI, RESET Setup Time	10		4-3	
T20a	SMI#, SUSP#, WM_RST Setup Time	10		4-3	
T21	A20M#, FLUSH#, INTR, IGNNE#, NMI, RESET Hold Time	3		4-3	
T21a	SMI#, SUSP#, WM_RST Hold Time	3		4-3	
T22	A31-A4, D31-D0, DP3-DP0 Read Setup Time	6		4-3, 4-4	
T23	A31-A4, D31-D0, DP3-DP0 Read Hold Time	3		4-3, 4-4	

Note 1: Not 100% tested.

Table 4-12. AC Characteristics for BL486DX-V33/BL486DX2-V66
V_{CC} = 3.0 to 3.6 V, T_{CASE} = 0° to 85° C, C_L = 50pF
External CLK = 33 MHz (Max.)

SYMBOL	PARAMETERS	MIN (ns)	MAX (ns)	FIGURE	NOTES
T1	CLK Period	30		4-2	
T2	CLK High Time	11		4-2	At 2 V
T3	CLK Low Time	11		4-2	$V_{IL(MAX)}$
T4	CLK Fall Time		3	4-2	2 V to $V_{IL(MAX)}$
T5	CLK Rise Time		3	4-2	$V_{IL(MAX)}$ to 2 V
T6	A31-A2, ADS#, BE3#-BE0#, BREQ, D/C#, FERR#, HLDA, LOCK#, M/IO#, PCD, PWT, W/R# Valid Delay	3	16	4-6	
T6a	SMADS#, SMI# Valid Delay	3	16	4-6	
T7	A31-A2, ADS#, BE3#-BE0#, BREQ, D/C#, HLDA, LOCK#, M/IO#, PCD, PWT, W/R# Float Delay		20	4-7	Note 1
T7a	SMADS#, SMI# Float Delay		20	4-7	Note 1
T8	PCHK# Valid Delay	3	22	4-5	
T8a	BLAST#, PLOCK# Valid Delay	3	20	4-6	
T8b	HITM#, RPLSET(1-0), RPLVAL#, SUSPA# Valid Delay	3	20	4-6	
T9	BLAST#, PLOCK# Float Delay		20	4-7	Note 1
T9a	RPLSET(1-0), RPLVAL# Float Delay		20	4-7	Note 1
T10	D31-D0, DP3-DP0 Write Data Valid Delay	3	19	4-6	
T11	D31-D0, DP3-DP0 Write Data Float Delay		20	4-7	Note 1
T12	EADS# Setup Time	6		4-3	
T12a	INVAL Setup Time	6		4-3	
T13	EADS# Hold Time	3		4-3	
T13a	INVAL Hold Time	3		4-3	
T14	BS16#, BS8#, KEN# Setup Time	6		4-3	
T15	BS16#, BS8#, KEN# Hold Time	3		4-3	
T16	BRDY#, RDY# Setup Time	6		4-4	
T17	BRDY#, RDY# Hold Time	3		4-4	
T18	AHOLD, HOLD Setup Time	6		4-3	
T18a	BOFF# Setup Time	9		4-3	
T19	AHOLD, BOFF#, HOLD Hold Time	3		4-3	
T20	A20M#, FLUSH#, IGNNE#, INTR, NMI, RESET Setup Time	6		4-3	
T20a	SMI#, SUSP#, WM_RST Setup Time	6		4-3	
T21	A20M#, FLUSH#, IGNNE#, INTR, NMI, RESET Hold Time	3		4-3	
T21a	SMI#, SUSP#, WM_RST Hold Time	3		4-3	
T22	A31-A4, D31-D0, DP3-DP0 Read Setup Time	6		4-3, 4-4	
T23	A31-A4, D31-D0, DP3-DP0 Read Hold Time	3		4-3, 4-4	

Note 1: Not 100% tested.

Table 4-13. AC Characteristics for BL486DX-V40, BL486DX2-V80
V_{CC} = 3.0 to 3.6 V, T_{CASE} = 0° to 85° C, C_L = 50pF
External CLK = 40 MHz (Max.)

SYMBOL	PARAMETERS	MIN (ns)	MAX (ns)	FIGURE	NOTES
T1	CLK Period	25		4-2	
T2	CLK High Time	9		4-2	At 2 V
T3	CLK Low Time	9		4-2	$V_{IL(MAX)}$
T4	CLK Fall Time		3	4-2	2 V to $V_{IL(MAX)}$
T5	CLK Rise Time		3	4-2	$V_{IL(MAX)}$ to 2 V
T6	A31-A2, ADS#, BE3#-BE0#, BREQ, D/C#, FERR#, HLDA, LOCK#, M/IO#, PCD, PWT, W/R# Valid Delay	3	14	4-6	
T6a	SMADS#, SMI# Valid Delay	3	14	4-6	
T7	A31-A2, ADS#, BE3#-BE0#, BREQ, D/C#, HLDA, LOCK#, M/IO#, PCD, PWT, W/R# Float Delay		19	4-7	Note 1
T7a	SMADS#, SMI# Float Delay		19	4-7	Note 1
T8	PCHK# Valid Delay	3	18	4-5	
T8a	BLAST#, PLOCK# Valid Delay	3	16	4-6	
T8b	HITM#, RPLSET(1-0), RPLVAL#, SUSPA# Valid Delay	3	16	4-6	
T9	BLAST#, PLOCK# Float Delay		16	4-7	Note 1
T9a	RPLSET(1-0), RPLVAL# Float Delay		16	4-7	Note 1
T10	D31-D0, DP3-DP0 Write Data Valid Delay	3	17	4-6	
T11	D31-D0, DP3-DP0 Write Data Float Delay		19	4-7	Note 1
T12	EADS# Setup Time	6		4-3	
T12a	INVAL Setup Time	6		4-3	
T13	EADS# Hold Time	3		4-3	
T13a	INVAL Hold Time	3		4-3	
T14	BS16#, BS8#, KEN# Setup Time	6		4-3	
T15	BS16#, BS8#, KEN# Hold Time	3		4-3	
T16	BRDY#, RDY# Setup Time	6		4-4	
T17	BRDY#, RDY# Hold Time	3		4-4	
T18	AHOLD, HOLD Setup Time	6		4-3	
T18a	BOFF# Setup Time	7		4-3	
T19	AHOLD, BOFF#, HOLD Hold Time	3		4-3	
T20	A20M#, FLUSH#, IGNNE#, INTR, NMI, RESET Setup Time	6		4-3	
T20a	SMI#, SUSP#, WM_RST Setup Time	6		4-3	
T21	A20M#, FLUSH#, IGNNE#, INTR, NMI, RESET Hold Time	3		4-3	
T21a	SMI#, SUSP#, WM_RST Hold Time	3		4-3	
T22	A31-A4, D31-D0, DP3-DP0 Read Setup Time	6		4-3, 4-4	
T23	A31-A4, D31-D0, DP3-DP0 Read Hold Time	3		4-3, 4-4	

Note 1: Not 100% tested

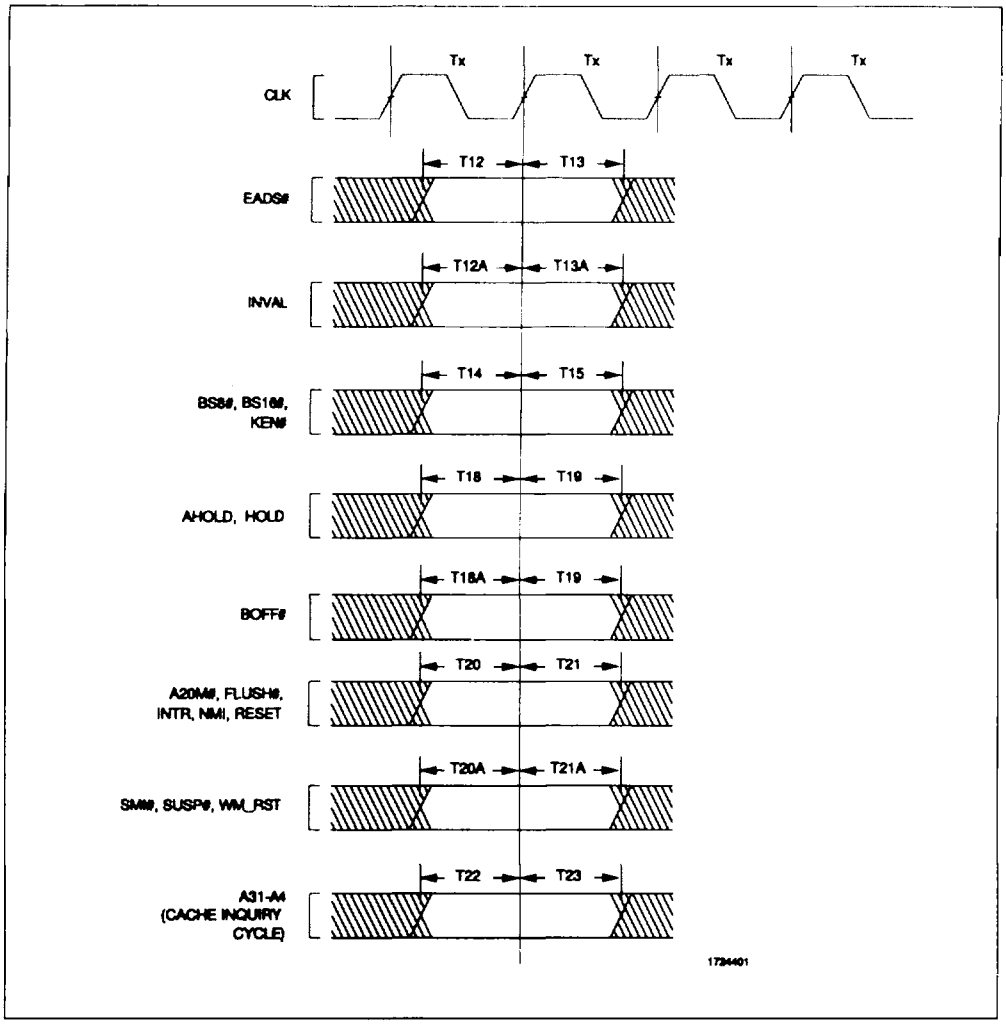

Figure 4-3. Input Setup and Hold Timing

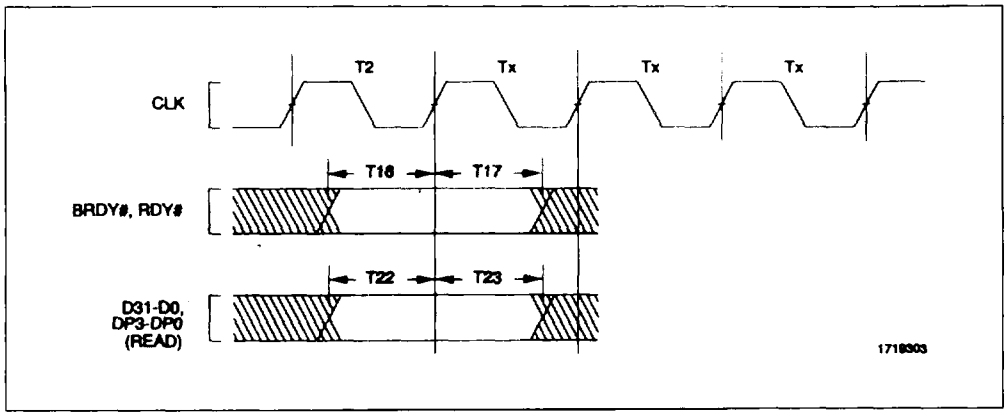

Figure 4-4. Input Setup and Hold Timing (continued)

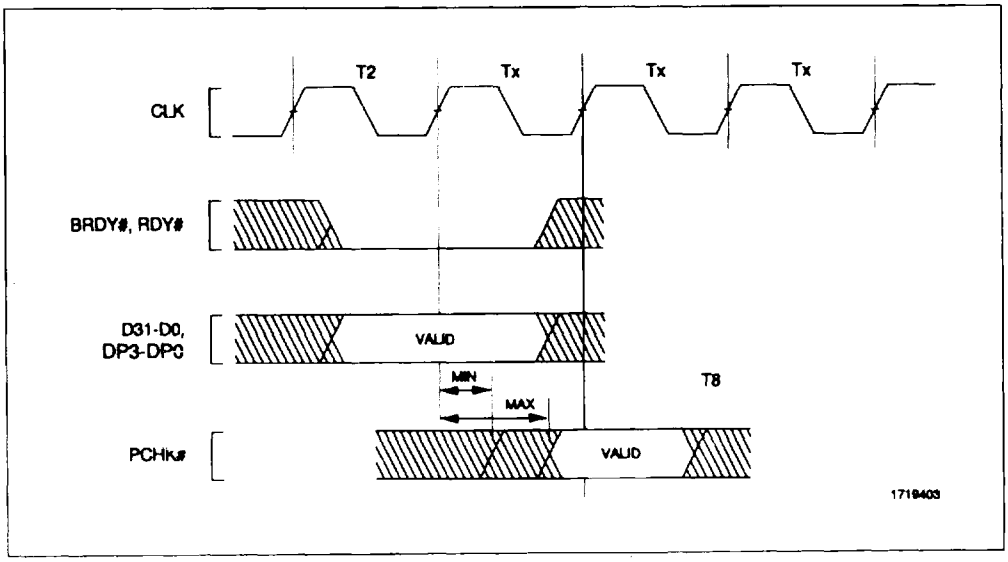

Figure 4-5. .PCHK# Valid Delay Timing

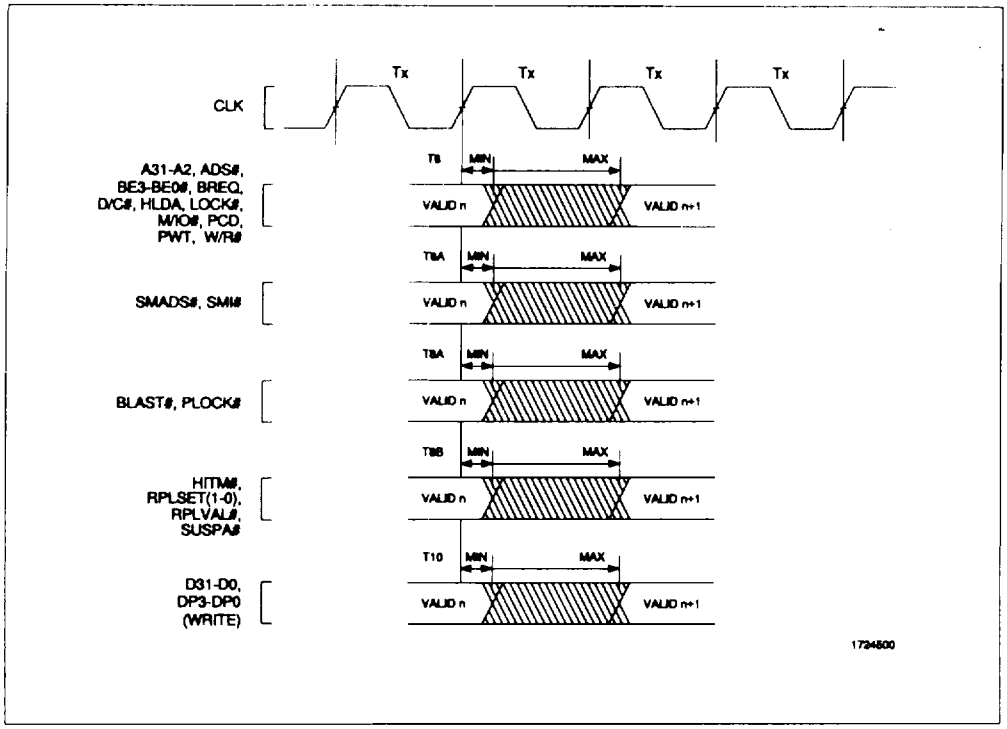

Figure 4-6 . Output Valid Delay Timing

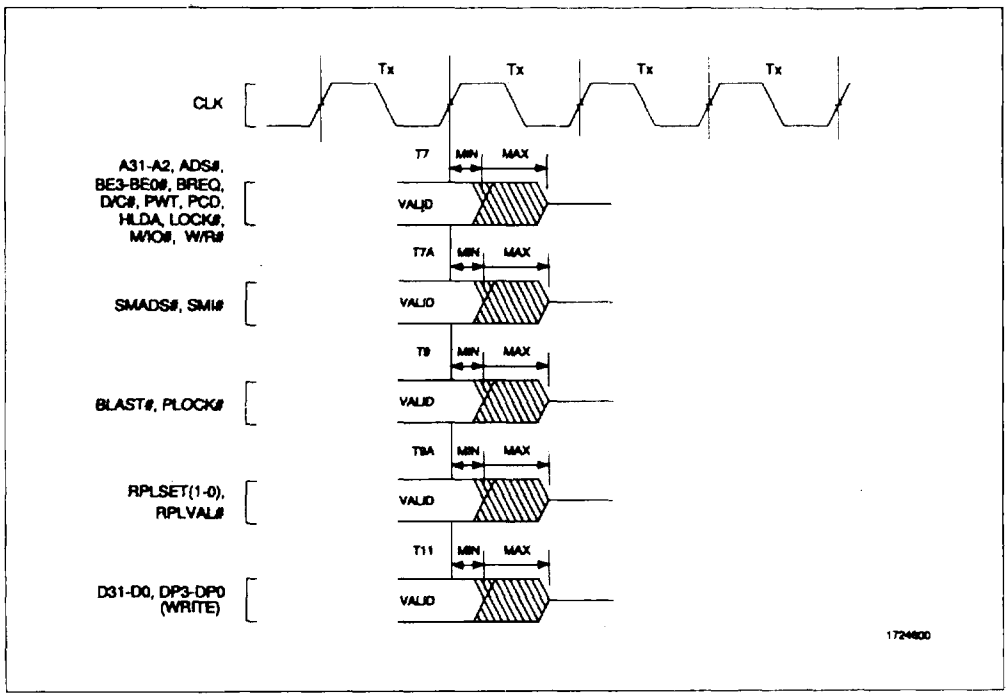

Figure 4-7 . Maximum Float Delay Timing