Integrated Device Technology, Inc.

HIGH-SPEED 1K x 8 FOUR-PORT STATIC RAM

ADVANCE INFORMATION
IDT 7050S
IDT 7050L

FEATURES:

- High-speed access
  - Military: 30/35/45ns (max.)
  - Commercial: 25/30/35/45ns (max.)
- Low-power operation
  - IDT7050S
    Active: ---mW (typ.)
    Standby: ---mW (typ.)
  - IDT7050L
    Active: ---mW (typ.)
    Standby: ---mW (typ.)
- Fully asynchronous operation from each of the four ports: P1, P2, P3, P4
- Versatile control for write-inhibit: separate $\overline{BUSY}$ input to control write-inhibit for each of the four ports
- Battery backup operation—2V data retention
- TTL-compatible; single 5V (±10%) power supply
- Available in several popular hermetic and plastic packages for both through-hole and surface mount
- Military product compliant to MIL-STD-883, Class B

DESCRIPTION:

The IDT7050 is a high-speed 1K x 8 four-port static RAM designed to be used in systems where multiple access in a common RAM is required. This four-port static RAM offers increased system performance in multiprocessed systems that have a need to communicate in real time and also offers added benefit for high-speed systems in which multiple access is required in the same cycle.

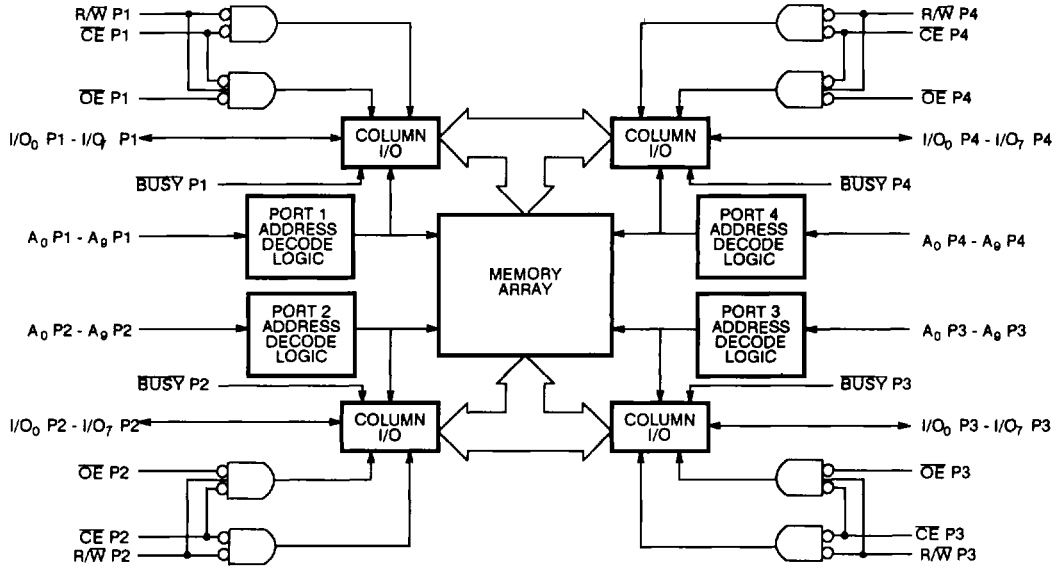
The IDT7050 is also an extremely high-speed 1K x 8 four-port static RAM designed to be used in systems where on-chip hardware port arbitration is not needed. This part lends itself to those systems which cannot tolerate wait states or are designed to be able to externally arbitrate or withstand contention when all ports simultaneously access the same four-port RAM location.

The IDT7050 provides four independent ports with separate control, address and I/O pins that permit independent, asynchronous access for reads or writes to any location in memory. It is the user's responsibility to ensure data integrity when simultaneously accessing the same memory location from all ports. An automatic power down feature, controlled by $\overline{CE}$, permits the on-chip circuitry of each port to enter a very low standby power mode.

Fabricated using IDT's CEMOS™ high-performance technology, these four ports typically operate on only ---mW of power at maximum access times as fast as 25ns. Low-power (L) versions offer battery backup data retention capability, with each port typically consuming ---μW from a 2V battery.

The IDT7050 is packaged in either a ceramic or plastic 108-pin PGA and 132-pin quad flatpack. Military grade product is manufactured in compliance with the latest revision of MIL-STD-883, Class B.

FUNCTIONAL BLOCK DIAGRAM



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PIN CONFIGURATIONS

SYMBOL	PIN NAME
A0 P1 - A9 P1	Address Lines - Port 1
A0 P2 - A9 P2	Address Lines - Port 2
A0 P3 - A9 P3	Address Lines - Port 3
A0 P4 - A9 P4	Address Lines - Port 4
I/O0 P1 - I/O7 P1	Data I/O - Port 1
I/O0 P2 - I/O7 P2	Data I/O - Port 2
I/O0 P3 - I/O7 P3	Data I/O - Port 3
I/O0 P4 - I/O7 P4	Data I/O - Port 4
R/$\overline{W}$ P1	Read/Write - Port 1
R/$\overline{W}$ P2	Read/Write - Port 2
R/$\overline{W}$ P3	Read/Write - Port 3
R/$\overline{W}$ P4	Read/Write - Port 4
GND	Ground
$\overline{CE}$ P1	Chip Enable - Port 1
$\overline{CE}$ P2	Chip Enable - Port 2
$\overline{CE}$ P3	Chip Enable - Port 3
$\overline{CE}$ P4	Chip Enable - Port 4
$\overline{OE}$ P1	Output Enable - Port 1
$\overline{OE}$ P2	Output Enable - Port 2
$\overline{OE}$ P3	Output Enable - Port 3
$\overline{OE}$ P4	Output Enable - Port 4
$\overline{BUSY}$ P1	Write Disable - Port 1
$\overline{BUSY}$ P2	Write Disable - Port 2
$\overline{BUSY}$ P3	Write Disable - Port 3
$\overline{BUSY}$ P4	Write Disable - Port 4
V_{CC}	Power
GND	Ground

81 R/$\overline{W}$ P2	80 NC	77 A7 P2	74 A5 P2	72 A3 P2	69 A0 P2	68 A0 P3	65 A3 P3	63 A5 P3	60 A7 P3	57 NC	54 R/$\overline{W}$ P3	12
84 $\overline{BUSY}$ P2	83 $\overline{OE}$ P2	78 A8 P2	76 NC	73 A4 P2	70 A1 P2	67 A1 P3	64 A4 P3	61 NC	59 A8 P3	56 $\overline{OE}$ P3	53 $\overline{BUSY}$ P3	11
87 A2 P1	86 A1 P1	82 $\overline{CE}$ P2	79 A9 P2	75 A6 P2	71 A2 P2	66 A2 P3	62 A6 P3	58 A9 P3	55 $\overline{CE}$ P3	51 A1 P4	50 A2 P4	10
90 A5 P1	88 A3 P1	85 A0 P1							52 A0 P4	49 A3 P4	47 A5 P4	09
92 NC	91 A6 P1	89 A4 P1							48 A4 P4	46 A6 P4	45 NC	08
95 A8 P1	94 A7 P1	93 V_{CC}				IDT7050 108 Pin PGA			44 GND	43 A7 P4	42 A8 P4	07
96 A9 P1	97 NC	98 $\overline{CE}$ P1				TOP VIEW			39 $\overline{CE}$ P4	40 NC	41 A9 P4	06
99 R/$\overline{W}$ P1	100 $\overline{OE}$ P1	102 I/O0 P1							35 V_{SS}	37 $\overline{OE}$ P4	38 R/$\overline{W}$ P4	05
101 $\overline{BUSY}$ P1	103 I/O1 P1	106 GND							31 GND	34 I/O7 P4	36 $\overline{BUSY}$ P4	04
104 I/O2 P1	105 I/O3 P1	1 I/O6 P1	4 V_{CC}	8 GND	12 V_{CC}	17 V_{CC}	21 GND	25 V_{CC}	28 I/O2 P4	32 I/O5 P4	33 I/O6 P4	03
107 I/O4 P1	2 I/O7 P1	5 I/O0 P2	7 I/O2 P2	10 I/O4 P2	13 I/O6 P2	16 I/O1 P3	19 I/O3 P3	22 I/O5 P3	24 I/O7 P3	29 I/O3 P4	30 I/O4 P4	02
108 I/O5 P1	3 NC	6 I/O1 P2	9 I/O3 P2	11 I/O5 P2	14 I/O7 P2	15 I/O0 P3	18 I/O2 P3	20 I/O4 P3	23 I/O6 P3	26 I/O0 P4	27 I/O1 P4	01
A	B	C	D	E	F	G	H	J	K	L	M	

NOTES:
1. All V_{CC} pins must be connected to the power supply.
2. All GND pins must be connected to the ground supply.

ABSOLUTE MAXIMUM RATINGS (1)

SYMBOL	RATING	COMMERCIAL	MILITARY	UNIT
V_{TERM}	Terminal Voltage with Respect to GND	-0.5 to +7.0	-0.5 to +7.0	V
T_A	Operating Temperature	0 to +70	-55 to +125	°C
T_{BIAS}	Temperature Under Bias	-55 to +125	-65 to +135	°C
T_{STG}	Storage Temperature	-55 to +125	-65 to +150	°C
I_{OUT}	DC Output Current	50	50	mA

NOTE:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

SYMBOL	PARAMETER(1)	CONDITIONS	MAX.	UNIT
C_{IN}	Input Capacitance	V_{IN} = 0V	11	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	11	pF

NOTE:
1. This parameter is determined by device characterization but is not production tested.

RECOMMENDED OPERATING TEMPERATURE AND SUPPLY VOLTAGE

GRADE	AMBIENT TEMPERATURE	GND	V_{CC}
Military	-55°C to +125°C	0V	5.0V ± 10%
Commercial	0°C to +70°C	0V	5.0V ± 10%

RECOMMENDED DC OPERATING CONDITIONS

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{CC}	Supply Voltage	4.5	5.0	5.5	V
GND	Supply Voltage	0	0	0	V
V_{IH}	Input High Voltage	2.2	–	6.0	V
V_{IL}	Input Low Voltage	-0.5(1)	–	0.8	V

NOTE:
1. V_{IL} (min.) = -3.0V for pulse width less than 20ns.

DC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE AND SUPPLY VOLTAGE (V_{CC} = 5.0V ±10%)

SYMBOL	PARAMETER	TEST CONDITIONS	IDT7050S MIN.	IDT7050S MAX.	IDT7050L MIN.	IDT7050L MAX.	UNIT
$\|I_{LI}\|$	Input Leakage Current	V_{CC} = 5.5V, V_{IN} = 0V to V_{CC}	–	10	–	5	µA
$\|I_{LO}\|$	Output Leakage Current	$\overline{CE}$ = V_{IH}, V_{OUT} = 0V to V_{CC}	–	10	–	5	µA
V_{OL}	Output Low Voltage	I_{OL} = 4mA	–	0.4	–	0.4	V
V_{OH}	Output High Voltage	I_{OH} = -4mA	2.4	–	2.4	–	V

DC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE AND SUPPLY VOLTAGE RANGE [1, 2] (V_{CC} = 5.0V ±10%)

SYMBOL	PARAMETER	TEST CONDITION	VERSION		IDT7050x25[3] TYP.	IDT7050x25[3] MAX.	IDT7050x30 TYP.	IDT7050x30 MAX.	IDT7050x35 TYP.	IDT7050x35 MAX.	IDT7050x45 TYP.	IDT7050x45 MAX.	UNIT
I_{CC1}	Operating Power Supply Current (All Ports Active)	$\overline{CE}$ = V_{IL}, Outputs Open, f = 0[4]	MIL.	S	–	–	–	360	–	360	–	360	mA
				L	–	–	–	300	–	300	–	300	
			COM'L.	S	–	300	–	300	–	300	–	300	
				L	–	250	–	250	–	250	–	250	
I_{CC2}	Dynamic Operating Current (All Ports Active)	$\overline{CE}$ = V_{IL}, Outputs Open, f = f_{MAX}[5]	MIL.	S	–	–	–	400	–	395	–	390	mA
				L	–	–	–	335	–	330	–	325	
			COM'L.	S	–	350	–	340	–	335	–	330	
				L	–	295	–	285	–	280	–	275	
I_{SB}	Standby Current (All Ports – TTL Level Inputs)	$\overline{CE}$ ≥ V_{IH}, f = f_{MAX}[5]	MIL.	S	–	–	–	115	–	110	–	105	mA
				L	–	–	–	85	–	80	–	75	
			COM'L.	S	–	85	–	80	–	75	–	70	
				L	–	70	–	65	–	60	–	55	
I_{SB1}	Full Standby Current (Both Ports – All CMOS Level Inputs)	All Ports, $\overline{CE}$ ≥ V_{CC} -0.2V, V_{IN} ≥ V_{CC} -0.2V or V_{IN} ≤ 0.2V, f = 0[4]	MIL.	S	–	–	–	15	–	15	–	15	mA
				L	–	–	–	4.5	–	4.5	–	4.5	
			COM'L.	S	–	5	–	5	–	5	–	5	
				L	–	1.5	–	1.5	–	1.5	–	1.5	

NOTES:

1. "x" in part number indicates power rating (S or L).
2. V_{CC} = 5V, T_A = +25°C for TYP.
3. 0°C to +70°C temperature range only.
4. f = 0 means no address or control lines change.
5. At f = f_{MAX}, address and data inputs (except Output Enable) are cycling at the maximum frequency of read cycle of $1/t_{RC}$, and using "AC Test Conditions" of input levels of GND to 3V.

DATA RETENTION CHARACTERISTICS OVER ALL TEMPERATURE RANGES[1]

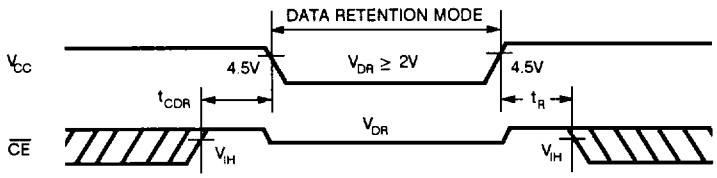
(L Version Only) V_{LC} = 0.2V, V_{HC} = V_{CC} - 0.2V

SYMBOL	PARAMETER	TEST CONDITION		MIN.	TYP.[1]	MAX.	UNIT
V_{DR}	V_{CC} for Data Retention	V_{CC} = 2V $\overline{CE} \geq V_{HC}$ $V_{IN} \geq V_{HC}$ or $\leq V_{LC}$		2.0	–	–	V
I_{CCDR}	Data Retention Current		MIL.	–	–	1800	µA
			COM'L.	–	–	600	
t_{CDR}[3]	Chip Deselect to Data Retention Time			0	–	–	ns
t_R[3]	Operation Recovery Time			t_{RC}[2]	–	–	ns

NOTES:
1. V_{CC} = 2V, T_A = +25°C
2. t_{RC} = Read Cycle Time
3. This parameter is guaranteed but not tested.

5

LOW V_{CC} DATA RETENTION WAVEFORM



AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	5ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figures 1 & 2

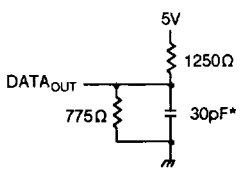


Figure 1. Output Load

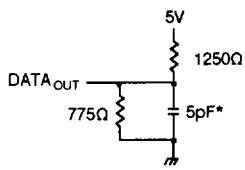


Figure 2. Output Load (for t_{LZ}, t_{HZ}, t_{WZ}, t_{OW})

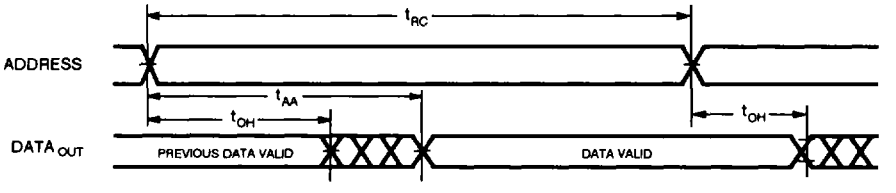
*Including scope and jig.

AC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE AND SUPPLY VOLTAGE

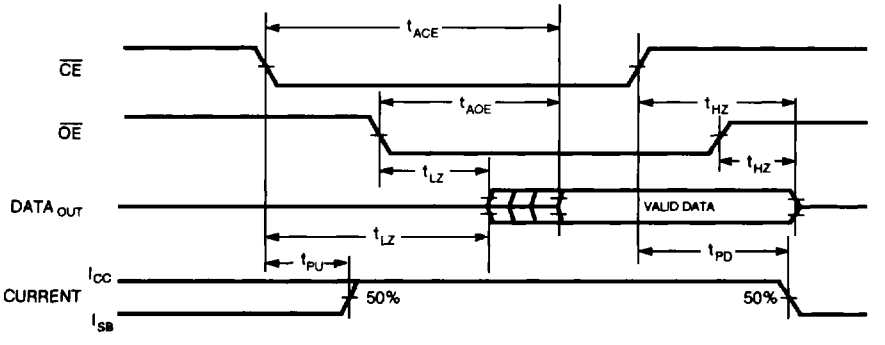
SYMBOL	PARAMETER	IDT7050S25 [1, 3] IDT7050L25 [1, 3] MIN.	MAX.	IDT7050S30 IDT7050L30 MIN.	MAX.	IDT7050S35 IDT7050L35 MIN.	MAX.	IDT7050S45 IDT7050L45 MIN.	MAX.	UNIT
READ CYCLE										
t_{RC}	Read Cycle Time	25	–	30	–	35	–	45	–	ns
t_{AA}	Address Access Time	–	25	–	30	–	35	–	45	ns
t_{ACE}	Chip Enable Access Time	–	25	–	30	–	35	–	45	ns
t_{AOE}	Output Enable Access Time	–	15	–	20	–	25	–	30	ns
t_{OH}	Output Hold From Address Change	0	–	0	–	0	–	0	–	ns
t_{LZ}	Output Low Z Time [1, 2]	3	–	3	–	5	–	5	–	ns
t_{HZ}	Output High Z Time [1, 2]	–	15	–	15	–	15	–	20	ns
t_{PU}	Chip Enable to Power Up Time [2]	0	–	0	–	0	–	0	–	ns
t_{PD}	Chip Disable to Power Down Time [2]	–	20	–	30	–	50	–	50	ns

NOTES:
1. Transition is measured ±500mV from low or high impedance voltage with load (Figures 1 and 2).
2. This parameter is guaranteed but not tested.
3. 0°C to +70°C temperature range only.

TIMING WAVEFORM OF READ CYCLE NO. 1, EITHER SIDE [1, 2, 4]



TIMING WAVEFORM OF READ CYCLE NO. 2, EITHER SIDE [1, 3]



NOTES:
1. R/$\overline{W}$ is high for Read Cycles.
2. Device is continuously enabled, $\overline{CE}$ = V_{IL}.
3. Addresses valid prior to or coincident with $\overline{CE}$ transition low.
4. $\overline{OE}$ = V_{IL}

AC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE AND SUPPLY VOLTAGE

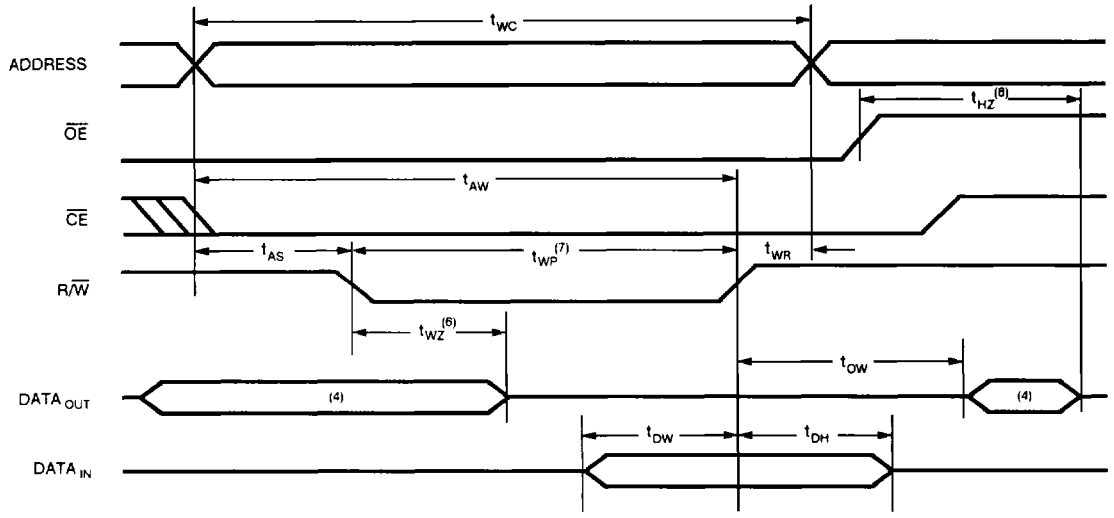
SYMBOL	PARAMETER	IDT7050S25[7] IDT7050L25[7] MIN.	MAX.	IDT7050S30 IDT7050L30 MIN.	MAX.	IDT7050S35 IDT7050L35 MIN.	MAX.	IDT7050S45 IDT7050L45 MIN.	MAX.	UNIT
WRITE CYCLE										
t_{WC}	Write Cycle Time	25	–	30	–	35	–	45	–	ns
t_{EW}	Chip Enable to End of Write	20	–	25	–	30	–	35	–	ns
t_{AW}	Address Valid to End of Write	20	–	25	–	30	–	35	–	ns
t_{AS}	Address Set-up Time	0	–	0	–	0	–	0	–	ns
t_{WP}	Write Pulse Width[3]	20	–	25	–	30	–	35	–	ns
t_{WR}	Write Recovery Time	5	–	5	–	5	–	5	–	ns
t_{DW}	Data Valid to End of Write	15	–	15	–	20	–	20	–	ns
t_{HZ}	Output High Z Time[1,2]	–	15	–	15	–	15	–	20	ns
t_{DH}	Data Hold Time	0	–	0	–	0	–	0	–	ns
t_{WZ}	Write Enabled to Output in High Z[1,2]	–	15	–	15	–	15	–	20	ns
t_{OW}	Output Active From End of Write[1,2]	0	–	0	–	0	–	0	–	ns
t_{WDD}	Write Pulse to Data Delay[4]	–	40	–	50	–	60	–	70	ns
t_{DDD}	Write Data Valid to Read Data Delay[4]	–	30	–	35	–	40	–	45	ns
BUSY INPUT TIMING										
t_{WB}	Write to $\overline{Busy}$[5]	0	–	0	–	0	–	0	–	ns
t_{WH}	Write Hold After $\overline{Busy}$[6]	15	–	20	–	20	–	20	–	ns

NOTES:

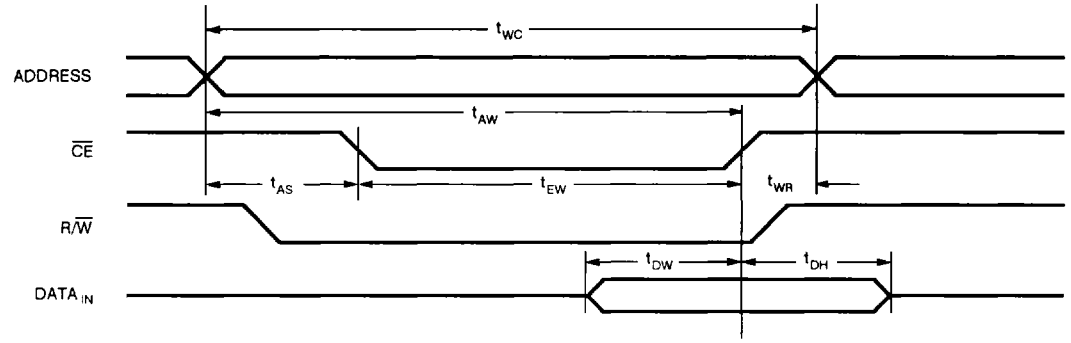
1. Transition is measured ±500mV from low or high impedance voltage with load (Figures 1 and 2).
2. This parameter is guaranteed but not tested.
3. Specified for $\overline{OE}$ at high (refer to "Timing Waveform of Write Cycle", Note 7).
4. Port-to-port delay through RAM cells from writing port to reading port, refer to "Timing Waveform of Read with Port-to-Port Delay".
5. To ensure that the write cycle is inhibited during contention.
6. To ensure that a write cycle is completed after contention.
7. 0°C to +70°C temperature range only.

5

TIMING WAVEFORM OF WRITE CYCLE NO. 1, R/$\overline{W}$ CONTROLLED TIMING [1, 2, 3, 7]



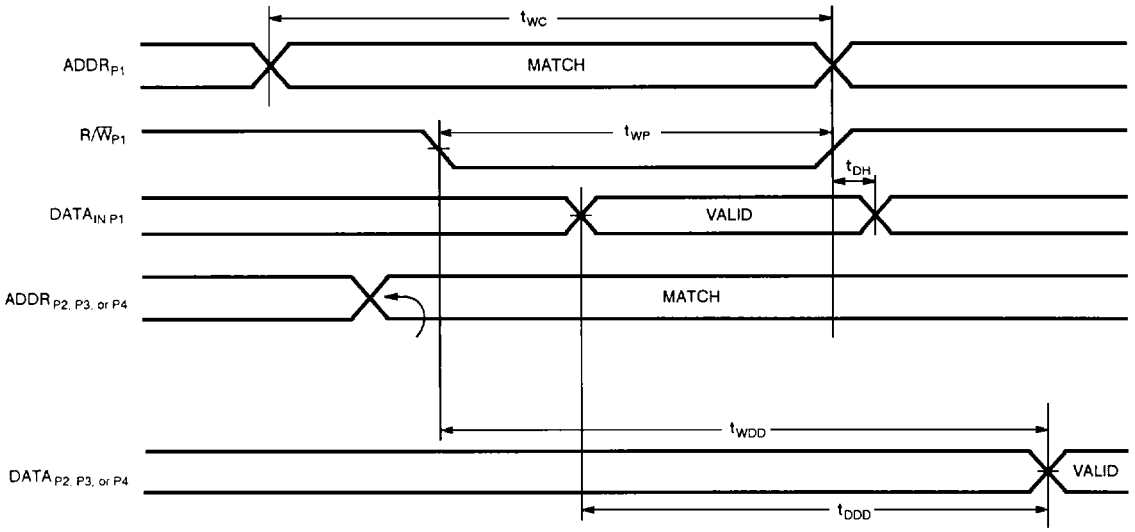
TIMING WAVEFORM OF WRITE CYCLE NO. 2, $\overline{CE}$ CONTROLLED TIMING [1, 2, 3, 5]



NOTES:

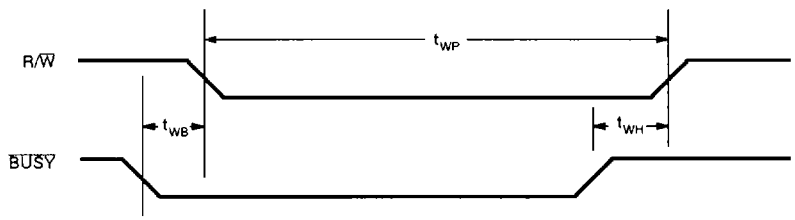
1. R/$\overline{W}$ must be high during all address transitions.
2. A write occurs during the overlap (t_{EW} or t_{WP}) of a low $\overline{CE}$ and a low R/$\overline{W}$.
3. t_{WR} is measured from the earlier of $\overline{CE}$ or R/$\overline{W}$ going high to the end of write cycle.
4. During this period, the I/O pins are in the output state, and input signals must not be applied.
5. If the $\overline{CE}$ low transition occurs simultaneously with or after the R/$\overline{W}$ low transition, the outputs remain in the high impedance state.
6. Transition is measured ±500mV from steady state with a 5pF load (including scope and jig). This parameter is sampled and not 100% tested.
7. If $\overline{OE}$ is low during a R/$\overline{W}$ controlled write cycle, the write pulse width must be the larger of t_{WP} or (t_{WZ} + t_{DW}) to allow the I/O drivers to turn off data to be placed on the bus for the required t_{DW}. If $\overline{OE}$ is high during an R/$\overline{W}$ controlled write cycle, this requirement does not apply and the write pulse can be as short as the specified t_{WP}.

TIMING WAVEFORM OF READ WITH PORT-TO-PORT DELAY (1, 2, 3)



NOTES:
1. Assume $\overline{BUSY}$ input at HI and $\overline{CE}$ at LO for the writing port.
2. Write cycle parameters should be adhered to, to ensure proper writing.
3. Device is continuously enabled for any of the reading ports which has its $\overline{OE}$ at LO.

TIMING WAVEFORM OF WRITE WITH $\overline{BUSY}$ INPUT



FUNCTIONAL DESCRIPTION:

The IDT7050 provides four ports with separate control, address and I/O pins that permit independent access for reads or writes to any location in memory. These devices have an automatic power down feature controlled by $\overline{CE}$. The $\overline{CE}$ controls on-chip power down circuitry that permits the respective port to go into standby mode when not selected ($\overline{CE}$ high). When a port is enabled, access to the entire memory array is permitted. Each port has its own Output Enable control ($\overline{OE}$). In the read mode, the port's $\overline{OE}$ turns on the output drivers when set LOW. READ/WRITE conditions are illustrated in the table below.

TABLE I—READ/WRITE CONTROL

ANY PORT (1)				FUNCTION
R/$\overline{W}$	$\overline{CE}$	$\overline{OE}$	D_{0-7}	
X	H	X	Z	Port Disabled and In Power Down Mode
X	H	X	Z	$\overline{CE}_{P1} = \overline{CE}_{P2} = \overline{CE}_{P3} = \overline{CE}_{P4}$, = H Power Down Mode, I_{SB1} or I_{SB}
L	L	X	$DATA_{IN}$	Data on Port Written Into Memory (2,3)
H	L	L	$DATA_{OUT}$	Data in Memory Output on Port
X	X	H	Z	High Impedance Outputs

NOTES:

1. H = HIGH, L = LOW, X = DON'T CARE, Z = HIGH IMPEDANCE
2. If $\overline{BUSY}$ = LOW, data is not written.
3. For valid write operation, no more than one port can write to the same address location at the same time.