



Integrated Device Technology, Inc.

**128KB/256KB  
SECONDARY CACHE MODULES FOR  
THE INTEL® i486™ PROCESSOR**

INTEGRATED DEVICE

IDT7MP6121  
IDT7MP6122

**FEATURES**

- 128KB/256KB secondary cache module family
- Ideal for use with many Intel i486 CPU-based systems that use the industry standard chipsets
- Operates with external i486 processor speeds of 50MHz
- 64 position dual read-out SIMM (Single In-line Memory Module) with 128 leads
- Single 5V (±5%) power supply
- Multiple GND pins and decoupling capacitors for maximum noise immunity

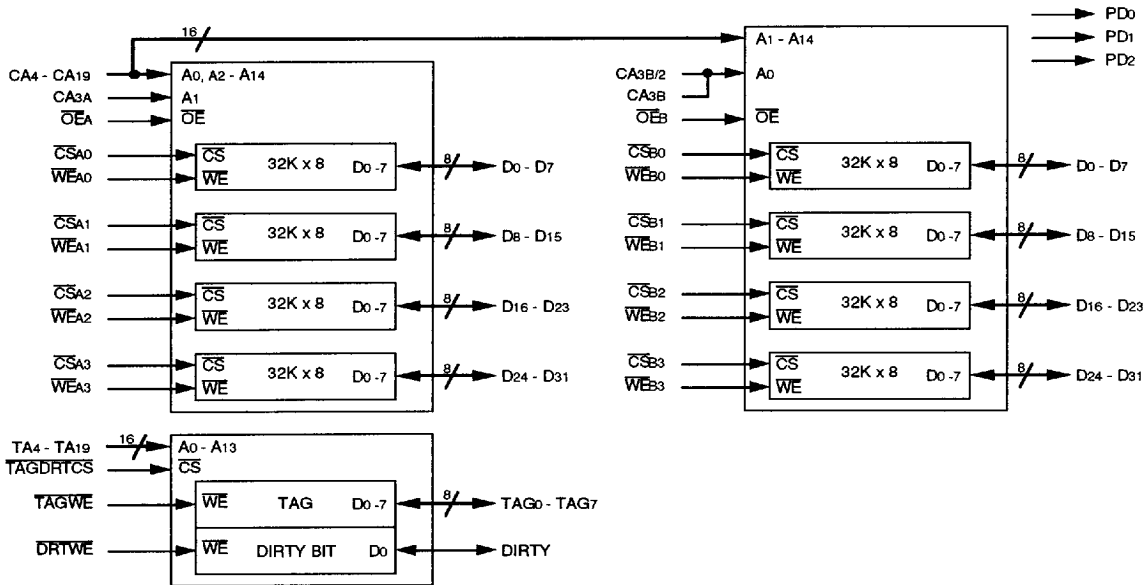
**DESCRIPTION**

The IDT7MP6121/22 are members of a family of secondary caches that are ideal for use with many Intel i486 CPU-based systems. The IDT7MP6121/22 use IDT's asynchronous SRAMs in plastic surface mount packages mounted on a multilayer epoxy laminate (FR-4) board. High speeds at optimum costs are achieved using IDT's high-performance, high-reliability CMOS technology.

The dual read-out SIMM package configuration allows 128 signal leads to be placed on a package 3.85" long. Depending on which cache configuration is used, the module is a maximum of 0.35" thick and a maximum of 1.05" tall.

The IDT7MP6121/22 operate from single 5V power supply. Multiple GND pins and on-board decoupling capacitors ensure maximum protection from noise.

**FUNCTIONAL BLOCK DIAGRAM  
IDT7MP6122 – 256KB VERSION**



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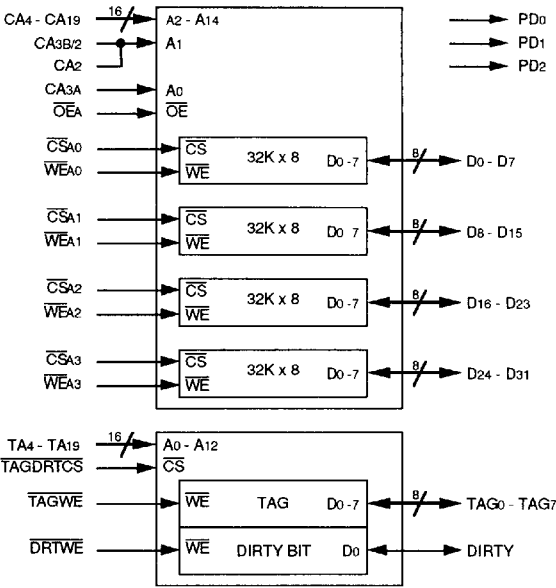
**COMMERCIAL TEMPERATURE RANGE**

**SEPTEMBER 1993**

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DSC-7105/1  
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**FUNCTIONAL BLOCK DIAGRAM**  
**IDT7MP6121 – 128KB VERSION**



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**PIN NAMES**

CA4 – CA19	Cache Address Inputs
CA2, CA3B/2, CA3A, CA3B	Bank Cache Address Inputs
D0 – D31	Cache Data Inputs/Outputs
CSA0 – CSA3	Bank A Byte Chip Select Inputs
CSB0 – CSB3	Bank B Byte Chip Select Inputs
WEA0 – WEA3	Bank A Byte Write Enable Inputs
WEB0 – WEB3	Bank B Byte Write Enable Inputs
OEA	Bank A Output Enable Input
OEB	Bank B Output Enable Input
TA4 – TA19	Tag, Dirty Bit Address Inputs
TAG0 – TAG7	Tag Data Inputs/Outputs
DIRTY	Dirty Bit Input/Output
TAGDRTCS	Tag/Dirty Chip Select Input
TAGWE	Tag Write Enable Input
DRTWE	Dirty Bit Write Enable Input
PD0 – PD2	Presence Detect Pins
N C	No Connect
GND	Ground
Vcc	Power Supply

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**PIN CONFIGURATION<sup>(3)</sup>**

PD0	1	65	PD1
PD2	2	66	GND
D0	3	67	D1
D2	4	68	D3
D4	5	69	VCC
D6	6	70	D5
D8	7	71	D7
GND	8	72	D9
D10	9	73	D11
D12	10	74	D13
D14	11	75	D15
D16	12	76	D17
D18	13	77	D19
D20	14	78	D21
GND	15	79	GND
D22	16	80	D23
D24	17	81	D25
VCC	18	82	VCC
D26	19	83	D27
D28	20	84	D29
D30	21	85	D31
(1) N C	22	86	N C (1)
(1) N C	23	87	N C (1)
GND	24	88	GND
CSA0	25	89	CSB0(2)
CSA1	26	90	CSB1(2)
CSA2	27	91	VCC
CSA3	28	92	CSB2(2)
GND	29	93	CSB3(2)
OEA	30	94	OEB(2)
WEA0	31	95	WEB0(2)
WEA1	32	96	WEB1(2)
WEA2	33	97	WEB2(2)
WEA3	34	98	WEB3(2)
TAGWE	35	99	DRTWE
TAGDRTCS	36	100	VCC
(1) N C	37	101	N C (1)
(1) N C	38	102	N C (1)
CA3A	39	103	CA3B/2
CA2	40	104	CA3B
GND	41	105	GND
CA4	42	106	CA5
CA6	43	107	CA7
CA8	44	108	CA9
CA10	45	109	CA11
CA12	46	110	CA13
CA14	47	111	CA15
CA16	48	112	CA17
CA18	49	113	CA19
GND	50	114	GND
TA4	51	115	TA5
TA6	52	116	TA7
TAB	53	117	TA9
TA10	54	118	TA11
TA12	55	119	TA13
TA14	56	120	TA15
TA16	57	121	TA17
TA18	58	122	TA19
GND	59	123	GND
TAG0	60	124	TAG1
TAG2	61	125	TAG3
TAG4	62	126	TAG5
TAG6	63	127	TAG7
DIRTY	64	128	VCC

**DUAL READ-OUT SIMM  
TOP VIEW**

**NOTES:**

- 1 These pins are reserved for future use. Please consult the factory for details.
- 2 These pins are N C (no connect) on the IDT7MP6121 module.
- 3 The module pinout supports cache sizes up to 1MB.

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**PRESENCE DETECT TABLE**

PD2	PD1	PD0	Size	Module
N.C.	N.C.	N.C.	—	no cache present
N.C.	N.C.	GND	—	reserved
N.C.	GND	N.C.	—	reserved
N.C.	GND	GND	128KB	IDT7MP6121
GND	N.C.	N.C.	256KB	IDT7MP6122
GND	N.C.	GND	—	reserved
GND	GND	N.C.	—	reserved
GND	GND	GND	—	reserved

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**CAPACITANCE<sup>(1, 2)</sup>**

(TA = +25°C, f = 1.0 MHz)

Symbol	Parameter <sup>(1)</sup>	Condition	7MP6121/22	Unit
CIN1	Input Capacitance (Data Address)	VIN = 0V	50/95	pF
CIN2	Input Capacitance (Tag Address, TAGDRTCS)	VIN = 0V	20	pF
CIN3	Input Capacitance (OE <sub>A</sub> , OE <sub>B</sub> )	VIN = 0V	50	pF
CIN4	Input Capacitance (All other controls)	VIN = 0V	14	pF
CIO1	Data I/O Capacitance	VOUT = 0V	14/25	pF
CIO2	Tag I/O Capacitance	VOUT = 0V	12	pF

**NOTES:**

1. These parameters are guaranteed by design but not tested.
2. These parameters are maximum values.

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**RECOMMENDED DC OPERATING CONDITIONS<sup>(1)</sup>**

Symbol	Parameter	Min.	Typ.	Max.	Unit
Vcc	Supply Voltage	4.75	5.0	5.25	V
GND	Supply Voltage	0	0	0.0	V
VIH	Input High Voltage	2.2	—	6.0	V
VIL	Input Low Voltage	-0.5 <sup>(1)</sup>	—	0.8	V

**NOTE:**

1 VIL = -3.0V for pulse width less than 5ns.

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**RECOMMENDED OPERATING TEMPERATURE AND SUPPLY VOLTAGE**

Grade	Ambient Temperature	GND	Vcc
Commercial	0°C to +70°C	0V	5.0V

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**ABSOLUTE MAXIMUM RATINGS**

Symbol	Rating	Value	Unit
VTERM	Terminal Voltage with Respect to GND	-0.5 to +7.0	V
TA	Operating Temperature	0 to +70	°C
TBIAS	Temperature Under Bias	-10 to +85	°C
TSTG	Storage Temperature	-55 to +125	°C
IOUT	DC Output Current	50	mA

**NOTE:**

Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

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**DC ELECTRICAL CHARACTERISTICS**

(Vcc = 5.0V ± 5%, TA = 0°C to 70°C)

Symbol	Parameter	Test Condition	7MP6121/22 Min.	7MP6121/22 Max.	Unit
ILI	Input Leakage Current (Data)	Vcc = Max, VIN = GND to Vcc	—	10/20	µA
ILI	Input Leakage Current (Data Address)	Vcc = Max, VIN = GND to Vcc	—	40/80	µA
ILI	Input Leakage Current (Tag Address, TAGDRTCS)	Vcc = Max, VIN = GND to Vcc	—	20	µA
ILI	Input Leakage Current (OE <sub>A</sub> , OE <sub>B</sub> )	Vcc = Max, VIN = GND to Vcc	—	40	µA
ILI	Input Leakage Current (Control)	Vcc = Max, VIN = GND to Vcc	—	10	µA
ILO	Output Leakage Current (Data)	VOUT = 0V to Vcc, Vcc = Max., CS ≥ VIH	—	10/20	µA
ILO	Output Leakage Current (Tag)	VOUT = 0V to Vcc, Vcc = Max., CS ≥ VIH	—	10	µA
VOL	Output Low Voltage	IOL = 8mA, Vcc = Min.	—	0.4	V
VOH	Output High Voltage	IOL = -4mA, Vcc = Min.	2.4	—	V
Icc	Operating Power Supply Current	Vcc = Max., CS ≤ VIL, f = fMAX, Outputs Open	—	935/1525	mA
Isb	Standby Supply Current	Vcc = Max., CS ≥ VIH, f = fMAX, Outputs Open	—	300/510	mA
Isb1	Full Standby Supply Current	Vcc = Max., CS ≥ Vcc - 0.2V, f = 0, VIN > Vcc - 0.2V or < 0.2V	—	115/200	mA

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**SRAM CYCLE TIMES<sup>(1, 2)</sup>**

Module Speed	Size	Data	Tag	Dirty
33MHz	128KB	20ns	15ns	15ns
33MHz	256KB	20ns	15ns	15ns

**NOTES:**  
 1 Cycle times are for the SRAMs themselves used on the module  
 Modules are tested for function only  
 2 Please consult the factory regarding other speeds

**AC TEST CONDITIONS INTEGRATED DEVICE**

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	5ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figures 1 and 2

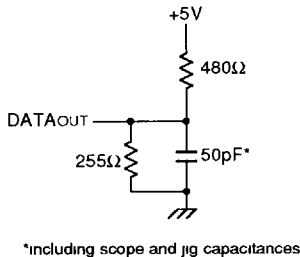


Figure 1. Output Load

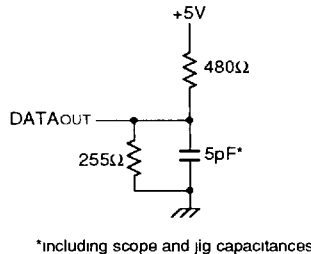
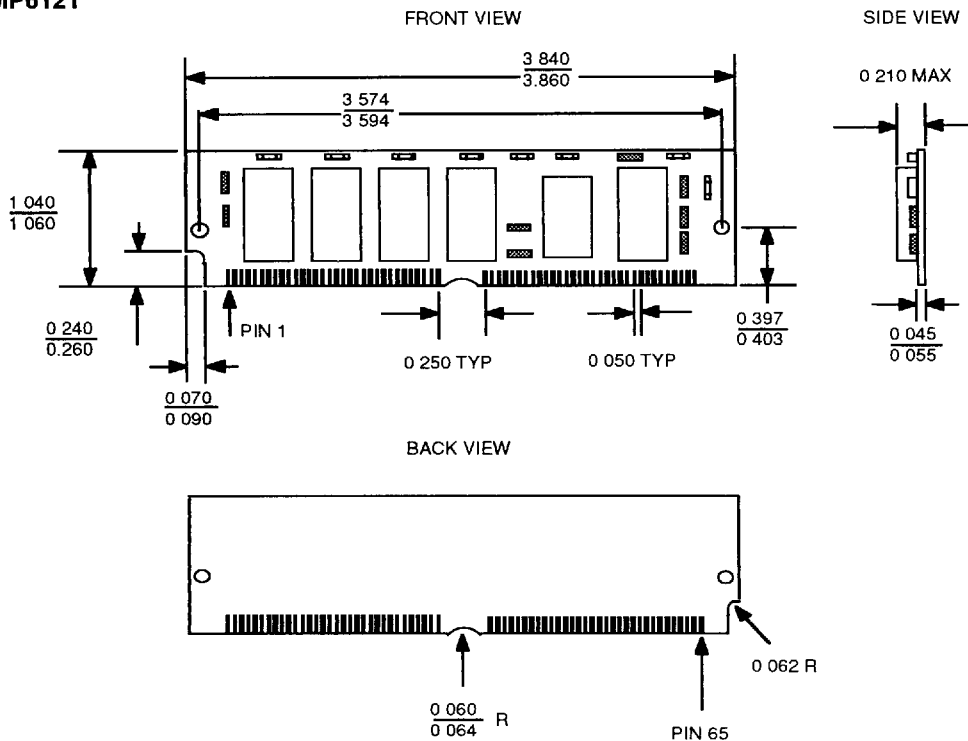


Figure 2. Output Load (for tOHZ, tCHZ, tOLZ and tCLZ)

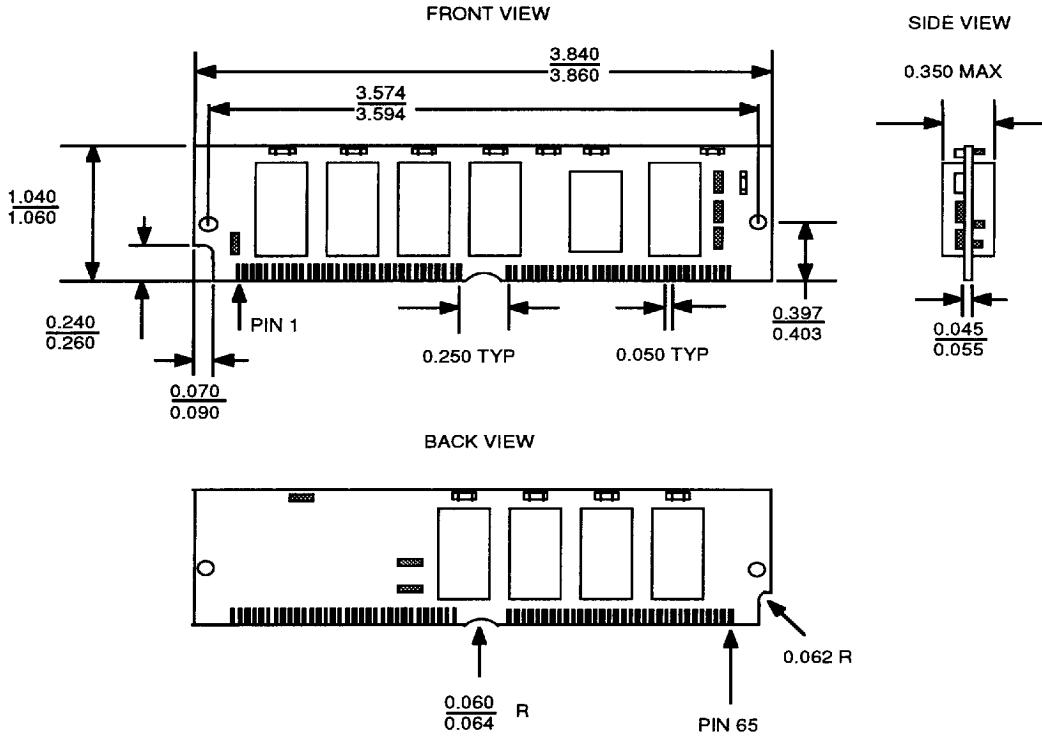
**PACKAGE DIMENSIONS**

**7MP6121**

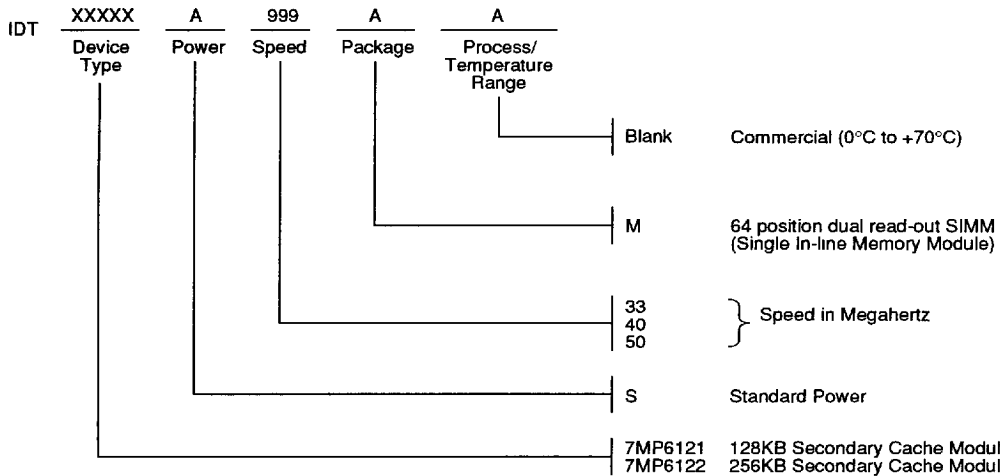


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7MP6122



**ORDERING INFORMATION**



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