JMF662

SATA III to Flash controller

Overview

JMF662 is a single chip, supports external SDRAM, SATA III to NAND flash interface. It is native design to provide higher bandwidth for flash memory access.

JMF662 can support the maximum read and write speed to drive the limit of flash memory. JMF662 has the best supporting to the latest NAND flash memory, including Toshiba 32nm/24nm HBL/ABL Flash. It also provides the embedded hardware error correction code (ECC), wear leveling, and bad block management technology in this chip. In order to resolve compatibility issue, JMF662 provides the on line firmware upgrade ability.

JMF662 provides embedded processor, internal masked ROM, data SRAM, SATA link/transport layer, SATA PHY. Data swap between different interfaces can be done very efficiency by DMA without CPU involvement. Based on the efficient architecture, the JMF662 can provide the best performance.

Features

Compliance

- Compliant with Serial ATA International Organization: Serial ATA Revision 2.6.

SATAI\II

- Supports 1-port 1.5/3.0/6.0Gbps SATA I/II/III interface.

CPU

- Embedded data buffer.
- 32bits Embedded processor.
- 32 KBytes Embedded masked program ROM.
- 128 KBytes Embedded system RAM.

Flash

- Support maximum 16CE’s Flash per channel.
- Support 32/24 nm Flash.
- Support legacy/toggle mode Flash
- Enhanced endurance by dynamic/static wear-leveling.
- Supports 4K/8K/16K bytes page size.
- Supports dynamic power management.
- SMART (Self-Monitoring, Analysis and Reporting Technology).
- Data integrity under power-cycling.
- Supports online SATA firmware update.

- Supports BCH 8/16/24/40 bits ECC.
- Support Shift read feature of NAND flash when ECC fail

SDRAM

- Support DDR2
- Support 512Mbits to 2Gbits

SYSTEM

- Integrated SATA III port and 8-channels Flash controller.
- LED indicator for SATA read/write access.
- LED indicator for SATA PHY link up.
- Provides 14 GPIO pins for customer.
- Provides UART and JTAG for S/W debugging.
- Built-in power-up self-test (BIST).
- Manual and automatic self-diagnostics.
- Provides voltage low detect interrupt.
- 399-ball TFBGA package

Firmware

- Support NCQ on this controller.
- Support LBA24 & LBA48 on this controller.
- Support 1/2/4/8 banks selected free.
- Support 4/8 channels selected free.

Block Diagram

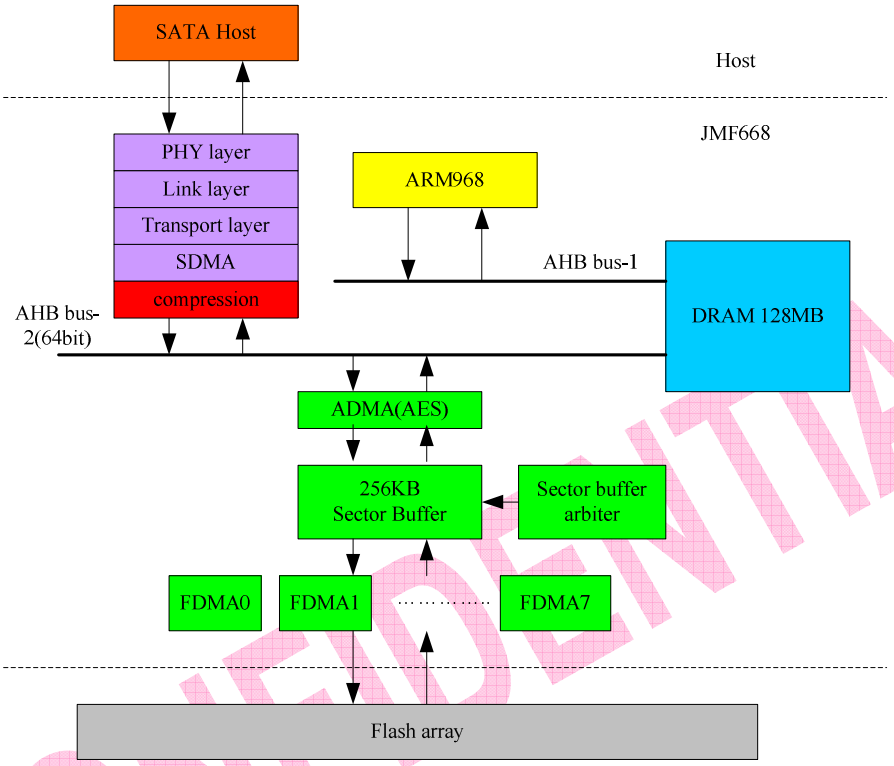

Figure 1: JMF662 Block Diagram

Total capacity

density/per flash	Support CE pins/per flash	maximum flash number	Total capacity
1G x 8 Bits (8Gb)	1 CE pin	32	32G Bytes
2G x 8 Bits (16Gb)	1 CE/ 2 CE pin	32	64G Bytes
4G x 8 Bits (32Gb)	1 CE/ 2 CE pin	32	128G Bytes
8G x 8 Bits (64Gb)	2 CE pin	32	256G Bytes
16G x 8 Bits (128Gb)	4 CE pin	32	512G Bytes

Table 1: JMF662 Total capacity table

Product Information

Name	Description
JMF662	SATA II to Flash Controller

Document

1	JMF662 Data Sheet
2	JMF662 Design Specification
3	JMF662 Hardware Design Guide
4	JMF662 Hardware Schematic

Contact Information

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