mo∫aic
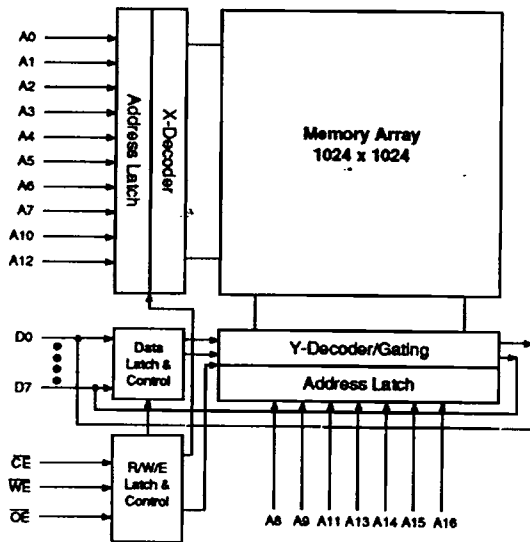
Mosaic Semiconductor Inc.

31,072 x 8 bit CMOS EEPROM

Features

Fast Access Time of 120/150/200 ns.
Operating Power 275 mW max.
Standby Power 2.75mW max.
Software Data Protection.
Data Polling/Toggle bit.
Byte or Page Write Cycle: 5ms typical.
JEDEC Pinout.
High Density VIL™ Package.
Data Retention > 10 years.
Endurance > 10^4 Write Cycles.
May be Processed In Accordance with
MIL-STD-883, Method 5004.

Block Diagram

Pin Definition
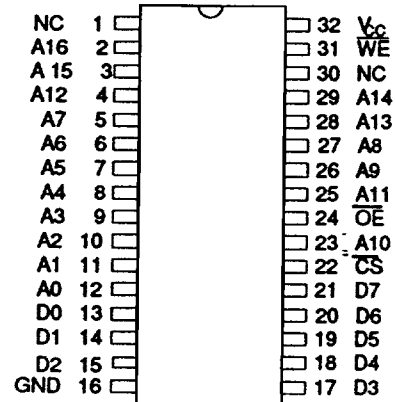
Package Type: 'V'

NC	1	32	Vcc
A16	2	31	WE
A15	3	30	NC
A12	4	29	A14
A7	5	28	A13
A6	6	27	A8
A5	7	26	A9
A4	8	25	A11
A3	9	24	OE
A2	10	23	A10
A1	11	22	CS
A0	12	21	D7
D0	13	20	D6
D1	14	19	D5
D2	15	18	D4
GND	16	17	D3

Pin Functions

A0-16	Address Inputs
D0-7	Data Inputs/Outputs
CS	Chip Select
OE	Output Enable
WE	Write Enable
NC	No Connect
Vcc	Power (+5V)
GND	Ground

Package Details (See package details section for details)

Pin Count	Description	Package Type	Material	Pin Out
32	100 mil Vertical-In-Line	VIL™	Ceramic	JEDEC

VIL is a Trademark of Mosaic Semiconductor Inc. US patent number D316251

MOSCS016

Absolute Maximum Ratings

Voltage on any pin relative to GND	V_T	-1.0 to +7.0	V
Power Dissipation	P_T	1	W
Storage Temperature	T_{STG}	-65 to +150	°C
Temperature Under Bias	T_{BIAS}	-65 to +135	°C

Notes : (1) Stresses above those listed may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

(2) V_T can be -3.5V pulse of less than 20ns.

Recommended Operating Conditions

		min	typ	max	
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Input High Voltage	V_{IH}	2.0	-	V_{CC}+1	V
Input Low Voltage	V_{IL}	-0.1	-	0.8	V
Operating Temperature	T_A	0	-	70	°C
	T_{AL}	-40	-	85	°C (MEM832I)
	T_{AM}	-55	-	125	°C (MEM832M,MB)

DC Electrical Characteristics

Parameter	Symbol	Test Condition	min	max	Unit
Input Leakage Current	I_{LI}	V_{IN}=GND to V_{CC}	-	10	µA
Output Leakage Current	I_{LO}	$\overline{CS}$=V_{IH}, V_{IO}=GND to V_{CC}	-	10	µA
Average Current	I_{CC1}	I_{IO}=0mA,$\overline{CS}$=$\overline{OE}$ =V_{IL},$\overline{WE}$ =V_{IH}, f=5MHz	-	50	mA
Standby Current TTL	I_{SB}	$\overline{CS}$=V_{IH}, OE=V_{IL}, I_{IO}=0mA	-	3	mA
Standby Current CMOS	I_{SB1}	$\overline{CE}$ =V_{CC}-0.3V, $\overline{OE}$ =V_{IL} , I_{IO}=0mA	-	500	µA
Output Voltage	V_{OL}	I_{OL}=2.1mA	-	0.4	V
	V_{OH}	I_{OH}=-400 µA	2.4	-	V

Capacitance (V_{CC}=5V±10%,T_A=25°C, f=1MHz)

Parameter	Symbol	Test Condition	typ	max	Unit
Input Capacitance	C_{IN}	V_{IN} = 0V	-	10	pF
I/O Capacitance	C_{IO}	V_{IO} = 0V	-	10	pF

Note: This parameter is periodically sampled and not 100% tested.

AC Test Conditions

* Input pulse levels: 0V to 3.0V
* Input rise and fall times: 10ns
* Input and Output timing reference levels: 1.5V
* Output load: 1 TTL gate + 100pF
* V_{CC}=5V±10%

Output Test Load

Vcc

1.8 kΩ

Output Pin

1.3 kΩ   100 pF
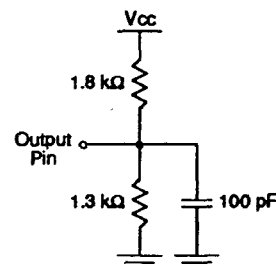
AC READ CHARACTERISTICS

Read Cycle

Parameter	Symbol	-12 min	-12 max	-15 min	-15 max	-20 min	-20 max	Unit	Notes
Read Cycle Time	t_{RC}	120	-	150	-	200	-	ns	
Address Access Time	t_{AA}	-	120	-	150	-	200	ns	
$\overline{CS}$ Access Time	t_{CS}	-	120	-	150	-	200	ns	
$\overline{OE}$ Access Time	t_{OE}	0	50	0	50	0	50	ns	
$\overline{CS}$, $\overline{OE}$ High to High Z Output	t_{HZ}, t_{OHZ}	0	50	0	50	0	50	ns	(1)
$\overline{CS}$, $\overline{OE}$ Low to Active Output	t_{LZ}, t_{OLZ}	0	-	0	-	0	-	ns	(1)
Output Hold from Address Change	t_{OH}	0	-	0	-	0	-	ns	

Notes: (1) t_{LZ} max. and t_{OLZ} max. are measured with CL = 5pF, from the point when $\overline{CS}$ or $\overline{OE}$ return high (whichever occurs first) to the time when the outputs are no longer driven. t_{HZ} and t_{OHZ} are shown for reference only: they are characterized and not tested.

### Read Cycle Timing Waveform
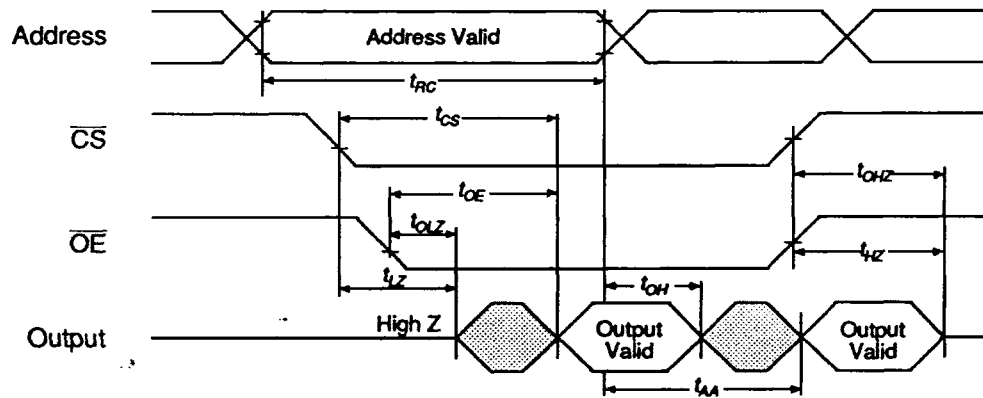
AC WRITE CHARACTERISTICS

Write Cycle

| Parameter	Symbol	min	typ	max	Unit
Write Cycle Time	t_{WC}	-	-	10	ms
Address Set-up Time	t_{AS}	0	-	-	ns
Address Hold Time	t_{AH}	50	-	-	ns
$\overline{OE}$ Set-up Time	t_{OES}	10	-	-	ns
$\overline{OE}$ Hold Time	t_{OEH}	10	-	-	ns
Chip Select Set-up Time	t_{CS}	0	-	-	ns
Chip Select Hold Time	t_{CH}	0	-	-	ns
Chip Select Pulse Width	t_{CW}	100	-	-	ns
Write Pulse Width	t_{WP}	100	-	-	ns
$\overline{WE}$ High Recovery	t_{WPH}	100	-	-	ns
Data Set-up Time	t_{DS}	50	-	-	ns
Data Hold Time	t_{DH}	10	-	-	ns
Data Valid	t_{DV}	-	-	1	μs
Delay to Next Write	t_{DW}	10	-	-	μs
Byte Load Cycle	t_{BLC}	0.2	-	100	μs

AC Write Waveform - $\overline{WE}$ Controlled
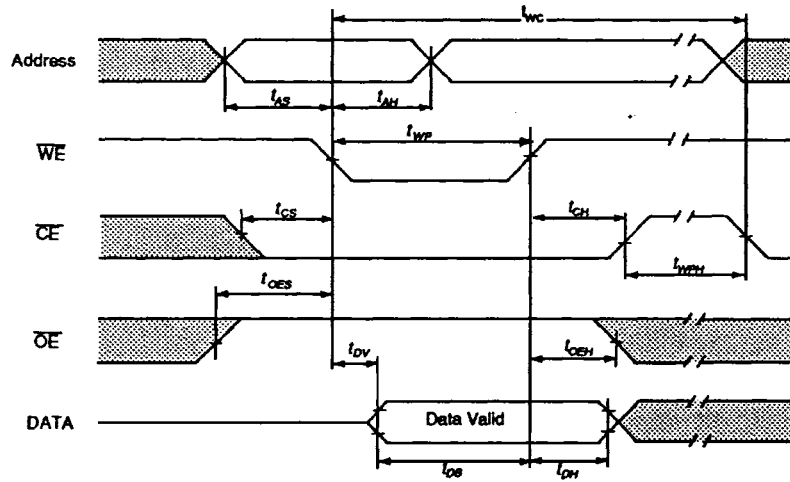
AC Write Waveform - $\overline{CS}$ Controlled
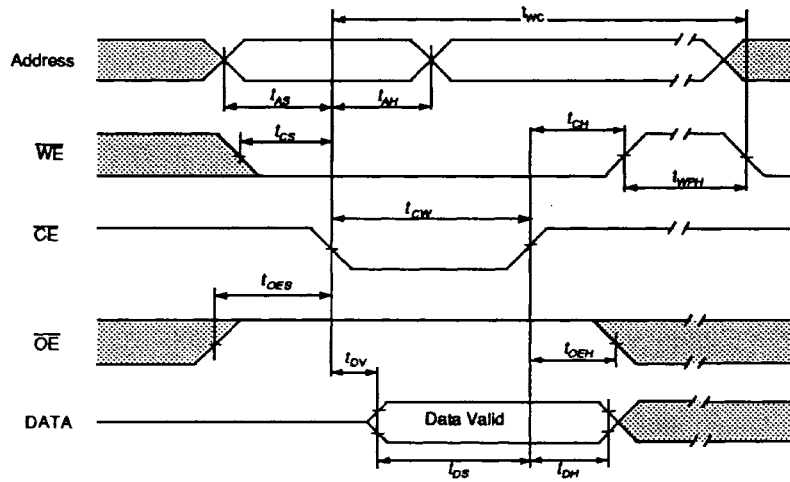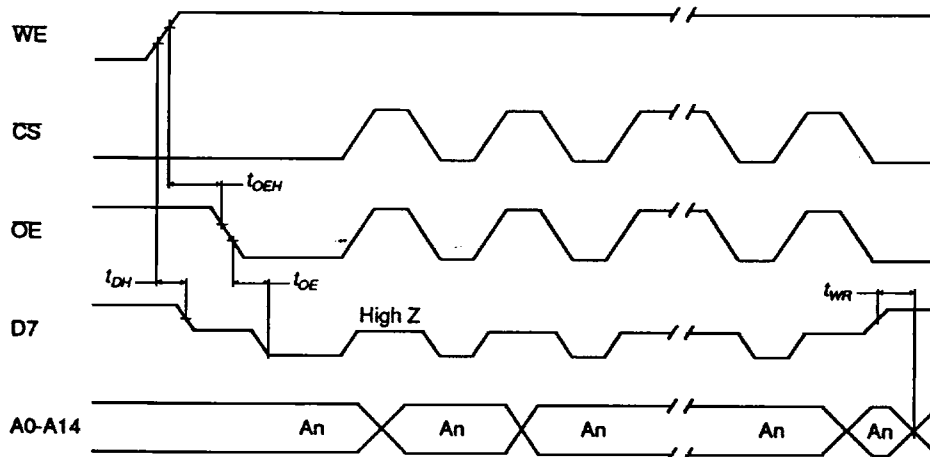
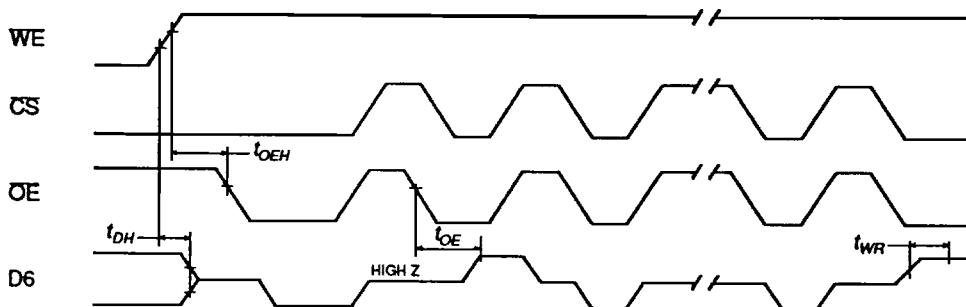## Page Mode Write Waveform
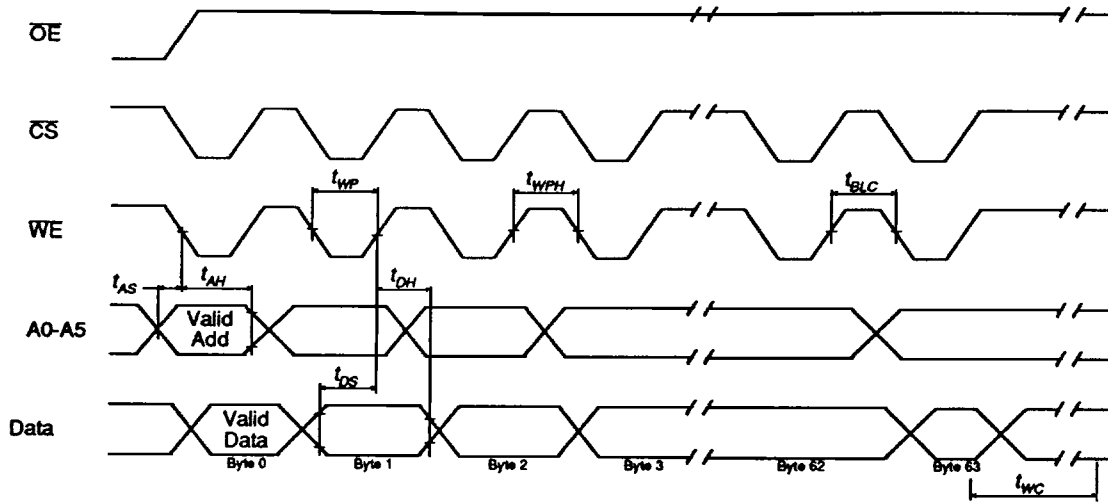
Note: A6 through A14 must specify the page address during each high to low transition of $\overline{WE}$ (or $\overline{CE}$).
$\overline{OE}$ must be high only when $\overline{WE}$ and $\overline{CE}$ are both low.

$\overline{DATA}$ Polling Waveform

Toggle Bit Waveform

Device Operation

Read

The MEM8128 read operations are initiated by both $\overline{OE}$ and $\overline{CS}$ LOW. The read operation is terminated by either $\overline{CS}$ or $\overline{OE}$ returning HIGH. This 2-line control architecture elimanates bus connection in a system environment. The data bus will be in a high impendence state when either $\overline{OE}$ or $\overline{CS}$ is HIGH.

Write

Write operations are initated when both $\overline{CS}$ and $\overline{WE}$ are LOW and $\overline{OE}$ is HIGH. The MEM8128 supports both a $\overline{CS}$ and $\overline{WE}$ controlled write cycle. That is, the address is latched by the falling edge of either $\overline{CS}$ or $\overline{WE}$, whichever occurs last. Similarly, the data is latched internally by the rising edge of either $\overline{CS}$ or $\overline{WE}$, whichever occurs first. A byte write operation, once initiated, will automatically continue to completion, typically within 5 ms.

Page Mode Write

The page write feature of the MEM8128 allows the entire memory to be written in 5 seconds. Page Write allows 256 bytes of data to be written prior to the internal programming cycle. The host can fetch data from another location within the system during a page write operation (change the source address), but the page address (A6 through A16) for each subsequent valid write cycle to the part during this operation must be the same as the initial page address.

The page write mode can be initiated during any write operation. Following the initial byte write cycle, the host can write up to 256 bytes in the same manner as the first byte written. Each successive byte load cycle, started by the $\overline{WE}$ HIGH to LOW transition, must begin within 100 μs of the falling edge of the preceding $\overline{WE}$. If a subsequent $\overline{WE}$ HIGH to LOW transition is not detected within 100 μs, the internal automatic programming cycle will commence.

DATA Polling

The MEM8128 features DATA Polling to indicate if the write cycle is completed. During the internal programming cycle, any attempt to read the last byte written will produce the compliment of that data on D7. Once the programming is complete, D7 will refect the true data. Note: If the the MEM8128 is in a protected state and an illegal write operation is attempted DATA Polling will not operate.

TOGGLE bit

In addition to DATA polling, another method is provided to determine the end of a Write Cycle. During a write operation successive attempts to read data will result in D6 toggling between 1 and 0. Once a write is complete, this toggling will stop and valid data will be read.

Hardware Data Protection

The MEM8128 provides three harware features to protect nonvololitile data from inadvertent writes.

* Noise Protection - A $\overline{WE}$ pulse less than 10 ns will not indicate a write cycle.

* Default V_{cc} Sence - All functions are inhabited when V_{cc} is ≤ 3.6 V.

* Write Inhibit - Holding either $\overline{OE}$ LOW, $\overline{WE}$ HIGH or $\overline{CS}$ HIGH will prevent an inadvertent write cycle during power-on power-off, maintaining data integrity.

Software Data Protection

The MEM8128 can be automatically protected during power-up and power-down without the need for external circuits by employing the software data protect feature. The internal software data protection circuit is enabled after the first write operation utilizing the software algorithm. This circuit is nonvolatile and will remain set for the life of the device unless the reset command is issued.
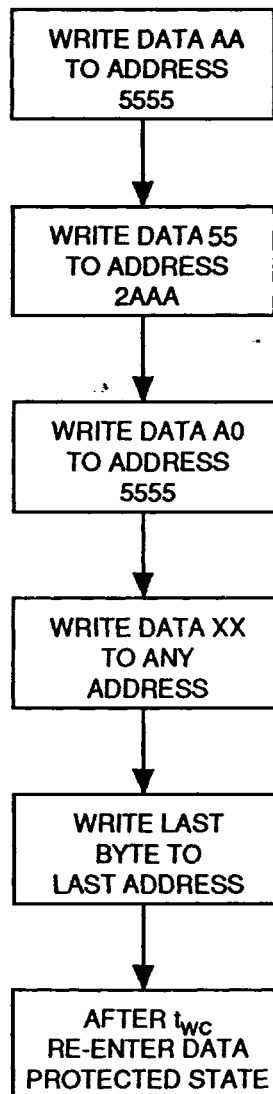
Once the software protection is enabled, the MEM8128 is also protected against inadvertent and accidental writes in that, the software algorithm must be issued prior to writing additional data to the device.

Software Algorithms

Selecting the software data protection mode requires the host system to precede datawrite operations by a series of three write operations to three specfic addresses. The three byte sequence opens the page write window enabling the host to write from from 1 to 256 bytes of data. Once the page load cycle has been completed, the device will automatically be returned to the data protected state
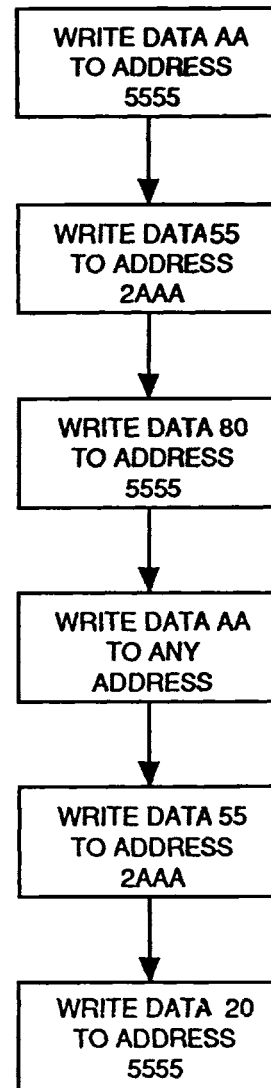
Software Data Protection Algorithm

Regardless of wheather the device has been protected or not, once the software data protected aglorithm is used and the data is written, the MEM8128 will automatically disable further writes unless another command is issued to cancel it. If no further commands are issued the MEM8128 will be write protected during power-down and any subsequent power-up.

```
WRITE DATA AA
TO ADDRESS
5555
      |
      v
WRITE DATA 55
TO ADDRESS
2AAA
      |
      v
WRITE DATA A0
TO ADDRESS
5555
      |
      v
WRITE DATA XX
TO ANY
ADDRESS
      |
      v
WRITE LAST
BYTE TO
LAST ADDRESS
      |
      v
AFTER t_wc
RE-ENTER DATA
PROTECTED STATE
```

Software Data Protect Disable

In the event the user wants to deactivate the software data protection feature for testing or reprogramming in an E²PROM programmer. The following six step algorithm will reset the internal protection circuit. After t_{wc}, the MEM8128 will be in standard operating mode.

```
WRITE DATA AA
TO ADDRESS
5555
      |
      v
WRITE DATA 55
TO ADDRESS
2AAA
      |
      v
WRITE DATA 80
TO ADDRESS
5555
      |
      v
WRITE DATA AA
TO ANY
ADDRESS
      |
      v
WRITE DATA 55
TO ADDRESS
2AAA
      |
      v
WRITE DATA 20
TO ADDRESS
5555
```

Package Details All dimensions in mm (inches). Tolerance on all dimensions +/- 0.254 (0.010).

32 Pin 0.1" Vertical-In Line (VIL™) "V"- Package
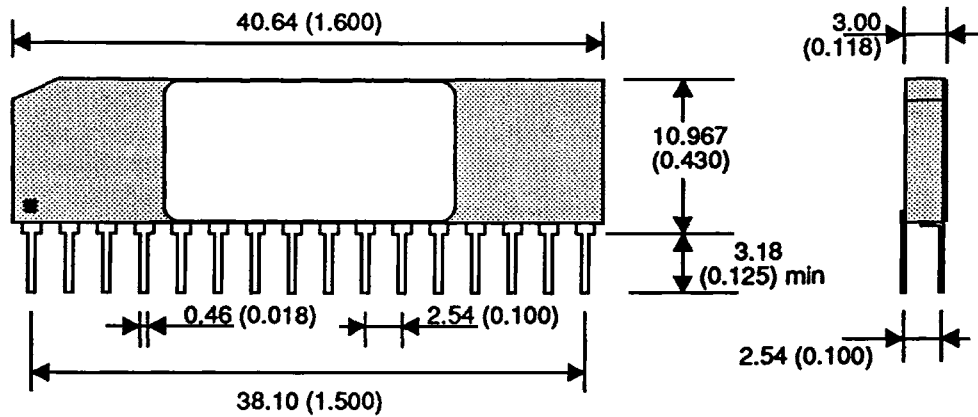
Ordering Information

MEM8128VMB-12

└──── Speed   12   = 120 ns
                                      15   = 150 ns
                                      20   = 200 ns

└──── Temp. range/screening   Blank = Commercial Temp.
                                          I   = Industrial Temp.
                                          M   = Military Temp.
                                          MB   = Processed to MIL-STD-883,
                                                          Method 5004, non compliant

└──── Packages   V   = Ceramic 0.1" VIL™

Note: For more information regarding screening levels, contact Mosaic Semiconductor Inc. for a 'Screening Level Applications Note.'