

MR16R1622(4/8/G)DF0
MR18R1622(4/8/G)DF0

Change History

| |
|---|
| Version 1.0 (July 2002) |
| <i>* First copy.</i> |
| <i>* Based on the 1.4 ver. (July 2002) 256/288Mbit A-die RIMM Datasheet</i> |

MR16R1622(4/8/G)DF0 MR18R1622(4/8/G)DF0

(16Mx16)*2(4/8/16)pcs RIMM™ Module based on 256Mb D-die, 32s banks,16K/32ms Ref, 2.5V
(16Mx18)*2(4/8/16)pcs RIMM™ Module based on 288Mb D-die, 32s banks,16K/32ms Ref, 2.5V

Overview

The RIMM™ module is a general purpose high- performance memory module suitable for use in a broad range of applications including computer memory, personal computers, workstations, and other applications where high bandwidth and low latency are required.

The RIMM module consists of 256/288Mb Direct RDRAM devices. These are extremely high-speed CMOS DRAMs organized as 16M words by 16 or 18 bits. The use of Rambus Signaling Level (RSL) technology permits up to 1066 MHz transfer rates while using conventional system and board design technologies. RDRAM devices are capable of sustained data transfers up to at 0.94 ns per two bytes (7.5ns per 16 bytes).

The RDRAM architecture enables the highest sustained bandwidth for multiple, simultaneous, randomly addressed, memory transactions. The separate control and data buses with independent row and column control yield over 95% bus efficiency. The RDRAM's 32-bank architecture supports up to four simultaneous transactions per device.

Features

- ◆ High speed up to 1066 MHz RDRAM storage
- ◆ 184 edge connector pads with 1mm pad spacing
- ◆ Module PCB size : 133.35mm x 31.75mm x 1.27mm (5.25" x 1.25" x 0.05") - 256Mb and 288Mb base PC800 RIMM
- ◆ Module PCB size : 133.35mm x 34.93mm x 1.27mm (5.25" x 1.375" x 0.05") - 256Mb and 288Mb base PC1066 RIMM
- ◆ Each RDRAM has 32 banks, for a total of 512, 256, 128, 64 banks on each 512/576MB, 256/288MB, 128/144MB, 64/72MB module respectively
- ◆ Gold plated edge connector pad contacts
- ◆ Serial Presence Detect (SPD) support
- ◆ Operates from a 2.5 volt supply (±5%)
- ◆ Powerdown self refresh modes
- ◆ Separate Row and Column buses for higher efficiency
- ◆ WBGa package (92 balls)

Key Timing Parameters/Part Numbers

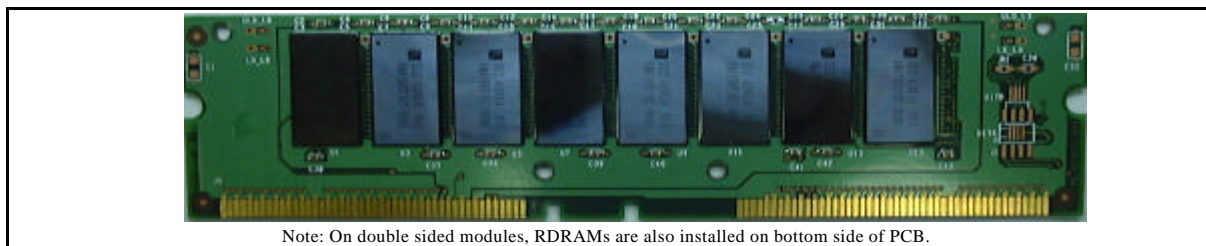
The following table lists the frequency and latency bins available for RIMM modules.

Table 1: Part Number by Freq. & Latency

| Organization | Speed | | | Part Number |
|--------------|-------|-----------------|---------------------------------------|---------------------|
| | Bin | I/O Freq. (MHz) | t _{RAC} (Row Access Time) ns | |
| 32M x 16/18 | -CT9 | 1066 | 32P | MR16/18R1622DF0-CT9 |
| | -CN9 | 1066 | 32 | MR16/18R1622DF0-CN9 |
| | -CM9 | 1066 | 35 | MR16/18R1622DF0-CM9 |
| | -CM8 | 800 | 40 | MR16/18R1622DF0-CM8 |
| | -CK8 | 800 | 45 | MR16/18R1622DF0-CK8 |
| 64M x 16/18 | -CT9 | 1066 | 32P | MR16/18R1624DF0-CT9 |
| | -CN9 | 1066 | 32 | MR16/18R1624DF0-CN9 |
| | -CM9 | 1066 | 35 | MR16/18R1624DF0-CM9 |
| | -CM8 | 800 | 40 | MR16/18R1624DF0-CM8 |
| | -CK8 | 800 | 45 | MR16/18R1624DF0-CK8 |
| 128M x 16/18 | -CT9 | 1066 | 32P | MR16/18R1628DF0-CT9 |
| | -CN9 | 1066 | 32 | MR16/18R1628DF0-CN9 |
| | -CM9 | 1066 | 35 | MR16/18R1628DF0-CM9 |
| | -CM8 | 800 | 40 | MR16/18R1628DF0-CM8 |
| | -CK8 | 800 | 45 | MR16/18R1628DF0-CK8 |
| 256M x 16/18 | -CT9 | 1066 | 32P | MR16/18R162GDF0-CT9 |
| | -CN9 | 1066 | 32 | MR16/18R162GDF0-CN9 |
| | -CM9 | 1066 | 35 | MR16/18R162GDF0-CM9 |
| | -CM8 | 800 | 40 | MR16/18R162GDF0-CM8 |
| | -CK8 | 800 | 45 | MR16/18R162GDF0-CK8 |

Form Factor

The RIMM modules are offered in 184-pad 1mm edge connector pad pitch suitable for 184 contact RIMM connectors. Figure 1 below, shows a sixteen device RIMM module.



Note: On double sided modules, RDRAMs are also installed on bottom side of PCB.

Figure 1: RIMM Module shown with heat spreader removed

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Table 2: Module Pad Numbers and Signal Names

| Pin | Pin Name | Pin | Pin Name |
|-----|----------|-----|----------|
| A1 | Gnd | B1 | Gnd |
| A2 | LDQA8 | B2 | LDQA7 |
| A3 | Gnd | B3 | Gnd |
| A4 | LDQA6 | B4 | LDQA5 |
| A5 | Gnd | B5 | Gnd |
| A6 | LDQA4 | B6 | LDQA3 |
| A7 | Gnd | B7 | Gnd |
| A8 | LDQA2 | B8 | LDQA1 |
| A9 | Gnd | B9 | Gnd |
| A10 | LDQA0 | B10 | LCFM |
| A11 | Gnd | B11 | Gnd |
| A12 | LCTMN | B12 | LCFMN |
| A13 | Gnd | B13 | Gnd |
| A14 | LCTM | B14 | NC |
| A15 | Gnd | B15 | Gnd |
| A16 | NC | B16 | LROW2 |
| A17 | Gnd | B17 | Gnd |
| A18 | LROW1 | B18 | LROW0 |
| A19 | Gnd | B19 | Gnd |
| A20 | LCOL4 | B20 | LCOL3 |
| A21 | Gnd | B21 | Gnd |
| A22 | LCOL2 | B22 | LCOL1 |
| A23 | Gnd | B23 | Gnd |
| A24 | LCOL0 | B24 | LDQB0 |
| A25 | Gnd | B25 | Gnd |
| A26 | LDQB1 | B26 | LDQB2 |
| A27 | Gnd | B27 | Gnd |
| A28 | LDQB3 | B28 | LDQB4 |
| A29 | Gnd | B29 | Gnd |
| A30 | LDQB5 | B30 | LDQB6 |
| A31 | Gnd | B31 | Gnd |
| A32 | LDQB7 | B32 | LDQB8 |
| A33 | Gnd | B33 | Gnd |
| A34 | LSCK | B34 | LCMD |
| A35 | Vcmos | B35 | Vcmos |
| A36 | SOUT | B36 | SIN |
| A37 | Vcmos | B37 | Vcmos |
| A38 | NC | B38 | NC |
| A39 | Gnd | B39 | Gnd |
| A40 | NC | B40 | NC |
| A41 | Vdd | B41 | Vdd |
| A42 | Vdd | B42 | Vdd |
| A43 | NC | B43 | NC |
| A44 | NC | B44 | NC |
| A45 | NC | B45 | NC |
| A46 | NC | B46 | NC |

| Pin | Pin Name | Pin | Pin Name |
|-----|----------|-----|----------|
| A47 | NC | B47 | NC |
| A48 | NC | B48 | NC |
| A49 | NC | B49 | NC |
| A50 | NC | B50 | NC |
| A51 | Vref | B51 | Vref |
| A52 | Gnd | B52 | Gnd |
| A53 | SCL | B53 | SA0 |
| A54 | Vdd | B54 | Vdd |
| A55 | SDA | B55 | SA1 |
| A56 | SVdd | B56 | SVdd |
| A57 | SWP | B57 | SA2 |
| A58 | Vdd | B58 | Vdd |
| A59 | RSCK | B59 | RCMD |
| A60 | Gnd | B60 | Gnd |
| A61 | RDQB7 | B61 | RDQB8 |
| A62 | Gnd | B62 | Gnd |
| A63 | RDQB5 | B63 | RDQB6 |
| A64 | Gnd | B64 | Gnd |
| A65 | RDQB3 | B65 | RDQB4 |
| A66 | Gnd | B66 | Gnd |
| A67 | RDQB1 | B67 | RDQB2 |
| A68 | Gnd | B68 | Gnd |
| A69 | RCOL0 | B69 | RDQB0 |
| A70 | Gnd | B70 | Gnd |
| A71 | RCOL2 | B71 | RCOL1 |
| A72 | Gnd | B72 | Gnd |
| A73 | RCOL4 | B73 | RCOL3 |
| A74 | Gnd | B74 | Gnd |
| A75 | RRROW1 | B75 | RRROW0 |
| A76 | Gnd | B76 | Gnd |
| A77 | NC | B77 | RRROW2 |
| A78 | Gnd | B78 | Gnd |
| A79 | RCTM | B79 | NC |
| A80 | Gnd | B80 | Gnd |
| A81 | RCTMN | B81 | RCFMN |
| A82 | Gnd | B82 | Gnd |
| A83 | RDQA0 | B83 | RCFM |
| A84 | Gnd | B84 | Gnd |
| A85 | RDQA2 | B85 | RDQA1 |
| A86 | Gnd | B86 | Gnd |
| A87 | RDQA4 | B87 | RDQA3 |
| A88 | Gnd | B88 | Gnd |
| A89 | RDQA6 | B89 | RDQA5 |
| A90 | Gnd | B90 | Gnd |
| A91 | RDQA8 | B91 | RDQA7 |
| A92 | Gnd | B92 | Gnd |

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Table 3: Module Connector Pad Description

| Signal | Pins | I/O | Type | Description |
|------------------|--|-----|-------------------|---|
| Gnd | A1, A3, A5, A7, A9, A11, A13, A15, A17, A19, A21, A23, A25, A27, A29, A31, A33, A39, A52, A60, A62, A64, A66, A68, A70, A72, A74, A76, A78, A80, A82, A84, A86, A88, A90, A92, B1, B3, B5, B7, B9, B11, B13, B15, B17, B19, B21, B23, B25, B27, B29, B31, B33, B39, B52, B60, B62, B64, B66, B68, B70, B72, B74, B76, B78, B80, B82, B84, B86, B88, B90, B92 | | | Ground reference for RDRAM core and interface. 72 PCB connector pads. |
| LCFM | B10 | I | RSL | Clock from master. Interface clock used for receiving RSL signals from the Channel. Positive polarity. |
| LCFMN | B12 | I | RSL | Clock from master. Interface clock used for receiving RSL signals from the Channel. Negative polarity. |
| LCMD | B34 | I | V _{CMOS} | Serial Command used to read from and write to the control registers. Also used for power management. |
| LCOL4.. LCOL0 | A20, B20, A22, B22, A24 | I | RSL | Column bus. 5-bit bus containing control and address information for column accesses. |
| LCTM | A14 | I | RSL | Clock to master. Interface clock used for transmitting RSL signals to the Channel. Positive polarity. |
| LCTMN | A12 | I | RSL | Clock to master. Interface clock used for transmitting RSL signals to the Channel. Negative polarity. |
| LDQA8.. LDQA0 | A2, B2, A4, B4, A6, B6, A8, B8, A10 | I/O | RSL | Data bus A. A 9-bit bus carrying a byte of read or write data between the Channel and the RDRAM. LDQA8 is non-functional on modules with x16 RDRAM devices |
| LDQB8.. LDQB0 | B32, A32, B30, A30, B28, A28, B26, A26, B24 | I/O | RSL | Data bus B. A 9-bit bus carrying a byte of read or write data between the Channel and the RDRAM. LDQB8 is non-functional on modules with x16 RDRAM devices. |
| LROW2.. LROW0 | B16, A18, B18 | I | RSL | Row bus. 3-bit bus containing control and address information for row accesses. |
| LSCK | A34 | I | V _{CMOS} | Serial Clock input. Clock source used to read from and write to the RDRAM control registers. |
| NC | A16, B14, A38, B38, A40, B40, A43, B43, A44, B44, A45, B45, A46, B46, A47, B47, A48, B48, A49, B49, A50, B50, A77, B79 | | | These pads are not connected. These 24 connector pads are reserved for future use. |
| RCFM | B83 | I | RSL | Clock from master. Interface clock used for receiving RSL signals from the Channel. Positive polarity. |
| RCFMN | B81 | I | RSL | Clock from master. Interface clock used for receiving RSL signals from the Channel. Negative polarity. |
| RCMD | B59 | I | V _{CMOS} | Serial Command Input. Pin used to read from and write to the control registers. Also used for power management. |

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| Signal | Pins | I/O | Type | Description |
|-------------------|---|-----|-------------------|--|
| RCOL4.. RCOL0 | A73, B73, A71, B71, A69 | I | RSL | Column bus. 5-bit bus containing control and address information for column accesses. |
| RCTM | A79 | I | RSL | Clock to master. Interface clock used for transmitting RSL signals to the Channel. Positive polarity. |
| RCTMN | A81 | I | RSL | Clock to master. Interface clock used for transmitting RSL signals to the Channel. Negative polarity. |
| RDQA8.. RDQA0 | A91, B91, A89, B89, A87, B87, A85, B85, A83 | I/O | RSL | Data bus A. A 9-bit bus carrying a byte of read or write data between the Channel and the RDRAM. RDQA8 is non-functional on modules x16 RDRAM devices. |
| RDQB8.. RDQB0 | B61, A61, B63, A63, B65, A65, B67, A67, B69 | I/O | RSL | Data bus B. A 9-bit bus carrying a byte of read or write data between the Channel and the RDRAM. RDQB8 is non-functional on modules x16 RDRAM devices. |
| RROW2.. RROW0 | B77, A75, B75 | I | RSL | Row bus. 3-bit bus containing control and address information for row accesses. |
| RSCK | A59 | I | V _{CMOS} | Serial Clock input. Clock source used to read from and write to the RDRAM control registers. |
| SA0 | B53 | I | SV _{DD} | Serial Presence Detect Address 0. |
| SA1 | B55 | I | SV _{DD} | Serial Presence Detect Address 1. |
| SA2 | B57 | I | SV _{DD} | Serial Presence Detect Address 2. |
| SCL | A53 | I | SV _{DD} | Serial Presence Detect Clock. |
| SDA | A55 | I/O | SV _{DD} | Serial Presence Detect Data (Open Collector I/O). |
| SIN | B36 | I/O | V _{CMOS} | Serial I/O for reading from and writing to the control registers. Attaches to SIO0 of the first RDRAM on the module. |
| SOUT | A36 | I/O | V _{CMOS} | Serial I/O for reading from and writing to the control registers. Attaches to SIO1 of the last RDRAM on the module. |
| SV _{DD} | A56, B56 | | | SPD Voltage. Used for signals SCL, SDA, SWE, SA0, SA1 and SA2. |
| SWP | A57 | I | SV _{DD} | Serial Presence Detect Write Protect (active high). When low, the SPD can be written as well as read. |
| V _{CMOS} | A35, B35, A37, B37 | | | CMOS I/O Voltage. Used for signals CMD, SCK, SIN, SOUT. |
| V _{dd} | A41, A42, A54, A58, B41, B42, B54, B58 | | | Supply voltage for the RDRAM core and interface logic. |
| V _{ref} | A51, B51 | | | Logic threshold reference voltage for RSL signals. |

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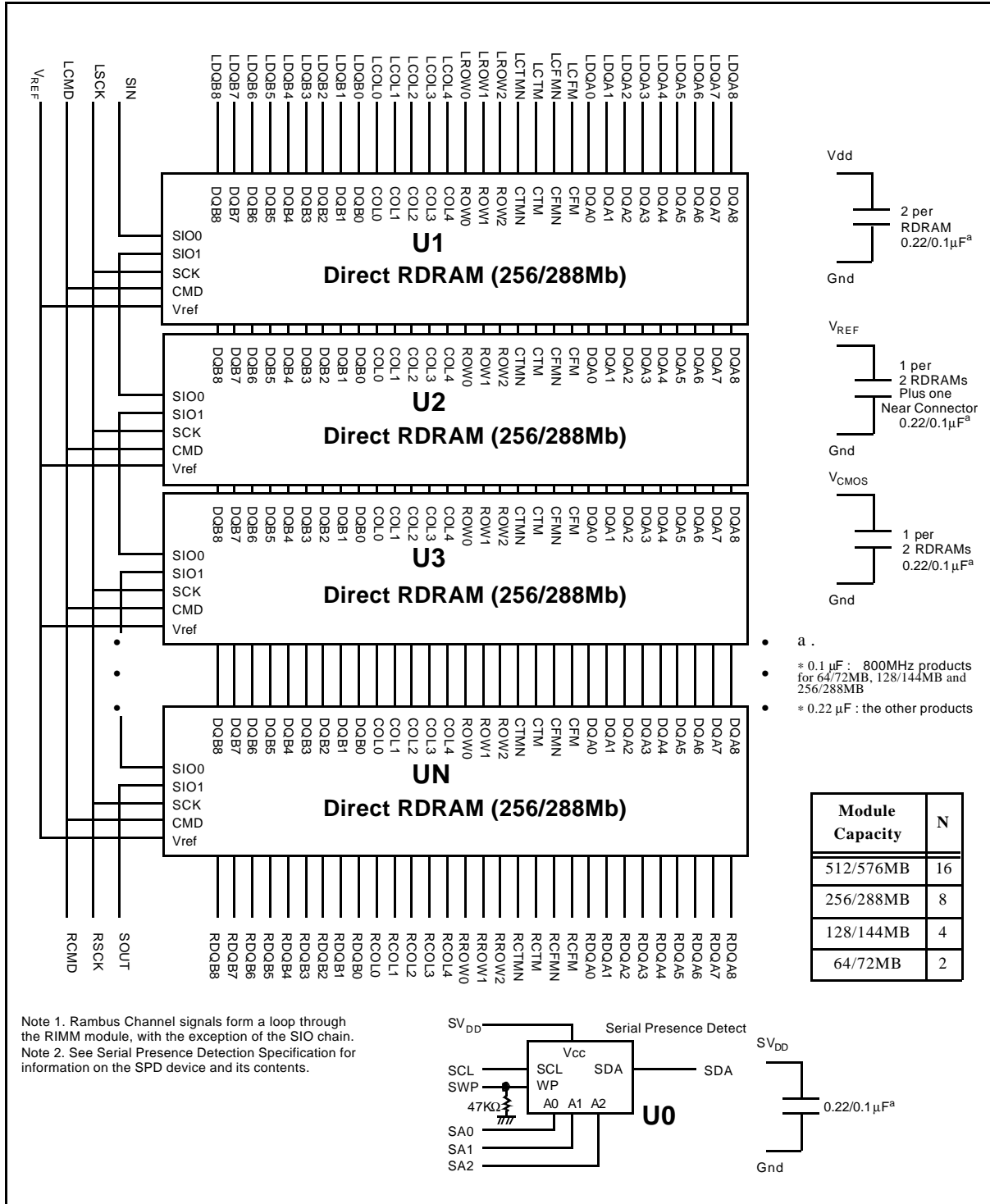


Figure 2: RIMM Module Functional Diagram

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Absolute Maximum Ratings

Table 4: Absolute Maximum Ratings

| Symbol | Parameter | Min | Max | Unit |
|---------------------|---|-------|-----------------------|------|
| V _{I,ABS} | Voltage applied to any RSL or CMOS signal pad with respect to Gnd | - 0.3 | V _{DD} + 0.3 | V |
| V _{DD,ABS} | Voltage on VDD with respect to Gnd | - 0.5 | V _{DD} + 1.0 | V |
| T _{STORE} | Storage temperature | - 50 | 100 | °C |
| T _{PLATE} | Plate temperature | - | 92 | °C |

DC Recommended Electrical Conditions

Table 5: DC Recommended Electrical Conditions

| Symbol | Parameter and Conditions | Min | Max | Unit |
|-------------------|--|------------------------------|------------------------------|--------|
| V _{DD} | Supply voltage | 2.50 - 0.13 | 2.50 + 0.13 | V |
| V _{CMOS} | CMOS I/O power supply at pad for 2.5V controllers: CMOS I/O power supply at pad for 1.8V controllers: | V _{DD} 1.8 - 0.1 | V _{DD} 1.8 + 0.2 | V V |
| V _{REF} | Reference voltage | 1.4 - 0.2 | 1.4 + 0.2 | V |
| V _{SPD} | Serial Presence Detector- Positive power supply | 2.2 | 3.6 | V |

Table 6: RIMM Module Capacity and Number of RDRAM device

| RIMM Module Capacity: | 512/576MB | 256/288MB | 128/144MB | 64/72MB |
|-----------------------------------|-----------|-----------|-----------|---------|
| Number of 256/288Mb RDRAM devices | 16 | 8 | 4 | 2 |

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RIMM Module Current Profile

Table 7: RIMM Module Current Profile

| I _{DD} | RIMM Module Capacity | | 512/576MB | 256/288MB | 128/144MB | 64/72MB | Unit |
|------------------|--|-------|----------------------|-----------|-----------|---------|------|
| | Number of 256/288Mb RDRAMs | | 16 | 8 | 4 | 2 | |
| | RIMM Module power conditions ^a | Freq | Max | Max | Max | Max | |
| I _{DD1} | One RDRAM in Read ^b , balance in NAP mode | -1066 | 710/760 ^c | 678/728 | 662/712 | 654/704 | mA |
| | | -800 | 590/620 | 558/588 | 542/572 | 534/564 | |
| I _{DD2} | One RDRAM in Read ^b , balance in Standby mode | -1066 | 2150/2200 | 1350/1400 | 950/1000 | 750/800 | mA |
| | | -800 | 1730/1760 | 1090/1120 | 770/800 | 610/640 | |
| I _{DD3} | One RDRAM in Read ^b , balance in Active mode | -1066 | 2900/2950 | 1700/1750 | 1100/1150 | 800/850 | mA |
| | | -800 | 2330/2360 | 1370/1400 | 890/920 | 650/680 | |
| I _{DD4} | One RDRAM in Write, balance in NAP mode | -1066 | 790/850 | 758/818 | 742/802 | 734/794 | mA |
| | | -800 | 635/680 | 603/648 | 587/632 | 579/624 | |
| I _{DD5} | One RDRAM in Write, balance in Standby mode | -1066 | 2230/2290 | 1430/1490 | 1030/1090 | 830/890 | mA |
| | | -800 | 1775/1820 | 1135/1180 | 815/860 | 655/700 | |
| I _{DD6} | One RDRAM in Write, balance in Active mode | -1066 | 2980/3040 | 1780/1840 | 1180/1240 | 880/940 | mA |
| | | -800 | 2375/2420 | 1415/1460 | 935/980 | 695/740 | |

a. Actual power will depend on memory controller and usage patterns. Power does not include Refresh Current.

b. I/O current is a function of the % of 1's, to add I/O power for 50% 1's for a X16 need to add 257mA or 290mA for X18 ECC module for the following:

$$V_{DD} = 2.5V, V_{TERM} = 1.8V, V_{REF} = 1.4V \text{ and } V_{DIL} = V_{REF} - 0.5V.$$

c. Current values represent X16(Non-Ecc) / X18(Ecc)

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AC Electrical Specifications

Table 8: AC Electrical Specifications

| Symbol | Parameter and Conditions | Min | Typ | Max | Unit |
|-------------------------|--|------|-----|----------------------------|----------|
| Z_L | Module Impedance of RSL Signals | 25.2 | 28 | 30.8 | Ω |
| $Z_{UL-CMOS}$ | Module Impedance of SCK and CMOS signals | 23.8 | 28 | 32.2 | Ω |
| T_{PD} | Propagation Delay variation of RSL signals. Average clock delay from finger to finger of all RSL clock nets (CTM, CTMN, CFM, and CFMN) | - | | See Table10 ^{a,b} | ns |
| ΔT_{PD} | Propagation delay variation of RSL signals with respect to T_{PD} ^{b,c} for 2, 4, and 8 device modules | -21 | | 21 | ps |
| | Propagation delay variation of RSL signals with respect to T_{PD} ^{b,c} for 16 device modules | -24 | | 24 | ps |
| $\Delta T_{PD-CMOS}$ | Propagation delay variation of SCK signals with respect to an average clock delay | -250 | | 250 | ps |
| $\Delta T_{PD-SCK,CMD}$ | Propagation delay variation of CMD signals with respect to SCK signal | -200 | | 200 | ps |
| V_{α}/V_{IN} | Attenuation Limit | | | See Table10 ^a | % |
| V_{XF}/V_{IN} | Forward crosstalk coefficient (300ps input rise time @ 20%-80%) | | | See Table10 ^a | % |
| V_{XB}/V_{IN} | Backward crosstalk coefficient (300ps input rise time @ 20%-80%) | | | See Table10 ^a | % |

a. Table 10 lists parameters and specifications for different storage capacity RIMM Modules that use 256Mb or 288Mb RDRAM devices.

b. T_{PD} or Average clock delay is defined as the delay from finger to finger of RSL signal.

c. If the RIMM module meets the following specification, then it is compliant to the specification. If the RIMM module does not meet these specifications, then the specification can be adjusted by the "Adjusted ΔT_{PD} Specification" table 9 below.

Adjusted ΔT_{PD} Specification

Table 9: Adjusted ΔT_{PD} Specification

| Symbol | Parameter and Conditions | Adjusted Min/Max | Absolute Min / Max | | Unit |
|-----------------|---|-------------------------------|--------------------|----|------|
| ΔT_{PD} | Propagation delay variation of RSL signals with respect to T_{PD} for 2, 4 and 8 device modules | $\pm/[20+(18*N*\Delta Z0)]^a$ | -30 | 30 | ps |
| | Propagation delay variation of RSL signals with respect to T_{PD} for 16 device modules | $\pm/[24+(18*N*\Delta Z0)]^a$ | -50 | 50 | ps |

a. Where: N = Number of RDRAM devices installed on the RIMM module

$\Delta Z0 = \text{delta } Z0\% = (\text{max } Z0 - \text{min } Z0)/(\text{min } Z0)$

(max Z0 and min Z0 are obtained from the loaded (high impedance) impedance coupons of all RSL layers on the modules)

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AC Electrical Specifications for RIMM Modules

Table 10: AC Electrical Specifications for RIMM Modules

| Symbol | RIMM Module Capacity | | 512/576MB | 256/288MB | 128/144MB | 64/72MB | Unit |
|----------------------------------|---|-------|-----------|-----------|-----------|---------|------|
| | Number of 256/288Mb RDRAMs | | 16 | 8 | 4 | 2 | |
| | Parameter and Condition for RIMM Modules | Freq. | Max | Max | Max | Max | |
| T _{PD} | Propagation Delay, all RSL signals | -1066 | 2.11 | 1.56 | 1.56 | 1.56 | ns |
| | | -800 | 2.11 | 1.56 | 1.56 | 1.56 | |
| V _α /V _{IN} | Attenuation Limit | -1066 | 27.0 | 17.0 | 17.0 | 17.0 | % |
| | | -800 | 25.0 | 16.0 | 16.0 | 16.0 | |
| V _{XF} /V _{IN} | Forward crosstalk coefficient (300ps input rise time @ 20%-80%) | -1066 | 8.0 | 4.0 | 4.0 | 4.0 | % |
| | | -800 | 8.0 | 4.0 | 4.0 | 4.0 | |
| V _{XB} /V _{IN} | Backward crosstalk coefficient (300ps input rise time @ 20%-80%) | -1066 | 2.5 | 2.0 | 2.0 | 2.0 | % |
| | | -800 | 2.5 | 2.0 | 2.0 | 2.0 | |
| R _{DC} | DC Resistance Limit | -1066 | 1.2 | 0.8 | 0.6 | 0.6 | Ω |
| | | -800 | 1.2 | 0.8 | 0.6 | 0.6 | |

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Physical Dimensions -1 (For PCB)

The following defines the RIMM module dimensions. All units are in millimeters with inches in brackets [], where appropriate. The dimensions without tolerance specification use the default tolerance of $\pm 0.127[\pm 0.005]$.

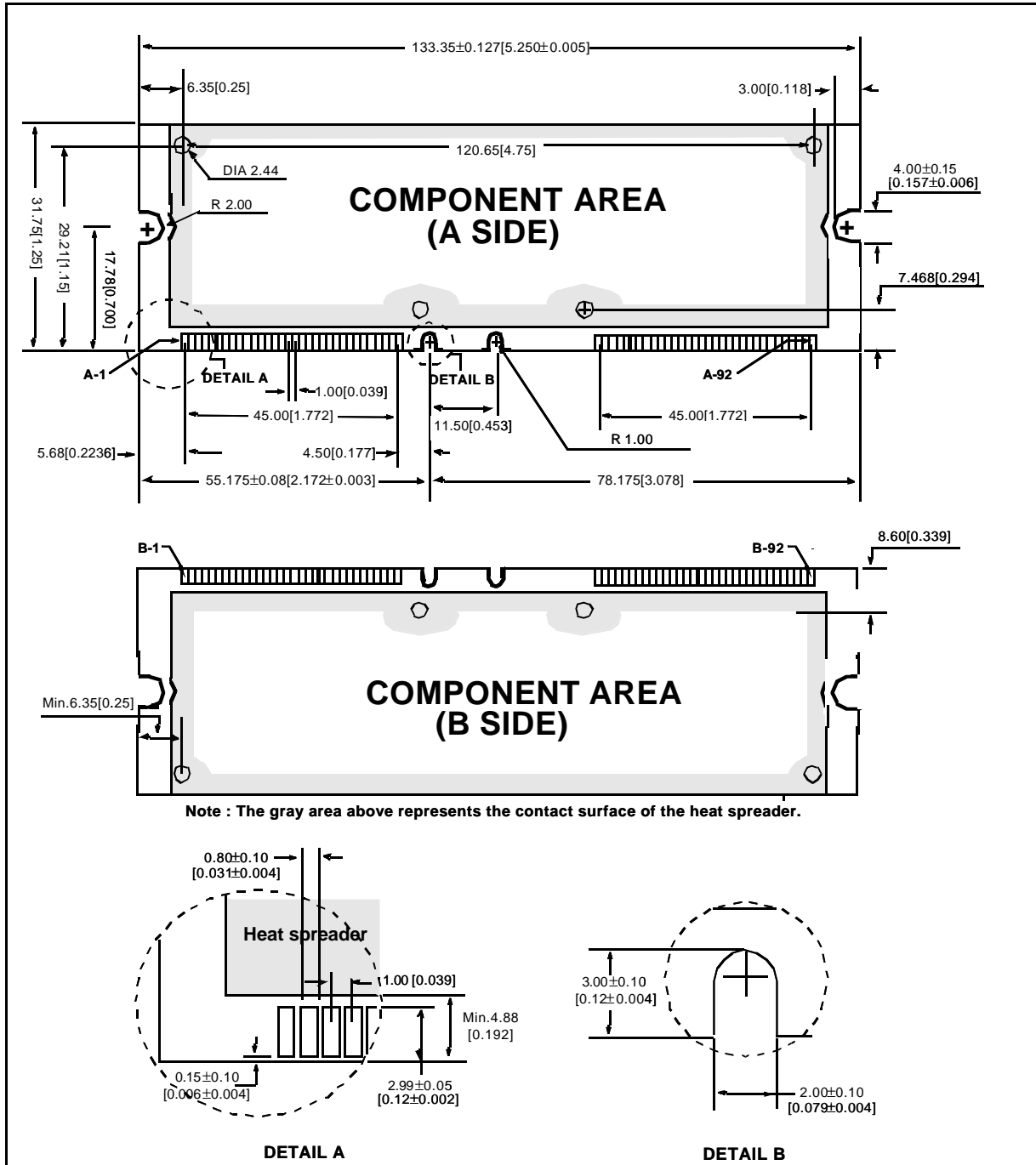


Figure 3: 256Mb/288Mb base RIMM Module PCB Physical Dimensions

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Physical Dimensions -2 (For PCB)

The following defines the RIMM module dimensions. All units are in millimeters with inches in brackets [], where appropriate. The dimensions without tolerance specification use the default tolerance of $\pm 0.127[\pm 0.005]$.

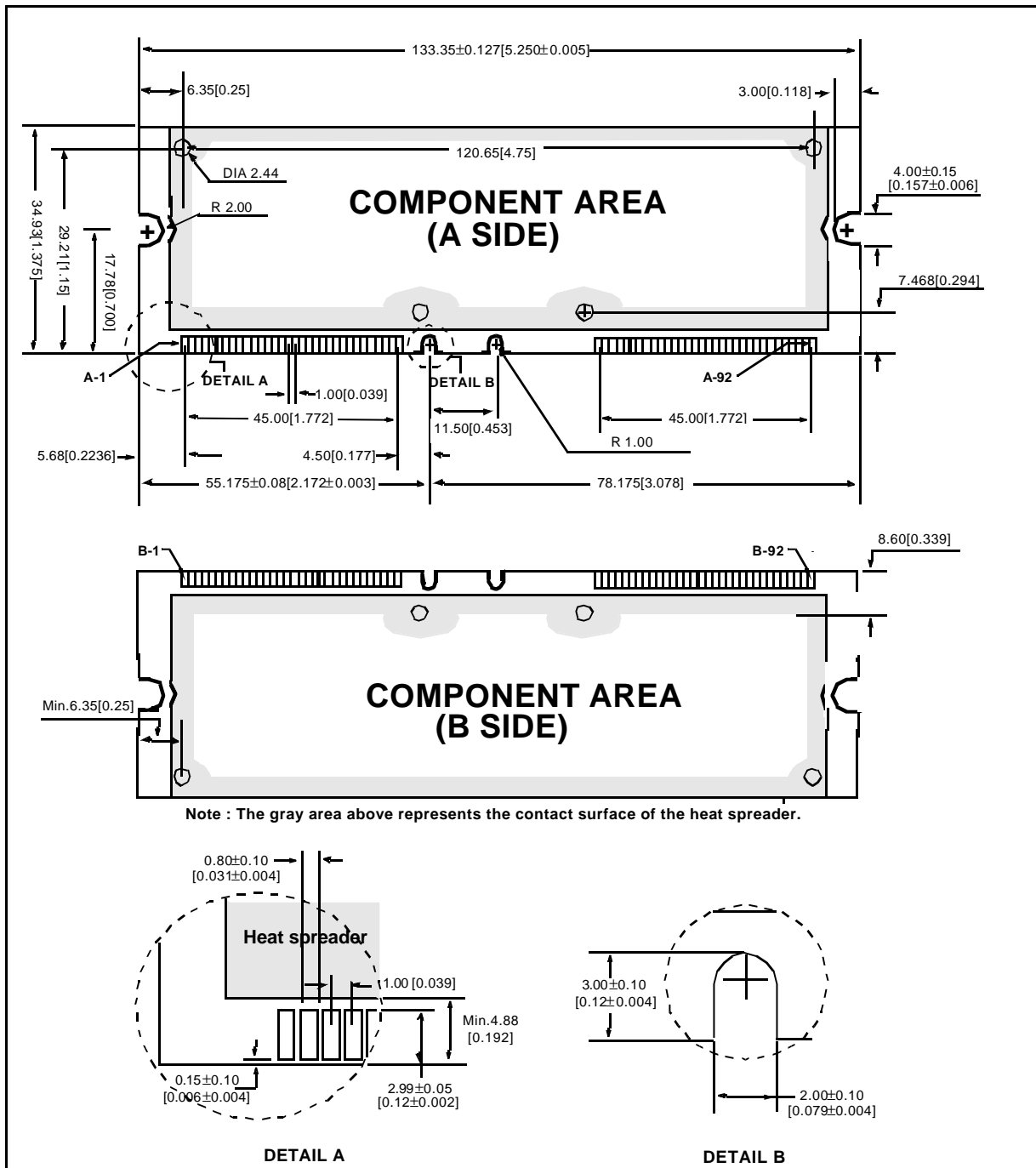


Figure 4: 256Mb/288Mb base RIMM Module PCB Physical Dimensions

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Physical Dimensions -3 (For Heat Spreader)

The following defines the RIMM module dimensions. All units are in millimeters with inches in brackets [], where appropriate. The dimensions without tolerance specification use the default tolerance of $\pm 0.127[\pm 0.005]$.

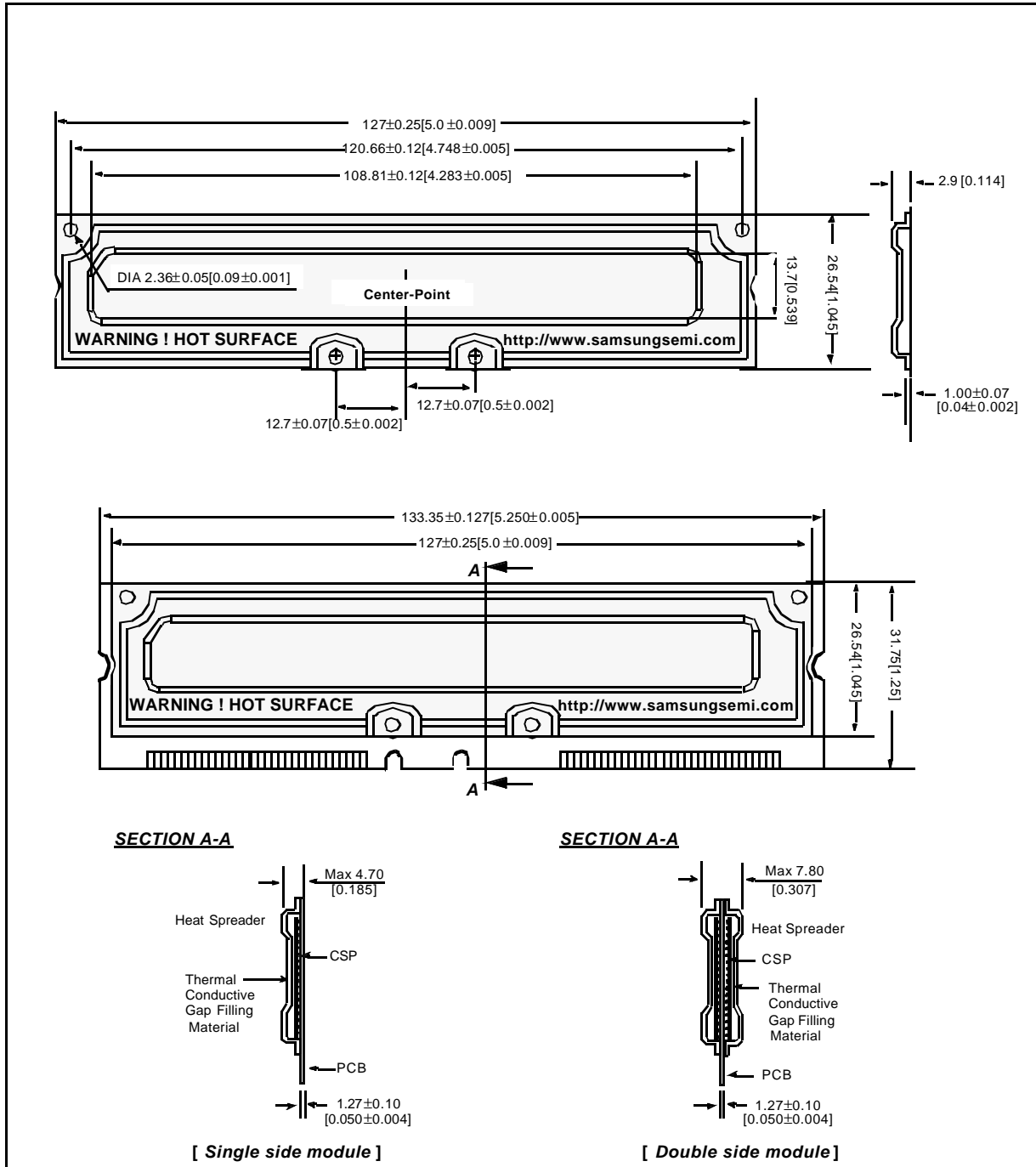


Figure 5: 256Mb/288Mb base Heat Spreader Physical Dimensions

MR16R1622(4/8/G)DF0 MR18R1622(4/8/G)DF0

Physical Dimensions -4 (For Heat Spreader)

The following defines the RIMM module dimensions. All units are in millimeters with inches in brackets [], where appropriate. The dimensions without tolerance specification use the default tolerance of $\pm 0.127[\pm 0.005]$.

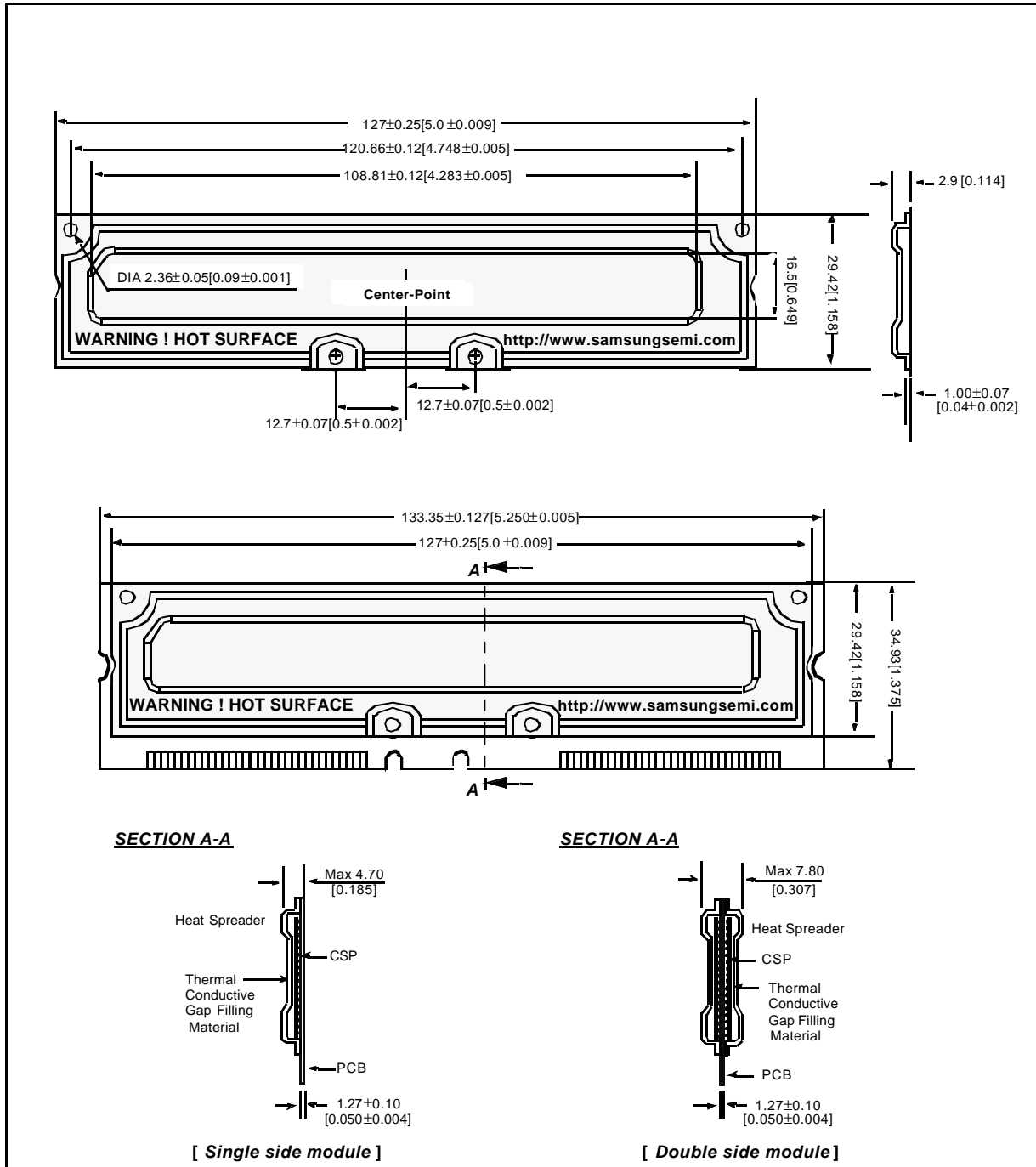


Figure 6: 256Mb/288Mb base Heat Spreader Physical Dimensions

MR16R1622(4/8/G)DF0 MR18R1622(4/8/G)DF0

Standard RIMM Module Marking

The RIMM modules available from Samsung are marked like Figure 7 below. This marking also assists users to specify and verify if the correct RIMM modules are installed in their systems. In the diagram, a label is shown attached to

the RIMM module's heat spreader. Information contained on the label is specific to the RIMM module and provides RDRAM information without requiring removal of the RIMM module's heat spreader.

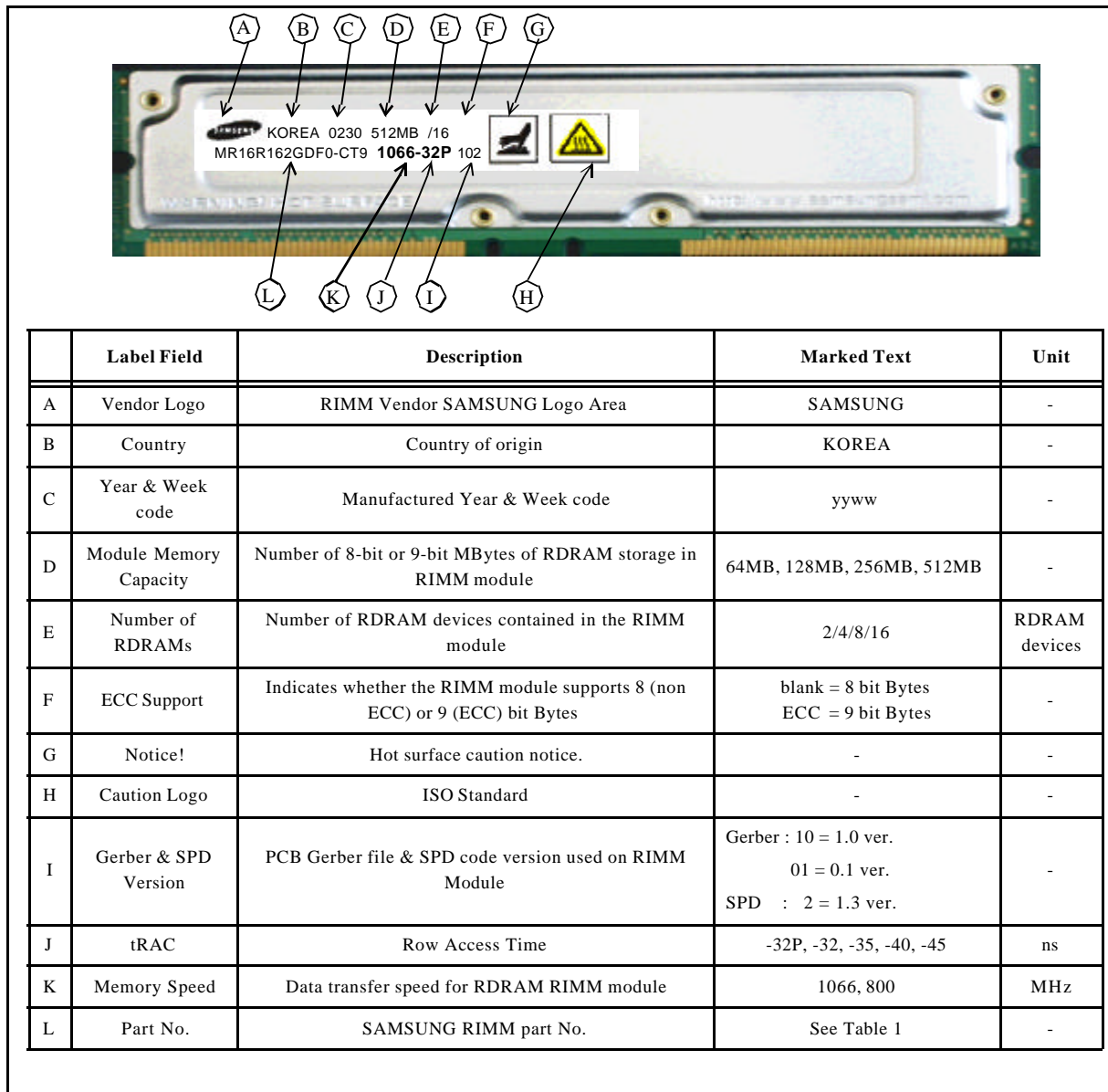


Figure 7: RIMM Marking Example

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