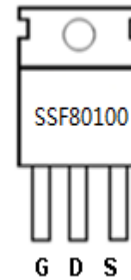
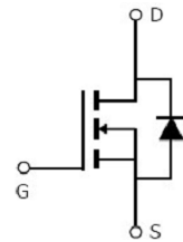


**Main Product Characteristics:**

$V_{DSS}$	75V
$R_{DS(on)}$	8m $\Omega$ (typ.)
$I_D$	80A <sup>①</sup>


**TO220**

**Marking and pin Assignment**

**Schematic diagram**
**Features and Benefits:**

- Advanced MOSFET process technology
- Special designed for motor control, PWM, load switching etc.
- Ultra low on-resistance with low gate charge
- Excellent Qgd/Qgs rating
- Fast switching and reverse body recovery
- 175°C operating temperature


**Description:**

It utilizes the latest processing techniques to achieve the high cell density and reduces the on-resistance with high repetitive avalanche rating. These features combine to make this design an extremely efficient and reliable device for use in power switching application, motor control and a wide variety of other applications.

**Absolute max Rating:**

Symbol	Parameter	Max.	Units
$I_D @ TC = 25^\circ C$	Continuous Drain Current, $V_{GS} @ 10V$	80 <sup>①</sup>	A
$I_D @ TC = 100^\circ C$	Continuous Drain Current, $V_{GS} @ 10V$	70 <sup>①</sup>	
$I_{DM}$	Pulsed Drain Current <sup>②</sup>	320	
$P_D @ TC = 25^\circ C$	Power Dissipation <sup>③</sup>	200	W
	Linear Derating Factor	2.0	W/°C
$V_{DS}$	Drain-Source Voltage	75	V
$V_{GS}$	Gate-to-Source Voltage	$\pm 20$	V
$E_{AS}$	Single Pulse Avalanche Energy @ L=0.3mH	375	mJ
$I_{AS}$	Avalanche Current @ L=0.3mH	50	A
$T_J T_{STG}$	Operating Junction and Storage Temperature Range	-55 to + 175	°C

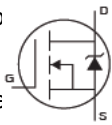
## Thermal Resistance

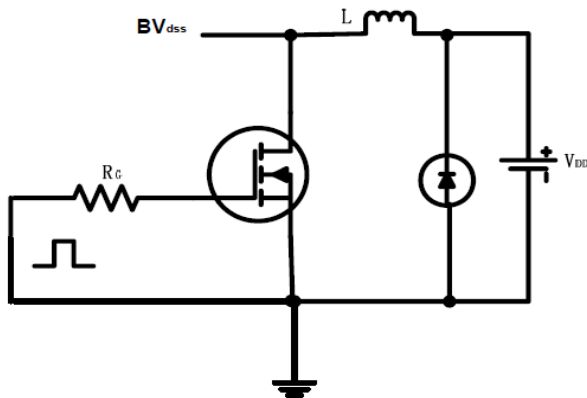
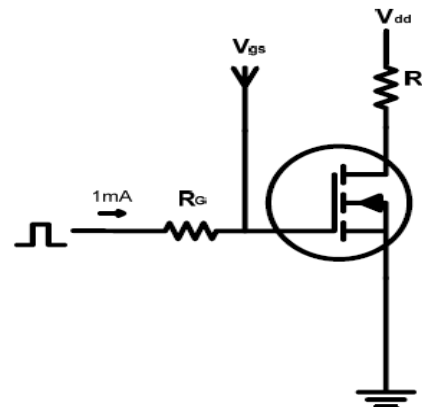
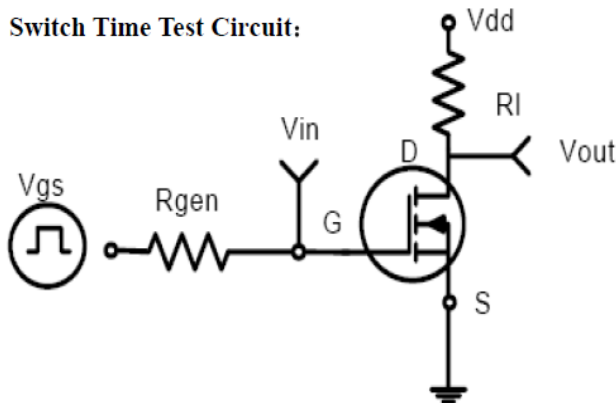
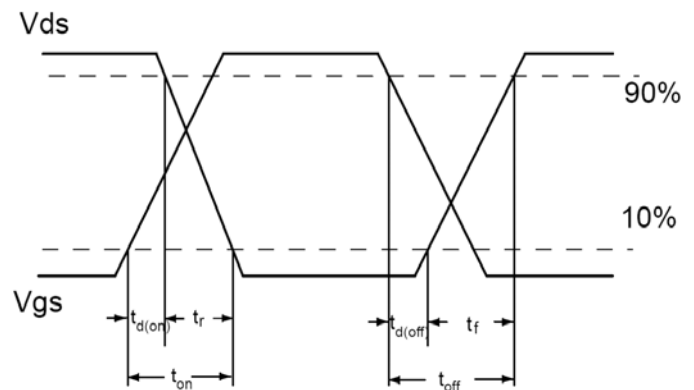
Symbol	Characterizes	Typ.	Max.	Units
R <sub>θJC</sub>	Junction-to-case ③	—	0.75	°C/W
R <sub>θJA</sub>	Junction-to-ambient (t ≤ 10s) ④	—	62	°C/W
	Junction-to-Ambient (PCB mounted, steady-state) ④	—	40	°C/W

## Electrical Characterizes @T<sub>A</sub>=25°C unless otherwise specified

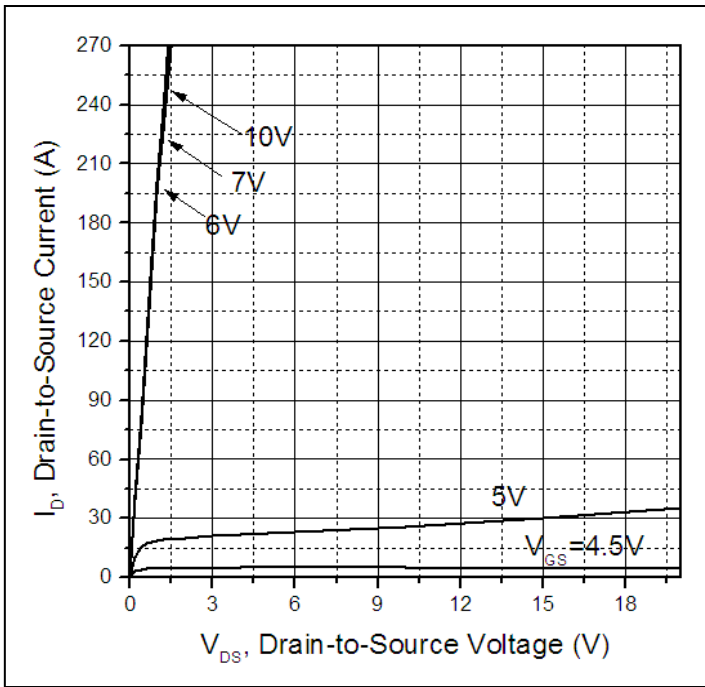
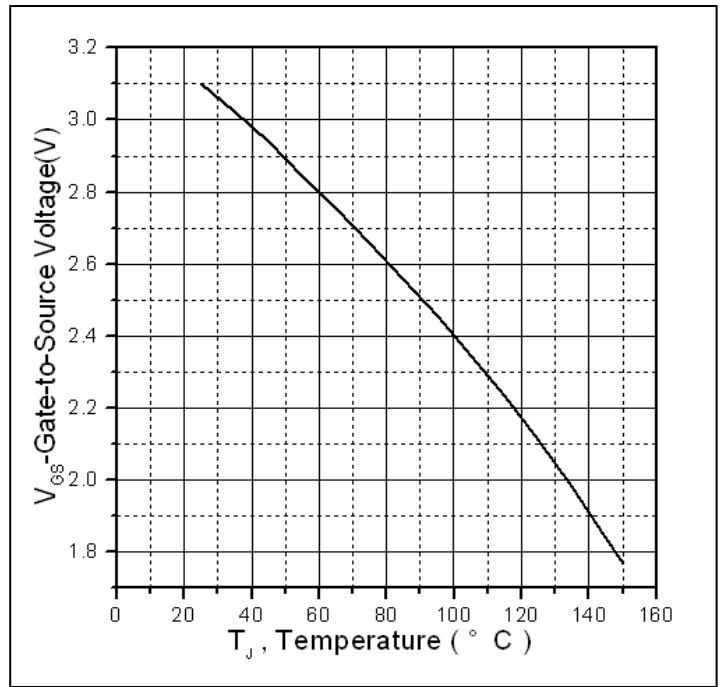
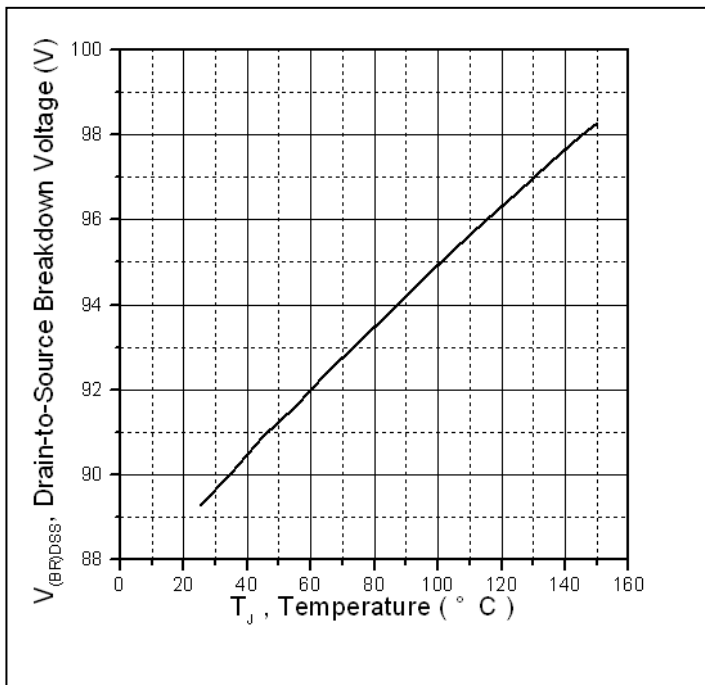
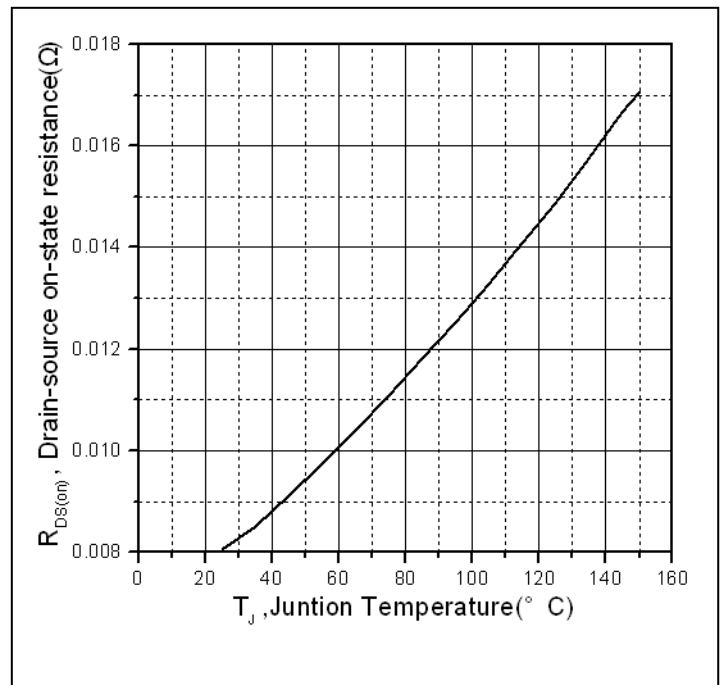
Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
V <sub>(BR)DSS</sub>	Drain-to-Source breakdown voltage	75	—	—	V	V <sub>GS</sub> = 0V, I <sub>D</sub> = 250μA
R <sub>DS(on)</sub>	Static Drain-to-Source on-resistance	—	8	10	mΩ	V <sub>GS</sub> =10V, I <sub>D</sub> = 30A T <sub>J</sub> = 125°C
		—	14.9	—		
V <sub>GS(th)</sub>	Gate threshold voltage	2	—	4	V	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = 250μA T <sub>J</sub> = 125°C
		—	2.11	—		
I <sub>DSS</sub>	Drain-to-Source leakage current	—	—	1	μA	V <sub>DS</sub> = 75V, V <sub>GS</sub> = 0V T <sub>J</sub> = 125°C
		—	—	50		
I <sub>GSS</sub>	Gate-to-Source forward leakage	—	—	100	nA	V <sub>GS</sub> = 20V V <sub>GS</sub> = -20V
		—	—	-100		
Q <sub>g</sub>	Total gate charge	—	73	—	nC	I <sub>D</sub> = 30A, V <sub>DS</sub> =30V, V <sub>GS</sub> = 10V
Q <sub>gs</sub>	Gate-to-Source charge	—	29	—		
Q <sub>gd</sub>	Gate-to-Drain("Miller") charge	—	23	—		
t <sub>d(on)</sub>	Turn-on delay time	—	19	—	ns	V <sub>GS</sub> =10V, V <sub>DS</sub> =30V, R <sub>L</sub> =15Ω, R <sub>GEN</sub> =2.5Ω
t <sub>r</sub>	Rise time	—	18	—		
t <sub>d(off)</sub>	Turn-Off delay time	—	56	—		
t <sub>f</sub>	Fall time	—	24	—		
C <sub>iss</sub>	Input capacitance	—	4308	—	pF	V <sub>GS</sub> = 0V V <sub>DS</sub> = 25V f = 1MHz
C <sub>oss</sub>	Output capacitance	—	328	—		
C <sub>rss</sub>	Reverse transfer capacitance	—	118	—		

## Source-Drain Ratings and Characteristics

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
I <sub>S</sub>	Continuous Source Current (Body Diode)	—	—	80 ①	A	MOSFET symb showing the integral reverse p-n junction diode. 
I <sub>SM</sub>	Pulsed Source Current (Body Diode)	—	—	320	A	
V <sub>SD</sub>	Diode Forward Voltage	—	0.88	1.3	V	I <sub>S</sub> =30A, V <sub>GS</sub> =0V
t <sub>rr</sub>	Reverse Recovery Time	—	36	—	ns	T <sub>J</sub> = 25°C, I <sub>F</sub> = 75A, di/dt =
Q <sub>rr</sub>	Reverse Recovery Charge	—	50	—	nC	100A/μs

**Test circuits and Waveforms**
**EAS test circuits:**

**Gate charge test circuit:**

**Switch Time Test Circuit:**

**Switch Waveforms:**

**Notes:**

- ① Calculated continuous current based on maximum allowable junction temperature. Package limitation current is 75A.
- ② Repetitive rating; pulse width limited by max. junction temperature.
- ③ The power dissipation PD is based on max. junction temperature, using junction-to-case thermal resistance.
- ④ The value of  $R_{\theta JA}$  is measured with the device mounted on 1 in 2 FR-4 board with 2oz. Copper, in a still air environment with  $T_A = 25^\circ\text{C}$
- ⑤ These curves are based on the junction-to-case thermal impedance which is measured with the device mounted to a large heatsink, assuming a maximum junction temperature of  $T_{J(\text{MAX})} = 175^\circ\text{C}$ .

**Typical electrical and thermal characteristics**

**Figure 1: Typical Output Characteristics**

**Figure 2. Gate to source cut-off voltage**

**Figure 3. Drain-to-Source Breakdown Voltage vs. Temperature**

**Figure 4: Normalized On-Resistance Vs. Case Temperature**

Typical electrical and thermal characteristics

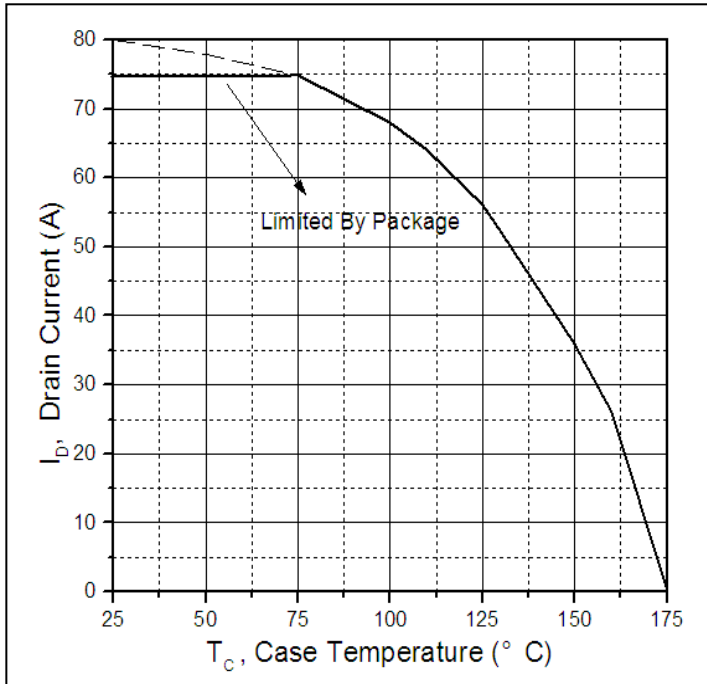


Figure 5. Maximum Drain Current Vs. Case Temperature

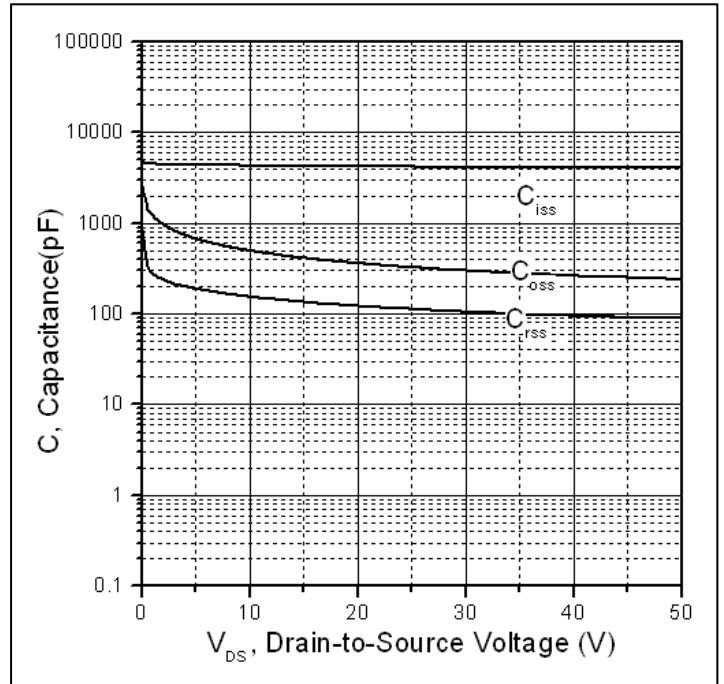


Figure 6. Typical Capacitance Vs. Drain-to-Source Voltage

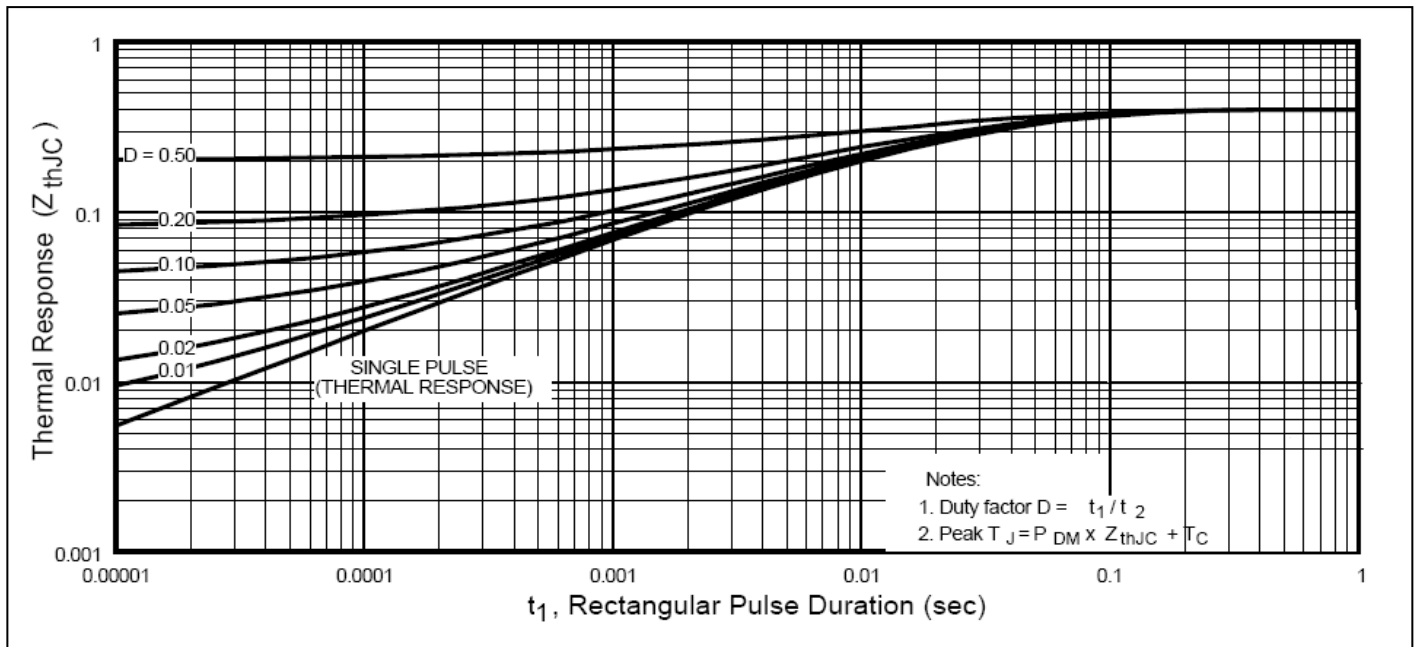
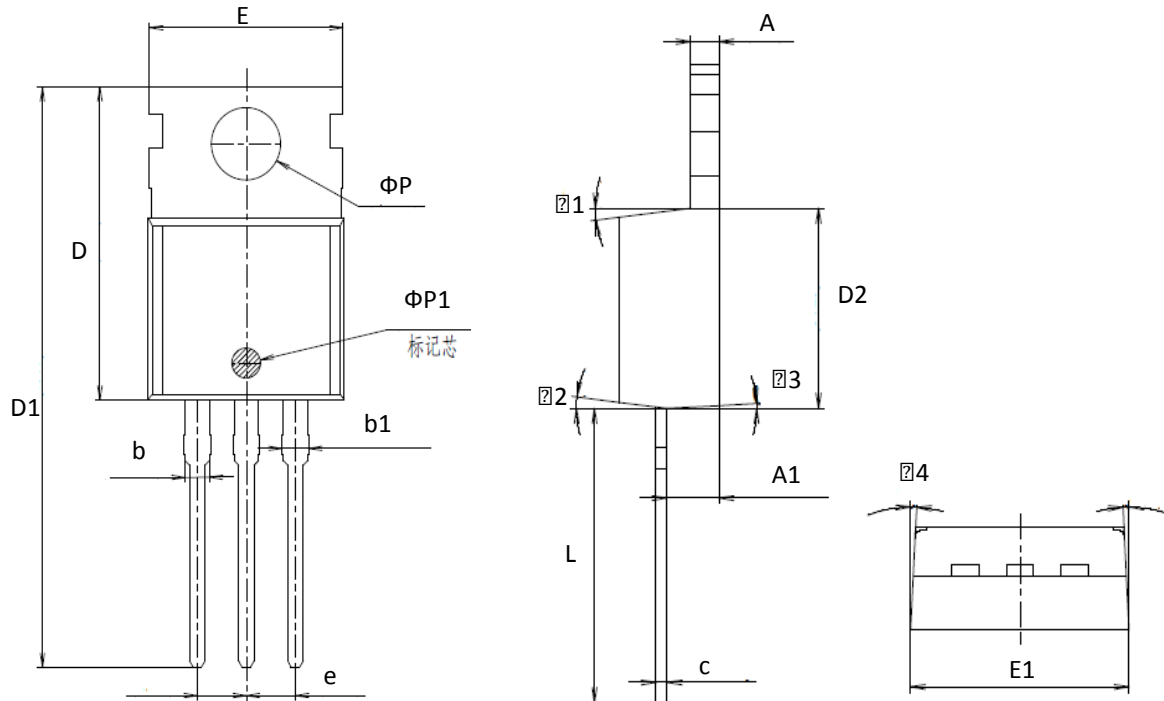


Figure 7. Maximum Effective Transient Thermal Impedance, Junction-to-Case

**Mechanical Data:**
**TO220 PACKAGE OUTLINE DIMENSION\_GN**


Symbol	Dimension In Millimeters			Dimension In Inches		
	Min	Nom	Max	Min	Nom	Max
A	-	1.300	-	-	0.051	-
A1	2.200	2.400	2.600	0.087	0.094	0.102
b	-	1.270	-	-	0.050	-
b1	1.270	1.370	1.470	0.050	0.054	0.058
c	-	0.500	-	-	0.020	-
D	-	15.600	-	-	0.614	-
D1	-	28.700	-	-	1.130	-
D2	-	9.150	-	-	0.360	-
E	9.900	10.000	10.100	0.390	0.394	0.398
E1	-	10.160	-	-	0.400	-
ΦP	-	3.600	-	-	0.142	-
ΦP1		1.500			0.059	
e	2.54BSC			0.1BSC		
L	12.900	13.100	13.300	0.508	0.516	0.524
Θ1	-	7°	-	-	7°	-
Θ2	-	7°	-	-	7°	-
Θ3	-	3°	-	5°	7°	9°
Θ4	-	3°	-	1°	3°	5°

**Ordering and Marking Information**
**Device Marking: SSF80100**

**Package (Available)**  
**TO220**  
**Operating Temperature Range**  
**C : -55 to 175 °C**

**Devices per Unit**

Package Type	Units/Tube	Tubes/Inner Box	Units/Inner Box	Inner Boxes/Carton Box	Units/Carton Box
TO220	50	20	1000	6	6000

**Reliability Test Program**

Test Item	Conditions	Duration	Sample Size
High Temperature Reverse Bias(HTRB)	$T_j=125^{\circ}\text{C}$ to $175^{\circ}\text{C}$ @ 80% of Max $V_{DSS}/V_{CES}/V_R$	168 hours 500 hours 1000 hours	3 lots x 77 devices
High Temperature Gate Bias(HTGB)	$T_j=150^{\circ}\text{C}$ or $175^{\circ}\text{C}$ @ 100% of Max $V_{GSS}$	168 hours 500 hours 1000 hours	3 lots x 77 devices

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Sales@silikron.com

**Technical Support:**

Technical@silikron.com

**Suzhou Silikron Semiconductor Corp.**

11A, 428 Xinglong Street, Suzhou Industrial Park, P.R.China

**TEL:** (86-512) 62560688

**FAX:** (86-512) 65160705

**E-mail:** Sales@silikron.com