SIMTEK

STK28C256

CMOS/SNOS EEPROM
High Performance
32K x 8 Electrically Erasable PROM

FEATURES

- **70, 90, 120 and 150ns Access Times**
- **Self-Timed Page Write**
- **Single 5V ±10% Supply**
- **Commercial and Military Temperature Ranges**
- **70, 90, 120 and 150ns Byte Load Times**
- **160µs/byte Effective Write Time**
- **80mA Active Current**
- **200µA Standby Current**
- **Hardware and Software Data Protection**
- **$\overline{\text{DATA}}$ Polling**
- **Toggle Bit**
- **10 Year Retention at 10^5 Write Cycles**
- **10ms Chip Erase and Chip Program**
- **Margin Mode**
- **Industry Standard Pinout and Operation**

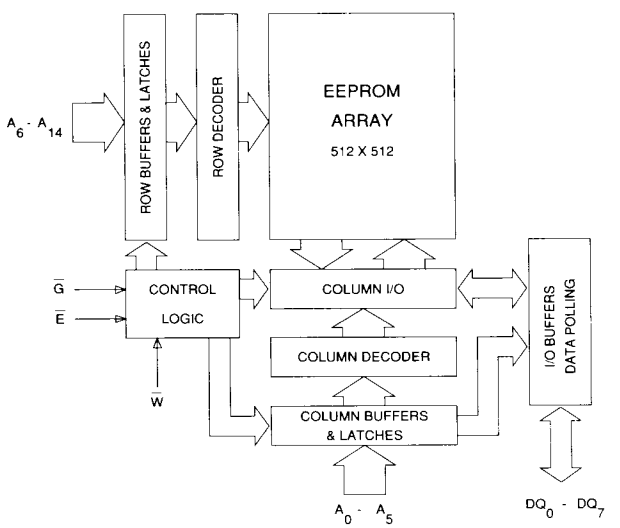
DESCRIPTION

The STK28C256 is a high performance EEPROM fabricated with Simtek's proprietary CMOS/SNOS technology. This full-featured device follows the JEDEC-approved pinout and 5V-only operation standard for 32K x 8 EEPROMs. Simtek is currently establishing a MIL-STD-883 compliant program.

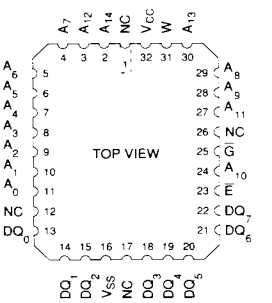
The STK28C256 features single and multi-byte page write cycles. Internal latches allow a byte load cycle time as fast as the read cycle time. Writing of latched data into the non-volatile cells is self-timed, resulting in an effective write time of 160µs/byte. Other features include software data protection, $\overline{\text{DATA}}$ polling and toggle bit early end-of-write detection, as well as software chip erase/program and hardware chip erase modes.

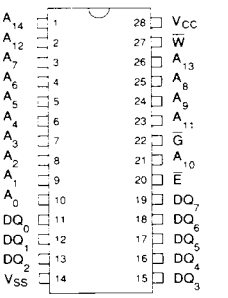
All devices are margin mode tested to a standard of 10 years data retention after 10^5 write cycles. Margin mode testing may be performed by the user at any time.

LOGIC BLOCK DIAGRAM



PIN CONFIGURATIONS





PIN NAMES

$A_0 - A_{14}$	Address Inputs
$DQ_0 - DQ_7$	Data In/Out
$\overline{E}$	Chip Enable
$\overline{G}$	Output Enable
$\overline{W}$	Write Enable
V_{CC}	Power (+5V)
V_{SS}	Ground

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ABSOLUTE MAXIMUM RATINGS[a]

Voltage on typical input relative to V_{SS} ..... –0.6V to 7.0V
Voltage on DQ_{0-7} and $\overline{W}$ ..... –0.5V to (V_{CC}+0.5V)
Voltage on $\overline{G}$ ..... –0.5V to 14.0V
Temperature under bias ..... –55°C to 125°C
Storage temperature ..... –65°C to 150°C
Power dissipation 1W
DC output current 15mA
(One output at a time, one second duration)

Note a: Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

DC CHARACTERISTICS

(V_{CC} = 5.0V ±10%)

SYMBOL	PARAMETER	COMMERCIAL		MILITARY		UNITS	NOTES	
		MIN	MAX	MIN	MAX			
T_C	Case Operating Temperature	0	70	–55	125	°C		
I_{CC}	Average V_{CC} Current (Active, Cycling TTL Inputs)		80			mA	t_{AVAV} = 70ns	$\overline{E}$ = $\overline{G}$ = V_{IL}
			70		80	mA	t_{AVAV} = 90ns	W = V_{IH}
			60		70	mA	t_{AVAV} = 120ns	DQ_{0-7} open
					60	mA	t_{AVAV} = 150ns	
I_{SB_1}	Average V_{CC} Current (Standby, Stable TTL Inputs)		1.5		1.5	mA	$\overline{E}$ = V_{IH}	
I_{SB_2}	Average V_{CC} Current (Standby, Stable CMOS Inputs)		200		200	µA	$\overline{E} \geq (V_{CC}-0.2V)$ $V_{IN} \leq 0.2V$ or $V_{IN} \geq (V_{CC}-0.2V)$	
I_{ILK}	Input Leakage Current		±5		±5	µA	V_{IN} = 0V to V_{CC}	
I_{OLK}	Output Leakage Current		±10		±10	µA	$\overline{E}$ = V_{IH} V_{IN} = 0V to V_{CC}	
V_{IH}	Input Logic "1" Voltage	2.0	V_{CC}+0.5	2.0	V_{CC}+0.5	V	All Inputs	
V_{IL}	Input Logic "0" Voltage	–0.5	0.8	–0.5	0.8	V	All Inputs	
V_{OH}	Output Logic "1" Voltage	2.4		2.4		V	I_{OH} = –4mA	
V_{OL}	Output Logic "0" Voltage		0.45		0.45	V	I_{OL} = 6mA	
V_{WI}	Write Inhibit Supply Voltage	3.2	3.8	3.2	3.8	V	See Note e.	
V_H	Supervoltage	11.5	13	11.5	13	V	See Note e.	

MODE SELECTION[b,c]

Mode	$\overline{E}$	$\overline{G}$	$\overline{W}$	DQ_{0-7}	I_{CC}
Standby	H	X	X	High Z	Standby
Read	L	L	H	D_{OUT}	Active
Byte or Page Write	L	H	L	D_{IN}	Active
Write Inhibit	X	X	H	-	-
Write Inhibit	X	L	X	-	-
Chip Erase	L	V_H	L	High Z	Active

Note b: H: high TTL level; L: low TTL level; X: H or L.
Note c: For information on Margin Mode, contact Simtek.

TYPICAL POWER-UP TIMING[d,e]

SYMBOL	PARAMETER	TYP	UNITS
t_{PUR}	Power-up to Read Operation	100	µs
t_{PUW}	Power-up to Write Operation	5	ms

Note d: T_A = 25°C and V_{CC} = 5.0V.
Note e: These parameters are guaranteed but not 100% tested.

CAPACITANCE[e] (T_A=25°C, f=1.0MHz)

SYMBOL	PARAMETER	MAX	UNITS	CONDITIONS
C_{IN}	Input Capacitance	6	pF	ΔV=0 to 3V
C_{OUT}	Output Capacitance	10	pF	ΔV=0 to 3V

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AC TEST CONDITIONS

Input Pulse Levels	0V to 3V
Input Rise and Fall Times	≤ 5ns
Input and Output Timing Reference Levels	1.5V
Output Load	See Figure 1

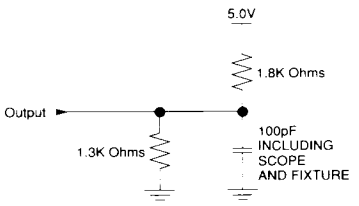


Figure 1 - AC Output Loading

AC CHARACTERISTICS

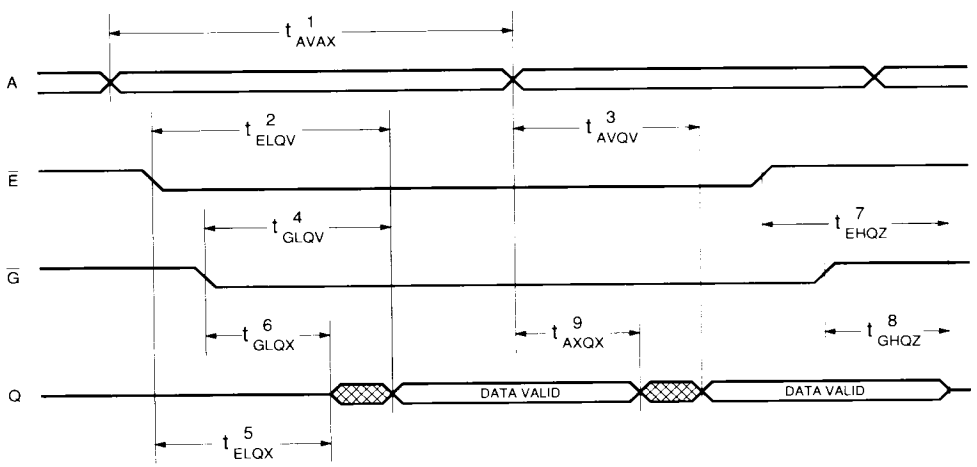
READ CYCLE [q]

(V_{CC} = 5.0V ±10%)

NO.	SYMBOL		PARAMETER	STK28C256-70		STK28C256-90		STK28C256-12		STK28C256-15		UNITS	NOTES
	Standard	Alternate		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX		
1	t_{AVAX}	t_{RC}	Read Cycle Time	70		90		120		150		ns	
2	t_{ELQV}	t_{CE}	Chip Enable Access Time		70		90		120		150	ns	
3	t_{AVQV}	t_{AA}	Address Access Time		70		90		120		150	ns	
4	t_{GLQV}	t_{OE}	Output Enable Access Time		35		40		50		60	ns	
5	t_{ELQX}	t_{LZ}	$\overline{E}$ Low to Active Output	10		10		10		10		ns	e,m
6	t_{GLQX}	t_{OLZ}	$\overline{G}$ Low to Active Output	10		10		10		10		ns	e
7	t_{EHQZ}	t_{HZ}	$\overline{E}$ High to High-Z Output		35		40		50		60	ns	e,n
8	t_{GHQZ}	t_{OHZ}	$\overline{G}$ High to High-Z Output		35		40		50		60	ns	e,n
9	t_{AXQX}	t_{OH}	Address Invalid to Data Out Invalid	0		0		0		0		ns	
10	t_{WHQVC}		$\overline{DATA}$ Polling Access Time		70		90		120		150	ns	e,p

Note e: These parameters are guaranteed but not 100% tested.
Note m: $\overline{G}$ is low before E goes low.
Note n: Measured ±200mV from steady state output voltage. Load capacitance is 5pF.
Note p: Refer to $\overline{DATA}$ Polling Cycle timing diagram.
Note q: $\overline{E}$ and $\overline{G}$ must make the transition between V_{IH} (min) to V_{IL} (max), or V_{IL} (max) to V_{IH} (min) in a monotonic fashion. $\overline{W}$ must remain high throughout the cycle.

READ CYCLE [q]



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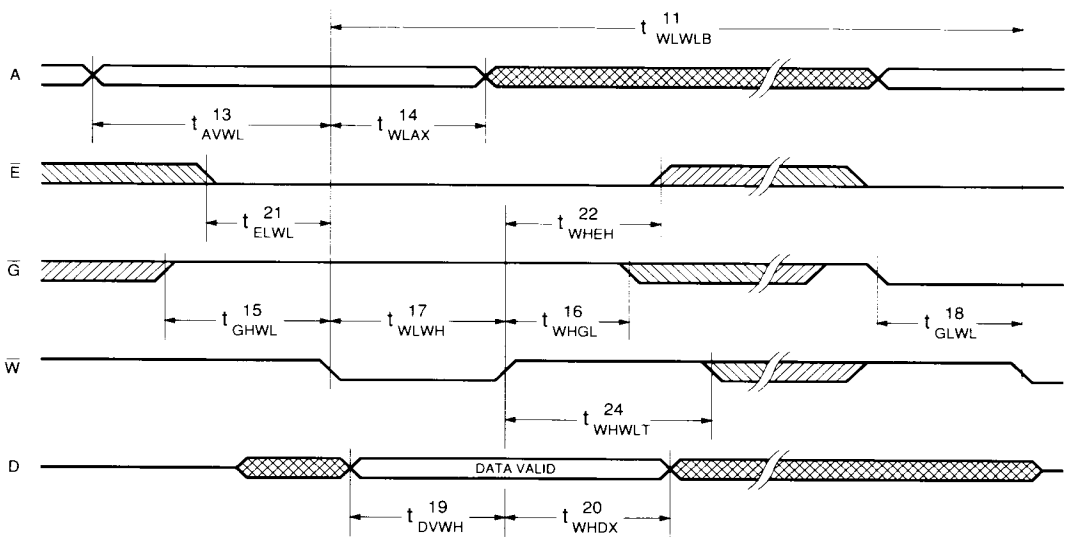
BYTE/PAGE WRITE CYCLE 1: $\overline{W}$ CONTROLLED[r,s]

(V_{CC} = 5.0V ±10%)

NO.	SYMBOL		PARAMETER	STK28C256-70		STK28C256-90		STK28C256-12		STK28C256-15		UNITS	NOTES
	Standard	Alternate		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX		
11	t_{WLWLB}	t_{WC}	Write Cycle Time		10		10		10		10	ms	
12	t_{WLWLP}	t_{BLC}	Byte Load Cycle Time	70		90		120		150		ns	t
13	t_{AVWL}	t_{AS}	Address Set-Up Time	0		0		0		0		ns	
14	t_{WLAX}	t_{AH}	Address Hold Time	35		45		50		75		ns	
15	t_{GHWL}	t_{OES}	$\overline{G}$ High to $\overline{W}$ Low Time	0		0		0		0		ns	
16	t_{WHGL}	t_{OEH}	$\overline{G}$ High Hold Time from $\overline{W}$ High	0		0		0		0		ns	
17	t_{WLWH}	t_{WP}	Write Pulse Duration	45		60		80		100		ns	r,x
18	t_{GLWL}		$\overline{G}$ Low Write Inhibit Setup Time	0		0		0		0		ns	
19	t_{DVWH}	t_{DS}	Data Set-Up Time	45		45		45		45		ns	
20	t_{WHDX}	t_{DH}	Data Hold Time	0		0		0		0		ns	
21	t_{ELWL}	t_{CS}	$\overline{E}$ Set-Up Time to W Low	0		0		0		0		ns	
22	t_{WHEH}	t_{CH}	$\overline{E}$ Hold Time from $\overline{W}$ High	0		0		0		0		ns	
23	t_{WHWLP}	t_{WPH}	$\overline{W}$ High to $\overline{W}$ Low Time	15		20		35		45		ns	t,x
24	t_{WHWLT}		$\overline{W}$ Timeout	100		100		100		100		µs	u

Note r: $\overline{W}$ and $\overline{E}$ are noise protected. A write pulse of less than 7ns (typical) will not activate a write cycle.
Note s: E, G and $\overline{W}$ must make the transition between V_{IH} (min) to V_{IL} (max), or V_{IL} (max) to V_{IH} (min) in a monotonic fashion.
Note t: Refer to Page Write Cycle 1 timing diagram.
Note u: This is the minimum time the internal timer waits before initiating the erase/program portion of the write cycle.
Note x: During a Page Write Cycle, the maximum pulse duration allowed is 100µs.

BYTE WRITE CYCLE 1: $\overline{W}$ CONTROLLED[r,s]



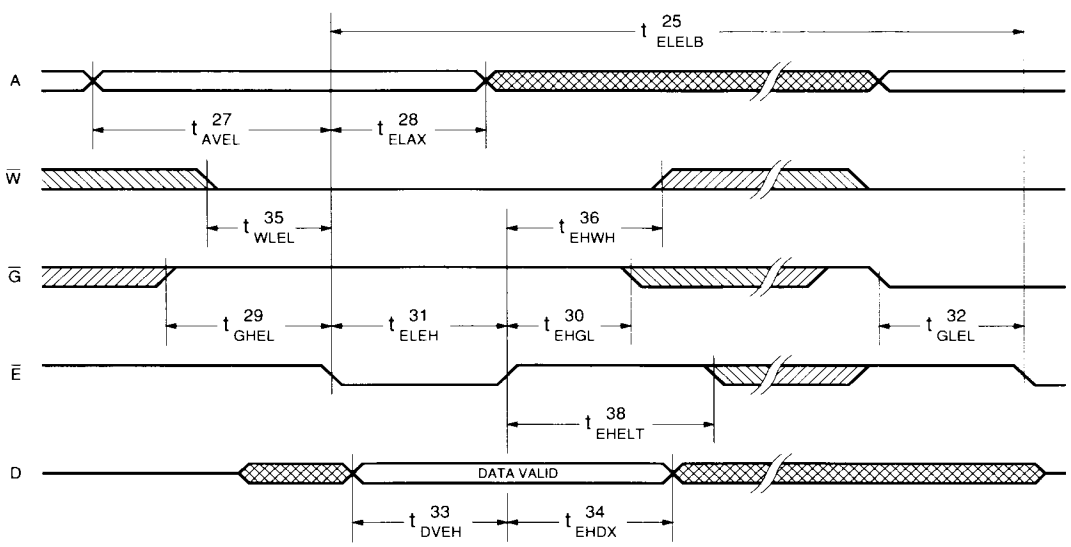
BYTE/PAGE WRITE CYCLE 2: $\overline{E}$ CONTROLLED[r,s]

(V_{CC} = 5.0V ±10%)

NO.	SYMBOL		PARAMETER	STK28C256-70		STK28C256-90		STK28C256-12		STK28C256-15		UNITS	NOTES
	Standard	Alternate		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX		
25	t_{ELELB}	t_{WC}	Write Cycle Time		10		10		10		10	ms	
26	t_{ELELP}	t_{BLC}	Byte Load Cycle Time	70		90		120		150		ns	v
27	t_{AVEL}	t_{AS}	Address Set-Up Time	0		0		0		0		ns	
28	t_{ELAX}	t_{AH}	Address Hold Time	35		45		50		75		ns	
29	t_{GHEL}	t_{OES}	$\overline{G}$ High to $\overline{E}$ Low Time	0		0		0		0		ns	
30	t_{EHGL}	t_{OEH}	$\overline{G}$ High Hold Time from $\overline{E}$ High	0		0		0		0		ns	
31	t_{ELEH}	t_{WP}	Write Pulse Duration	45		60		80		100		ns	r,x
32	t_{GLEL}		$\overline{G}$ Low Write Inhibit Setup Time	0		0		0		0		ns	
33	t_{DVEH}	t_{DS}	Data Set-Up Time	45		45		45		45		ns	
34	t_{EHDX}	t_{DH}	Data Hold Time	0		0		0		0		ns	
35	t_{WLEL}	t_{CS}	$\overline{W}$ Set-Up Time to $\overline{E}$ Low	0		0		0		0		ns	
36	t_{EHWH}	t_{CH}	$\overline{W}$ Hold Time from $\overline{E}$ High	0		0		0		0		ns	
37	t_{EHELP}	t_{WPH}	$\overline{E}$ High to $\overline{E}$ Low Time	15		20		35		45		ns	v,x
38	t_{EHELT}	t_{WPH}	$\overline{E}$ Timeout	100		100		100		100		µs	u

Note r: $\overline{W}$ and $\overline{E}$ are noise protected. A write pulse of less than 7ns (typical) will not activate a write cycle.
Note s: $\overline{E}$, $\overline{G}$ and $\overline{W}$ must make the transition between V_{IH} (min) to V_{IL} (max), or V_{IL} (max) to V_{IH} (min) in a monotonic fashion.
Note v: Refer to Page Write Cycle 2 timing diagram.
Note u: This is the minimum time the internal timer waits before initiating the erase/program portion of the write cycle.
Note x: During a Page Write Cycle, the maximum pulse duration allowed is 100µs.

BYTE WRITE CYCLE 2: $\overline{E}$ CONTROLLED[r,s]



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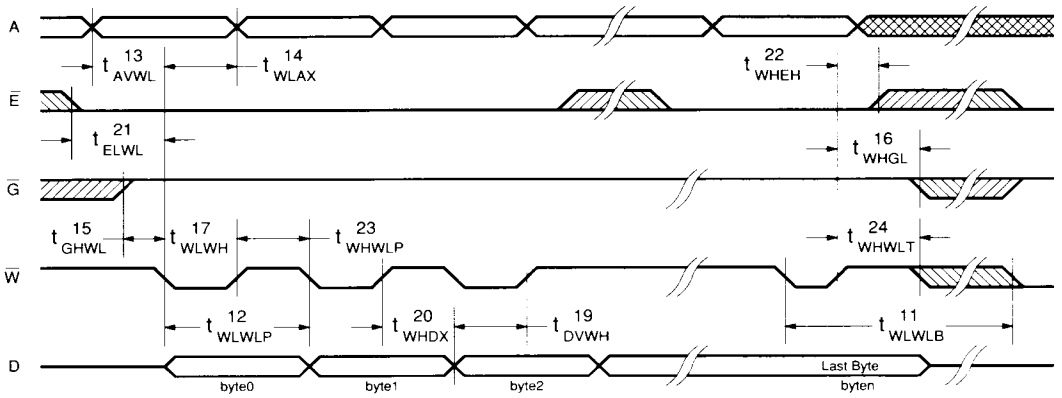
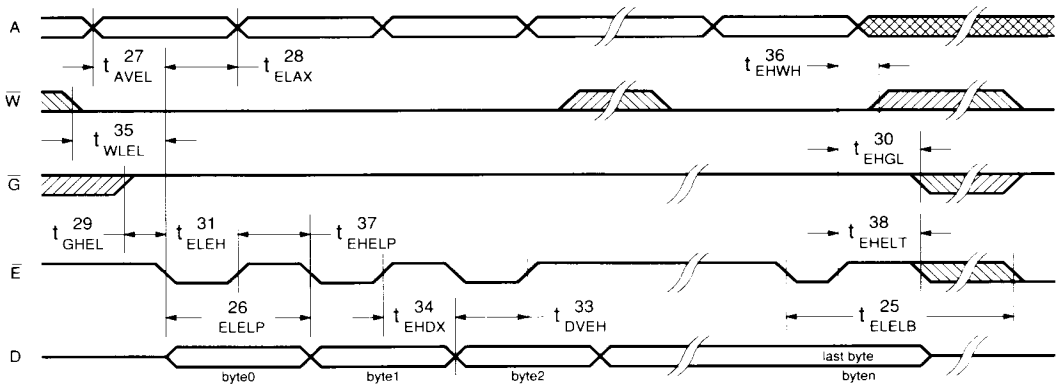
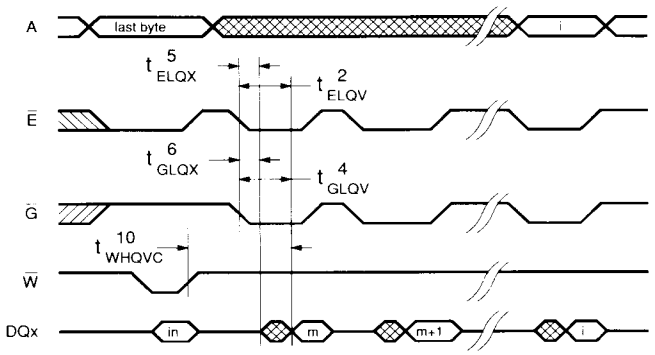
PAGE WRITE CYCLE 1: $\overline{W}$ CONTROLLED[r,s]



PAGE WRITE CYCLE 2: $\overline{E}$ CONTROLLED[r,s]



$\overline{DATA}$ & TOGGLE BIT POLLING CYCLES[s,t]



$\overline{DATA}$ POLLING

- DQx is data bit 7.
- $D_m = D_{m+1}$ = complement of input data until erase/program portion of the write cycle is complete.
- $D_i = Data_{IN}$ if $A_i = A_{last\ byte}$

TOGGLE BIT POLLING

- DQx is data bit 6.
- $D_m = 0$ and $D_{m+1} = 1$. Subsequent reads continue to toggle DQ_6 until the erase/program portion of the write cycle is complete.
- D_i = data at A_i

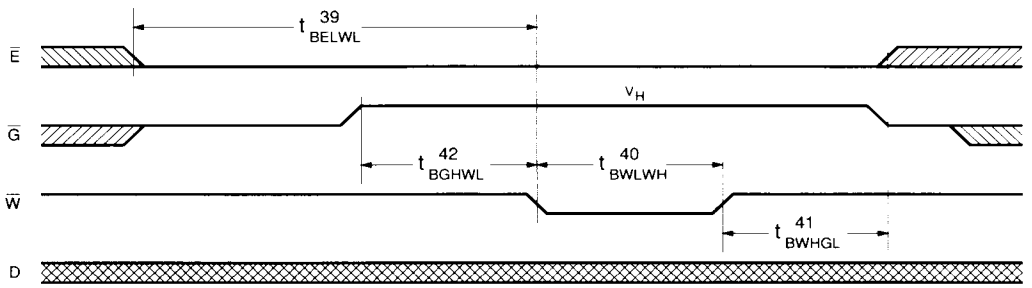
Note r: $\overline{W}$ and $\overline{E}$ are noise protected. A write pulse of less than 7ns (typical) will not activate a write cycle.
Note s: $\overline{E}$, $\overline{G}$ and $\overline{W}$ must make the transition between V_{IH} (min) to V_{IL} (max), or V_{IL} (max) to V_{IH} (min) in a monotonic fashion.
Note t: Either $\overline{E}$ or $\overline{W}$ controlled write cycles may be used prior to either of the polling cycles. During the polling operation, either $\overline{E}$ and $\overline{G}$ may toggle together, or each may toggle alone if the other is held low. Polling cycle access times are characterized but not tested.

CHIP ERASE CYCLE

(V_{CC} = 5.0V ±10%)

NO.	SYMBOL		PARAMETER	STK28C256-70		STK28C256-90		STK28C256-12		STK28C256-15		UNITS	NOTES
	Standard	Alternate		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX		
39	t_{BELWL}		Chip Enable Set-Up to $\overline{W}$	5		5		5		5		µs	
40	t_{BWLWH}	t_W	$\overline{W}$ Pulse Duration	10		10		10		10		ms	
41	t_{BWHGL}	t_H	$\overline{W}$ Recovery	5		5		5		5		µs	
42	t_{BGHWL}	t_S	$\overline{G}$ at V_H to $\overline{W}$ low	5		5		5		5		µs	

CHIP ERASE CYCLE



DEVICE OPERATION

READ

The read operation is identical to that of a static RAM. When $\overline{E}$ and $\overline{G}$ are LOW and $\overline{W}$ is HIGH, the data stored at the memory location determined by the address pins is asserted on the outputs. The outputs are in a high impedance state whenever $\overline{E}$ or $\overline{G}$ is HIGH.

BYTE and PAGE WRITE

A low pulse on $\overline{W}$ (with $\overline{E}$ low) or $\overline{E}$ (with $\overline{W}$ low), while $\overline{G}$ is HIGH, initiates a write cycle. The address is latched on the falling edge of $\overline{W}$ or $\overline{E}$, whichever occurs last. The data is latched on the rising edge of $\overline{W}$ or $\overline{E}$, whichever occurs first. The internal timer restarts when any $\overline{W}$ or $\overline{E}$ transition occurs. Once a write cycle is underway, if no $\overline{W}$ or $\overline{E}$ transitions are detected within the timeout period, the erase/program portion of the write begins, after which further write attempts are ignored.

The page write cycle allows 2 to 64 bytes to be loaded and then simultaneously written during the erase/program portion of the write cycle. The address of the page used for a page write operation is specified with A_{6-14}, which must be held constant throughout a given page write. The remaining addresses (A_{0-5}) specify bytes within each page.

HARDWARE PROTECTION

The STK28C256 offers three hardware protection features: **(1) V_{CC} Sense** - Writing is inhibited below a specified V_{CC} power supply level V_{WI}; **(2) Noise Filter** - When the $\overline{W}$ or $\overline{E}$ pulse is shorter than 7ns (typical), no write cycle occurs; and **(3) Write Inhibit** - Holding $\overline{G}$ low, $\overline{E}$ high, or $\overline{W}$ high inhibits writing.

SOFTWARE PROTECTION

Software protection is enabled by performing a 3-byte page write operation to specific addresses with specific data. Once enabled, the software protection feature may be overridden by preceding a page write operation with the same three addresses. The software protection circuitry is immune to power disruptions. To enable software protection, the following page write sequence must be executed (data format DQ_{7-0}; address format A_{14-0}):

1.	Load data	AAH	to address	5555H
2.	Load data	55H	to address	2AAAH
3.	Load data	A0H	to address	5555H
4.	Load data	XXH	to any address	(optional).

The part enters the software data protection mode at the end of the write period.

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To disable software protection mode, execute the following page write sequence:

1.	Load data	AAH	to address	5555H
2.	Load data	55H	to address	2AAAH
3.	Load data	80H	to address	5555H
4.	Load data	AAH	to address	5555H
5.	Load data	55H	to address	2AAAH
6.	Load data	20H	to address	5555H
7.	Load data	XXH	to any address	(optional).

The part exits the software data protection mode at the end of the write period. When the STK28C256 detects one of these sequences, all load commands that are part of the code information will be ignored. A valid page cycle could begin at this point. Note that the software protection enable and disable sequences constitute an illegal page write in that the page address is changed within a page write operation.

$\overline{\text{DATA}}$ POLLING

$\overline{\text{DATA}}$ polling may be used to detect an early end of the write cycle, minimizing waiting time. At any time during any write cycle, attempting a read from the last address written will result in the complement of the written data on DQ_7. Once the write cycle has been completed, true data will appear on DQ_{0-7} and the next cycle can begin.

TOGGLE BIT (DQ_6)

As an additional method for detecting an early end of the write cycle, DQ_6 will toggle between a logic one and a logic zero on consecutive attempts to read any address during the erase/program part of the cycle. When the write cycle is complete, DQ_6 will no longer toggle and will reflect the memory contents.

CHIP ERASE and CHIP PROGRAM

The following page write sequence will set all bits in the memory to a logic HIGH. The operation will take t_{WC} (max) time to complete, and the Toggle Bit will indicate early completion.

1.	Load data	AAH	to address	5555H
2.	Load data	55H	to address	2AAAH
3.	Load data	80H	to address	5555H
4.	Load data	AAH	to address	5555H
5.	Load data	55H	to address	2AAAH
6.	Load data	10H	to address	5555H

To set all the bits to a logic LOW, the data value in byte #6 should be changed from 10 (hex) to 40 (hex).

The entire memory may be set to a HIGH state through the hardware chip erase operation. By setting $\overline{E}$ LOW and $\overline{G}$ to the supervoltage V_H, the chip is erased when a 10ms pulse is applied to $\overline{W}$. If the chip is in software protection mode, neither software nor hardware chip erase/program operations will take place.

ORDERING INFORMATION

t_{ELQV}	Ordering Code	Package	Temp. Range
70	STK28C256C70	Ceramic 28-Pin DIP	Commercial 0° to 70° C
	STK28C256L70	Ceramic 28-Pin LCC	
	STK28C256P70	Plastic 28-Pin DIP	
	STK28C256J70	Plastic 28-Pin SOJ	
90	STK28C256C90	Ceramic 28-Pin DIP	Commercial 0° to 70° C
	STK28C256L90	Ceramic 28-Pin LCC	
	STK28C256P90	Plastic 28-Pin DIP	
	STK28C256J90	Plastic 28-Pin SOJ	
	STK28C256C90M	Ceramic 28-Pin DIP	Military -55° to 125° C
	STK28C256L90M	Ceramic 28-Pin LCC	
120	STK28C256C12	Ceramic 28-Pin DIP	Commercial 0° to 70° C
	STK28C256L12	Ceramic 28-Pin LCC	
	STK28C256P12	Plastic 28-Pin DIP	
	STK28C256J12	Plastic 28-Pin SOJ	
	STK28C256C12M	Ceramic 28-Pin DIP	Military -55° to 125° C
	STK28C256L12M	Ceramic 28-Pin LCC	
150	STK28C256C15M	Ceramic 28-Pin DIP	Military -55° to 125° C
	STK28C256L15M	Ceramic 28-Pin LCC	

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