ADVANCED INFORMATION

CMOS LDO REGULATOR WITH INPUT AND OUTPUT VOLTAGE DETECTORS

FEATURES

- **Low Dropout Voltage**
- **Very Low Quiescent Current (50 µA maximum)**
- **Internal Bandgap Reference**
- **Regulates down to 1.8 V**
- **Short Circuit Protection**
- **Very Low Standby Current**
- **Active High On/Off Control**
- **Low Input Voltage Detection**
- **Low Output Voltage Detection**
- **Small SOT23L-6 Package**

APPLICATIONS

- **Battery Powered Systems**
- **Cellular Telephones**
- **Pagers**
- **Toys**
- **Radio Control Systems**
- **Low Voltage Systems**
- **Personal Communications Systems**
- **Portable Instrumentation**
- **Portable Consumer Equipment**

DESCRIPTION

The TK655xx is a low dropout linear regulator housed in a small SOT23L-6 package, rated at 400 mW.

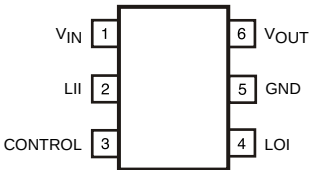
An internal P Channel pass element is used in order to achieve low dropout voltage. The device has extremely low quiescent current (max 50 µA). The device offers high precision output voltage of 2.5% over the full temperature range. The low quiescent current and dropout voltage make this part ideal for battery powered applications. In the standby mode when the output is disabled, the linear regulator only draws 6 µA typically.

The TK655xx CMOS Linear Regulator also offers Low Input Indication (LII). This supply monitor trips typically at 1.1 times VOUT to indicate the user the supply is running low.

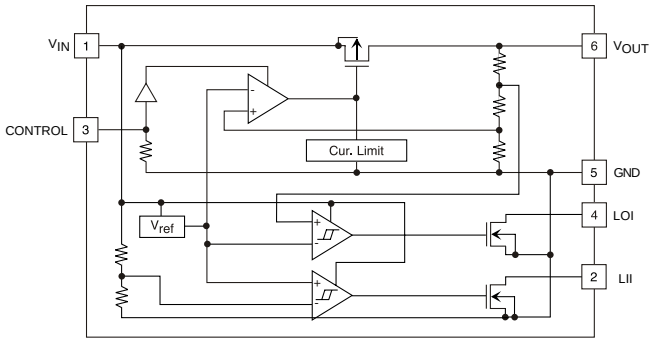
The device further offers a Low Output Indicator (LOI) which typically trips if the output drops to 93% of its regulation level.

With the integration of the voltage monitors for input and output voltages, the TK655xx CMOS Linear Regulator is a space and cost effective solution to a power management system designer.

TK655xxM



BLOCK DIAGRAM



ORDERING INFORMATION

TK655xxM □□

Tape/Reel Code
Package Code
Voltage Code

VOLTAGE CODE

18 = 1.8 V	33 = 3.3 V
20 = 2.0 V	35 = 3.5 V
25 = 2.5 V	40 = 4.0 V
28 = 2.8 V	45 = 4.5 V
30 = 3.0 V	50 = 5.0 V

TAPE/REEL CODE
TL: Tape Left

PACKAGE CODE
M: SOT-23L-6

ABSOLUTE MAXIMUM RATINGS

Supply Voltage ..... 6 V
Power Dissipation (Note 1) ..... 400 mW
Storage Temperature Range ..... -55 to +150 °C
Operating Temperature Range ..... -30 to +80 °C

ELECTRICAL CHARACTERISTICS

Test conditions: V_{DD} = 5 V, T_A = 25 °C, unless otherwise specified.

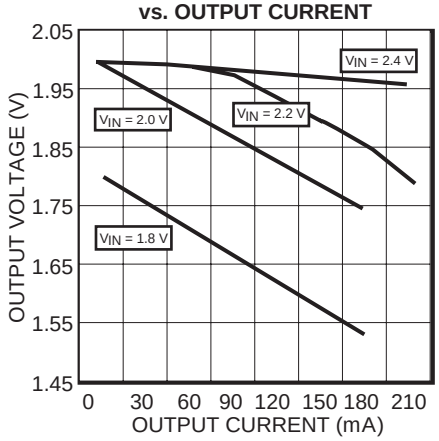
SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
V_{IN}	Supply Voltage Range		2		5.5	V
I_Q	Quiescent Current	I_{OUT} = 0 mA			50	µA
I_{STBY}	Standby Current	Output Off		6	20	µA
V_{OUT}	Output Voltage	I_{OUT} = 1 mA (Note 2)	-1.5%	V_{REG}	+1.5%	V
$V_{OUT(TEMP)}$	Output Voltage	I_{OUT} = 1 mA OVER OPERATING Temperature Range	-1%	V_{OUT}	+1%	V
V_{DROP}	Dropout Voltage	I_{OUT} = 100 mA		100	350	mV
I_{OUT}	Output Current		100		TBD	mA
Line Reg	Line Regulation	V_{IN} = V_{REG} + .5 V to 5.5 V @ 1 mA			50	mV
Load Reg	Load Regulation	I_{OUT} = 1 mA to 80 mA			100	mV
RR	Ripple Rejection	@ 30 mA		60		dB
CONTROL TERMINAL SPECIFICATIONS						
I_{CONT}	Control Terminal Current			1	10	µA
V_{CONT} (ON)	Control Voltage ON	Output ON	1.8		V_{IN} + 0.1	V
V_{CONT} (OFF)	Control Voltage OFF	Output OFF	0		0.6	V
Trans	Transient (OFF to ON)	I_{OUT} = 50 mA, CL = 0.1 µF		100		µS
LOW OUTPUT INDICATOR TERMINAL SPECIFICATION						
$V_{TH(LOI)}$	LOI Threshold		-1%	.93V_{OUT}	1%	V
$I_{S(LOI)}$	LOI Sink Current	LOI pin @ 0.5 V, V_{IN} = 3 V	1.5			mA
$\Delta V_{TH(LOI)}$	LOI Threshold Hysteresis			5		%
$T_{d(HL)}$	Delay (High to Low)				200	µS
$T_{d(LH)}$	Delay (Low to High)				100	µS
LOW INPUT INDICATOR TERMINAL SPECIFICATION						
$V_{TH(LII)}$	LII Threshold		-2.5%	1.1V_{OUT}	+2.5%	V
$I_{S(LII)}$	LII Sink Current	LII pin @ 0.5 V, V_{IN} = 3 V	1.5			mA
$\Delta V_{TH(LII)}$	LII Threshold Hysteresis		3	5	7	%
$T_{d(HL)}$	Delay (High to Low)				200	µS
$T_{d(LH)}$	Delay (Low to High)				100	µS

Note 1: Power dissapation is 400 mW when mounted as recommended. Derate at 3.2 mW/°C for operation above 25 °C.
Note 2: V_{REG} = 1.8 V to 5 V, 0.1 V step.

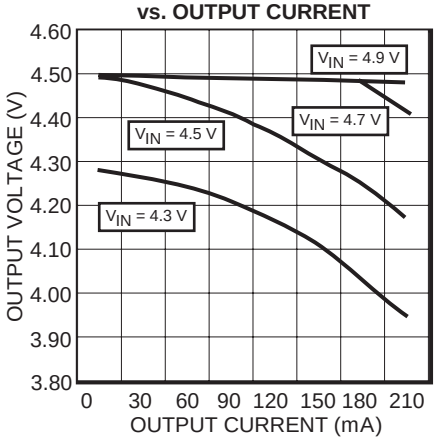
TYPICAL PERFORMANCE CHARACTERISTICS

T_A = 25 °C, unless otherwise specified.

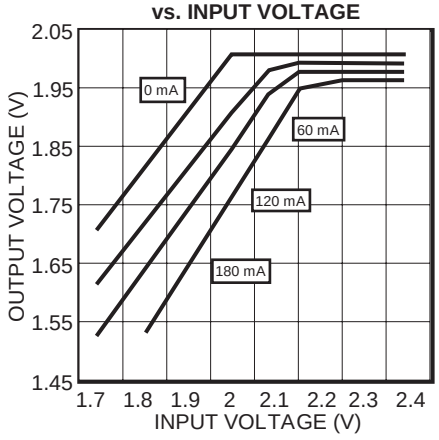
TK65520 OUTPUT VOLTAGE vs. OUTPUT CURRENT



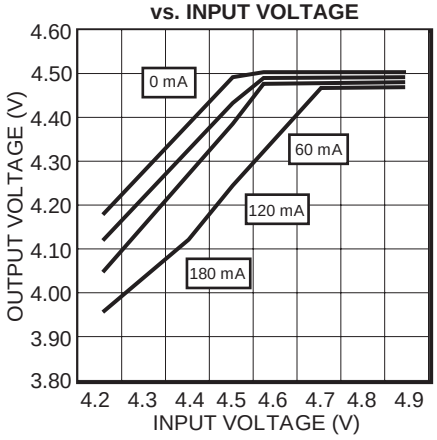
TK65545 OUTPUT VOLTAGE vs. OUTPUT CURRENT



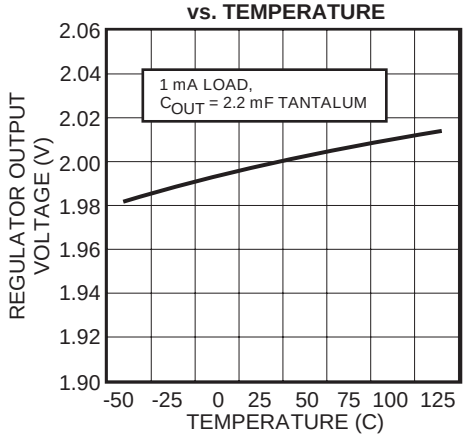
TK65520 OUTPUT VOLTAGE vs. INPUT VOLTAGE



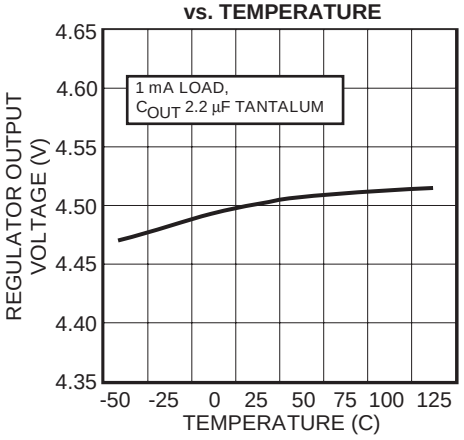
TK65545 OUTPUT VOLTAGE vs. INPUT VOLTAGE



TK65520 OUTPUT VOLTAGE vs. TEMPERATURE



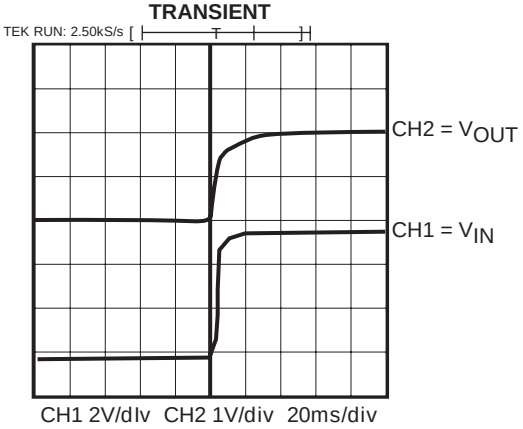
TK65545 OUTPUT VOLTAGE vs. TEMPERATURE



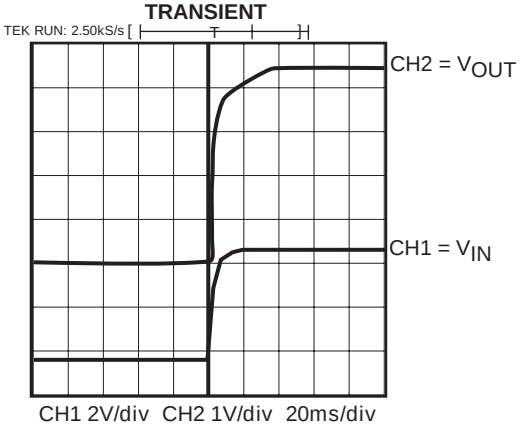
TYPICAL PERFORMANCE CHARACTERISTICS (CONT)

T_A = 25 °C, unless otherwise specified.

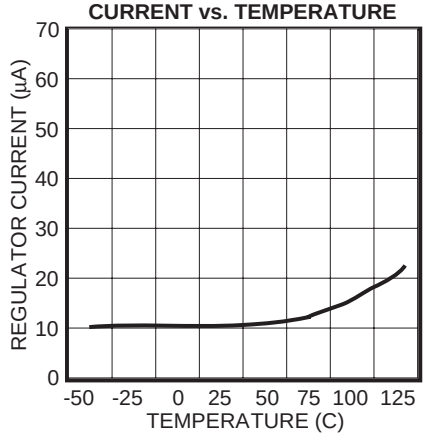
TK65520 POWER OFF to ON TRANSIENT



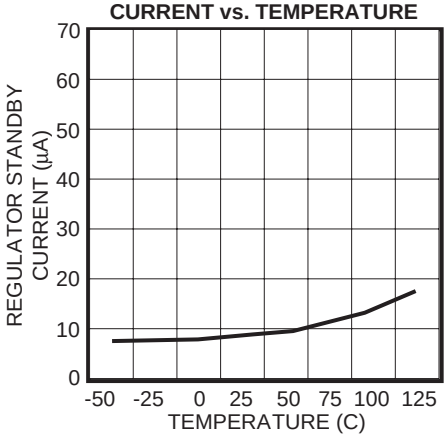
TK65545 POWER OFF to ON TRANSIENT



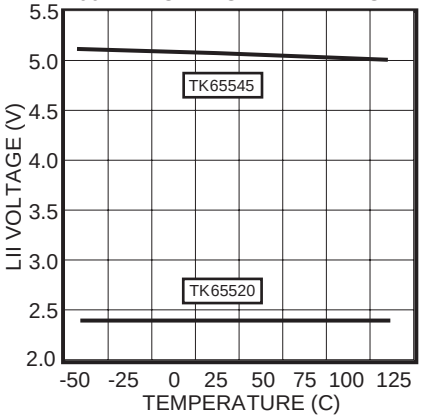
TK655xx REGULATOR CURRENT vs. TEMPERATURE



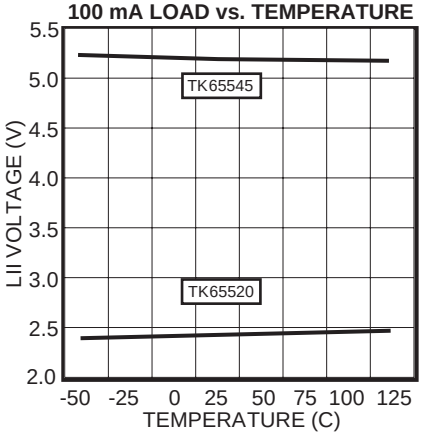
TK655xx STANDBY CURRENT vs. TEMPERATURE



TK655xx LII ASSERTED (ON) 100 mA LOAD vs. TEMPERATURE



TK655xx LII DE-ASSERTED (OFF) 100 mA LOAD vs. TEMPERATURE



PIN DESCRIPTION

Pin1 Input Voltage pin (V_{IN})

This pin is the positive input supply for the TK655xx CMOS Linear Regulator. Current flowing into this pin provides power to the IC and to the internal pass transistor. The voltage source driving this pin should have relatively low AC impedance. Good design practices dictate decoupling to the GND pin.

Pin 2 Low Input Indicator pin (LII)

This pin is an open drain where typically a high value resistor of the order of 300k ohms will be used to pull the LII pin to V_{OUT} or V_{IN} depending on the application. The supply voltage is internally monitored via a resistor divider network which compares against the bandgap reference. The trip point to indicate the supply is low is set to 1.1 V_{OUT}.

Pin 3 Control pin

The control pin acts as an enable pin to power up the device when the control pin is tied to a high potential (greater than 0.8 V). When the user requires to disable the part, the control pin must be brought below 0.6 V. while in the disable mode, the output voltage will droop to zero volts, the device will draw lower current (Standby current), yet the Low Input Indicator circuit is still awake monitoring the supply.

Pin 4 Low Output Indicator pin (LOI)

This pin is also an open drain where a large value resistor of the order of 300k ohms will pull the LOI pin to V_{IN} or V_{OUT} depending on the application. The purpose of this signal is to inform that the device is out of regulation. The device can go out of regulation when excessive loading is requested from the regulator. The device can also go out of regulation if the input supply is low and therefore the output must drop with the input.

Pin 5 Ground pin (GND)

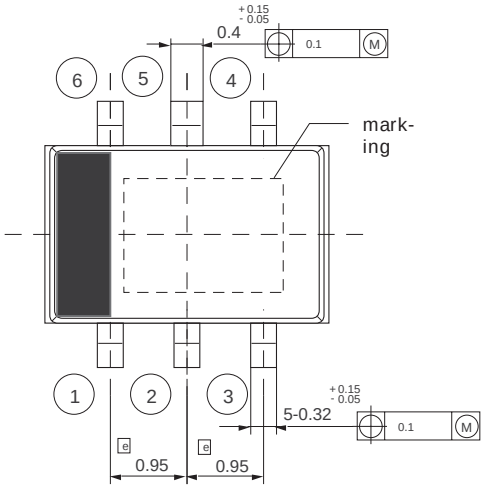
This pin provides the ground connection for the IC.

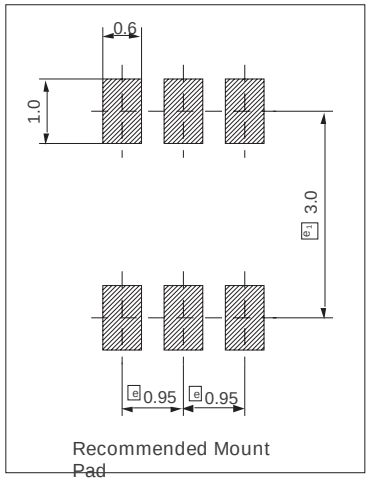
Pin 6 Output Voltage pin (V_{OUT})

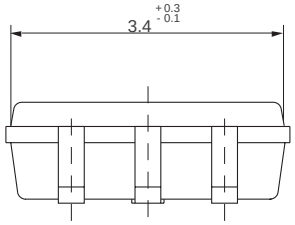
This pin senses the output voltage of the regulator. The output voltage is resistively divided in the IC and compared to the bandgap voltage. If the output voltage drops below regulation, the TK655xx pass transistor will be activated by the opamp regulation loop to maintain the output at the desired voltage.

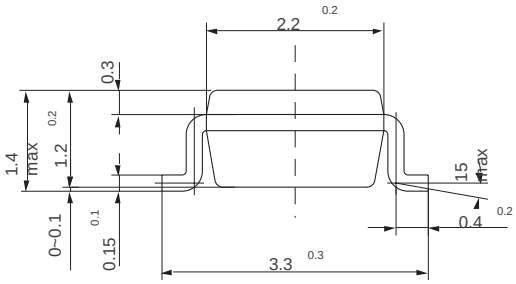
PACKAGE OUTLINE

SOT23L-6









Marking Information

Part Number	Marking

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