TOSHIBA MOS MEMORY PRODUCTS

TMM24256BP/BF-17, -20

DESCRIPTION

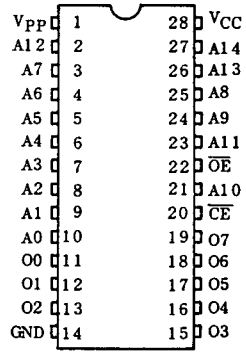
The TMM24256BP/BF is a 32,768 words × 8 bits one time programmable read only memory, and molded in a 28 pin plastic package.
The TMM24256BP/BF's access time is 170ns/200ns, and has low power standby mode which reduces the power dissipation without increasing access time.
The electrical characteristics and programming method are the same as U.V. EPROM TMM27256BD's.
Once progamed, the TMM24256BP/BF can not be erased because of using plastic DIP without transparent window.

FEATURES

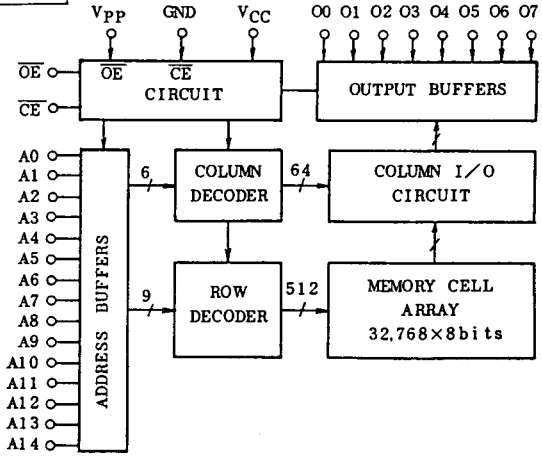
	-17	-20
V_{CC}	5V±5%	
t_{ACC}	170ns	200ns
I_{CC2}	100mA	
I_{CC1}	30mA	

- Full static operation
- High speed programming mode I, II
- Inputs and outputs TTL compatible
- Pin compatible with TMM27256D/AD/BD
- Standard 28 pin DIP plastic package: TMM24256BP
- Plastic Flat Package: TMM24256BF

PIN CONNECTION (TOP VIEW)



BLOCK DIAGRAM



PIN NAMES

A0 ∿ A14	Address Inputs
O0 ∿ O7	Outputs (Inputs)
$\overline{CE}$	Chip Enable Input
$\overline{OE}$	Output Enable Input
V_{PP}	Program Supply Voltage
V_{CC}	Power Supply Voltage (+5V)
GND	Ground

MODE SELECTION

MODE \ PIN	$\overline{CE}$ (20)	$\overline{OE}$ (22)	V_{PP} (1)	V_{CC} (28)	O0 ∿ O7 (11∿13,15∿19)	POWER
Read	L	L	5V	5V	Data Out	Active
Output Deselect	*	H			High Impedance	
Standby	H	*			High Impedance	Standby
Program	L	H	12.5V 1)	6V 1)	Data In	Active
Program Inhibit	H	H			High Impecance	
Program Verify	*	L	12.75V 2)	6.25V 2)	Data Out	

*: H or L

1): HIGH SPEED PROGRAMMING MODE I
2): HIGH SPEED PROGRAMMING MODE II

MAXIMUM RATINGS

SYMBOL	ITEM	RATING	UNIT
V_{CC}	V_{CC} Power Supply Voltage	-0.6 ∿ 7.0	V
V_{PP}	Program Supply Voltage	-0.6 ∿ 14.0	V
V_{IN}	Input Voltage	-0.6 ∿ 7.0	V
$V_{I/O}$	Input/Output Voltage	-0.6 ∿ 7.0	V
P_D	Power Dissipation	1.0/0.6*	W
T_{SOLDER}	Soldering Temperature · Time	260 · 10	°C · sec
T_{STG}	Storage Temperature	-55 ∿ 150	°C
T_{OPR}	Operating Temperature	0 ∿ 70	°C

*: Plastic Flat Package

READ OPERATION

D.C. RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{IH}	Input High Voltage	2.0	-	V_{CC}+1.0	V
V_{IL}	Input Low Voltage	-0.3	-	0.8	V
V_{CC}	V_{CC} Power Supply Voltage	4.75	5.00	5.25	V
V_{PP}	Vpp Power Supply Voltage	2.0	V_{CC}	V_{CC}+0.6	V

D.C. AND OPERATING CHARACTERISTICS (Ta=0 ∿ 70°C, V_{CC}=5V±5%)

SYMBOL	PARAMETER	CONDITION	MIN.	TYP.	MAX.	UNIT
I_{LI}	Input Current	V_{IN}=0 ∿ V_{CC}	-	-	±10	μA
I_{CC1}	Supply Current (Standby)	$\overline{CE}$=V_{IH}	-	-	30	mA
I_{CC2}	Supply Current (Active)	$\overline{CE}$=V_{IL}	-	-	100	mA
V_{OH}	Output High Voltage	I_{OH}=-400μA	2.4	-	-	V
V_{OL}	Output Low Voltage	I_{OL}=2.1mA	-	-	0.4	V
I_{PP1}	Vpp Current	V_{PP}=0 ∿ VCC+0.6V	-	-	±10	μA
I_{LO}	Output Leakage Current	V_{OUT}=0.4V ∿ V_{CC}	-	-	±10	μA

A.C. CHARACTERISTICS (Ta=0 ~ 70°C, V_{CC}=5V±5%, V_{PP}=2.0V ~ V_{CC}+0.6V)

SYMBOL	PARAMETER	TMM24256BP/BF-17		TMM24256BP/BF-20		UNIT
		MIN.	MAX.	MIN.	MAX.	
t_{ACC}	Address Access Time	-	170	-	200	ns
t_{CE}	$\overline{CE}$ to Output Valid	-	170	-	200	ns
t_{OE}	$\overline{OE}$ to Output Valid	-	70	-	70	ns
t_{DF1}	$\overline{CE}$ to Output in High-Z	0	60	0	60	ns
t_{DF2}	$\overline{OE}$ to Output in High-Z	0	60	0	60	ns
t_{OH}	Output Data Hold Time	0	-	0	-	ns

A.C. TEST CONDITIONS

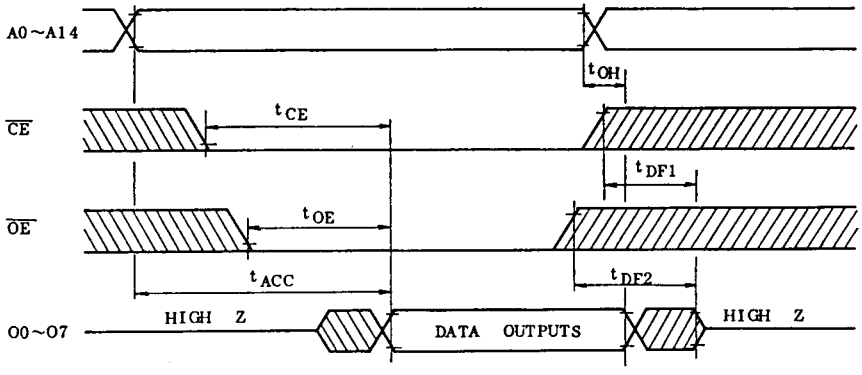
- Output Load : 1 TTL Gate and C =100pF
- Input Pulse Rise and Fall Times : 10ns Max.
- Input Pulse Levels : 0.45V ~ 2.4V
- Timing Measurement Reference Level: Inputs 0.8V and 2.0V, Outputs 0.8V and 2.0V

CAPACITANCE* (Ta=25°C, f=1MHz)

SYMBOL	PARAMETER	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
C_{IN}	Input Capacitance	V_{IN}=0V	-	4	6	pF
C_{OUT}	Output Capacitnace	V_{OUT}=0V	-	8	12	pF

* This parameter is periodically sampled and is not 100% tested.

TIMING WAVEFORMS (READ)



PROGRAM OPERATION (HIGH SPEED PROGRAMMING MODE I)

D.C. RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{IH}	Input High Voltage	2.0	-	V_{CC}+1.0	V
V_{IL}	Input Low Voltage	-0.3	-	0.8	V
V_{CC}	V_{CC} Power Supply Voltage	5.75	6.0	6.25	V
V_{PP}	V_{PP} Power Supply Voltage	12.0	12.5	13.0	V

D.C. AND OPERATING CHARACTERISTICS (Ta=25±5°C, V_{CC}=6V±0.25V, V_{PP}=12.5V±0.5V)

SYMBOL	PARAMETER	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
I_{LI}	Input Current	V_{IN}=0 ∿ V_{CC}	-	-	±10	μA
V_{OH}	Output High Voltage	I_{OH}=-400μA	2.4	-	-	V
V_{OL}	Output Low Voltage	I_{OL}=2.1mA	-	-	0.4	V
I_{CC}	V_{CC} Supply Current	-	-	-	100	mA
I_{PP2}	V_{PP} Supply Current	V_{PP}=13.0V	-	-	50	mA

A.C. PROGRAMMING CHARACTERISTICS (Ta=25±5°C, V_{CC}=6V±0.25V, V_{PP}=12.5V±0.5V)

SYMBOL	PARAMETER	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
t_{AS}	Address Setup Time	-	2	-	-	μs
t_{AH}	Address Hold Time	-	2	-	-	μs
t_{CES}	$\overline{CE}$ Setup Time	-	0	-	-	ns
t_{CEH}	$\overline{CE}$ Hold Time	-	0	-	-	ns
t_{OES}	$\overline{OE}$ Setup Time	-	2	-	-	μs
t_{DS}	Data Setup Time	-	2	-	-	μs
t_{DH}	Data Hold Time	-	2	-	-	μs
t_{VPS}	V_{PP} Setup Time	-	2	-	-	μs
t_{VCS}	V_{CC} Setup Time	-	2	-	-	μs
t_{PW}	Initial Program Pulse Width	$\overline{CE}$=V_{IL}, $\overline{OE}$=V_{IH}	0.95	1.0	1.05	ms
t_{OPW}	Overprogram Pulse Width	Note 1	2.85	3.0	78.75	ms
t_{OE}	$\overline{OE}$ to Output Valid	$\overline{CE}$=V_{IH}	-	-	150	ns
t_{DFP}	$\overline{OE}$ to Output in High-Z	$\overline{CE}$=V_{IH}	-	-	130	ns

A.C. TEST CONDITIONS

- Output Load : 1 TTL Gate and C_L (100pF)
- Input Pulse Rise and Fall Times : 10ns Max.
- Input Pulse Levels : 0.45V ∿ 2.4V
- Timing Measurement Reference Level: Input 0.8V and 2.0V, Output 0.8V and 2.0V

Note 1: The length of the overprogram pulse may vary as a function of the counter value X.

PROGRAM OPERATION (HIGH SPEED PROGRAMMING MODE II)

D.C. RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{IH}	Input High Voltage	2.0	-	V_{CC}+1.0	V
V_{IL}	Input Low Voltage	-0.3	-	0.8	V
V_{CC}	V_{CC} Power Supply Voltage	6.0	6.25	6.5	V
V_{PP}	V_{PP} Power Supply Voltage	12.5	12.75	13.0	V

D.C. AND OPERATING CHARACTERISTICS (Ta=25±5°C, V_{CC}=6.25V±0.25V, V_{PP}=12.75V±0.25V)

SYMBOL	PARAMETER	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
I_{LI}	Input Current	V_{IN}=0 ∿ V_{CC}	-	-	±10	μA
V_{OH}	Output High Voltage	I_{OH}=-400μA	2.4	-	-	V
V_{OL}	Output Low Voltage	I_{OL}=2.1mA	-	-	0.4	V
I_{CC}	V_{CC} Supply Current	-	-	-	100	mA
I_{PP2}	V_{PP} Supply Current	V_{PP}=13.0V	-	-	50	mA

A.C. PROGRAMMING CHARACTERISTICS (Ta=25±5°C, V_{CC}=6.25V±0.25V, V_{PP}=12.75V±0.25V)

SYMBOL	PARAMETER	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
t_{AS}	Address Setup Time	-	2	-	-	μs
t_{AH}	Address Hold Time	-	2	-	-	μs
t_{CES}	$\overline{CE}$ Setup Time	-	0	-	-	ns
t_{CEH}	$\overline{CE}$ Hold Time	-	0	-	-	ns
t_{OES}	$\overline{OE}$ Setup Time	-	2	-	-	μs
t_{DS}	Data Setup Time	-	2	-	-	μs
t_{DH}	Data Hold Time	-	2	-	-	μs
t_{VPS}	V_{PP} Setup Time	-	2	-	-	μs
t_{VCS}	V_{CC} Setup Time	-	2	-	-	μs
t_{PW}	Program Pulse Width	$\overline{CE}$=V_{IL}, $\overline{OE}$=V_{IH}	0.095	0.1	0.105	ms
t_{OE}	$\overline{OE}$ to Output Valid	$\overline{CE}$=V_{IH}	-	-	150	ns
t_{DFP}	$\overline{OE}$ to Output in High-Z	$\overline{CE}$=V_{IH}	-	-	130	ns

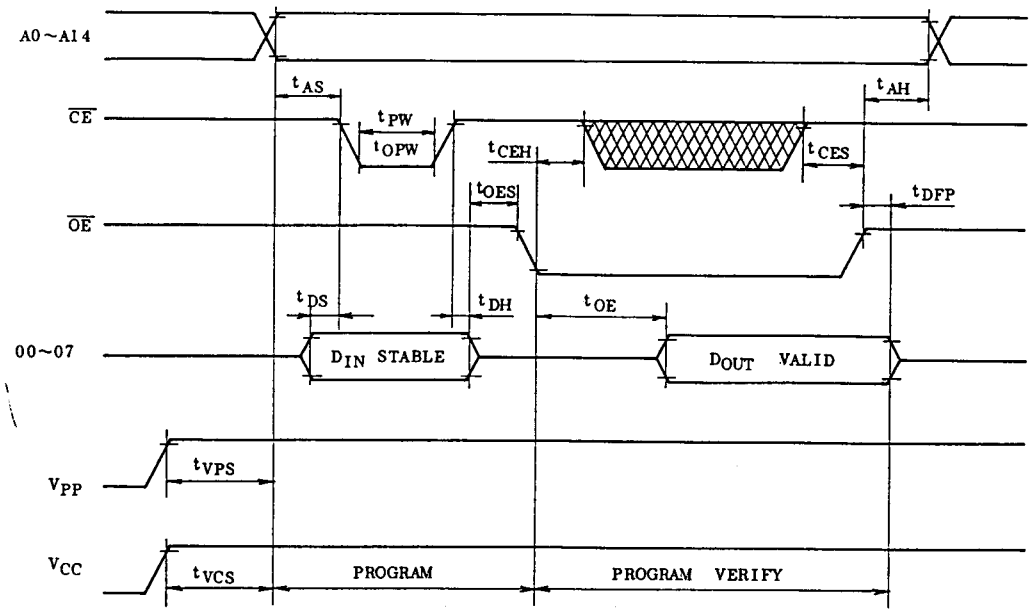
A.C. TEST CONDITIONS

- Output Load : 1 TTL Gate cnd C_L (100pF)
- Input Pulse Rise and Fall Times : 10ns Max.
- Input Pulse Levels : 0.45V ∿ 2.4V
- Timing Measurement Reference Level: Input 0.8V and 2.0V, Output 0.8V and 2.0V

TIMING WAVEFORMS (PROGRAM)

HIGH SPEED PROGRAMMING MODE I (V_{CC}=6V±0.25V, V_{PP}=12.5V±0.5V)

HIGH SPEED PROGRAMMING MODE II (V_{CC}=6.25V±0.25V, V_{PP}=12.75V±0.25V)



Note 1. V_{CC} must be applied simultaneously or before V_{PP} and cut off simultaneously or after V_{PP}.

2. Removing the device from socket and setting the device in socket with V_{PP}=12.5V±0.5V or V_{PP}=12.75V±0.25V may cause permanent damage to the device.

3. The V_{PP} supply voltage is permitted up to 14V for program operation. So the voltage over 14V should not be applied to the Vpp terminal. When the switching pulse voltage is applied to the V_{PP} terminal, the overshoot voltage of its pulse should not be exceeded 14V.

OPERATION INFORMATION

The TMM24256BP/BF's six operation modes are listed in the following table. Mode selection can be achieved by applying TTL level signal to all inputs.

MODE \ PIN-NAME (NUMBER)		$\overline{CE}$ (20)	$\overline{OE}$ (22)	V_{PP} (1)	V_{CC} (28)	O0 ∿ O7 (11 ∿ 13, 15 ∿ 19)	POWER
Read Operation (Ta=0 ∿ 70°C)	Read	L	L	5V	5V	Data Out	Active
	Output Deselect	*	H			High Impedance	
	Standby	H	*			High Impedance	Standby
Program Operation (Ta=25±5°C)	Program	L	H	1) 12.5V	1) 6V	Data In	Active
	Program Inhibit	H	H			High Impedance	
	Program Verify	*	L	2) 12.75V	2) 6.25V	Data Out	

Note: H; V_{IH}, L; V_{IL}, *; V_{IH} or V_{IL}

1); HIGH SPEED PROGRAMMING MODE I

2); HIGH SPEED PROGRAMMING MODE II

READ MODE

The TMM24256BP/BF has two control functions. The chip enable ($\overline{CE}$) controls the operation power and should be used for device selection.
The output enable ($\overline{OE}$) control the output buffers, independent of device selection.
Assuming the $\overline{CE}$=$\overline{OE}$=V_{IL}, the output data is valid at the outputs after address access time from stabilizing of all addresses.
The $\overline{CE}$ to output valid (t_{CE}) is equal to the address access time (t_{ACC}).
Assuming that $\overline{CE}$=V_{IL} and all addresses are valid, the output data is valid at the outputs after t_{OE} from the falling edge of $\overline{OE}$.

OUTPUT DESELECT MODE

Assuming that $\overline{CE}$=V_{IH} or $\overline{OE}$=V_{IH}, the outputs will be in high impedance state. So two or more TMM24256BP/BF's can be connected together on a common bus line.
When $\overline{CE}$ is decoded for device selection, all deselected devices are in low power standby mode.

STANDBY MODE

The TMM24256BP/BF has a low power standby mode controlled by the $\overline{CE}$ signal. By applying a high level to the $\overline{CE}$ input, the TMM24256BP/BF is placed in the standby mode which reduce the operating current to 30mA from 100mA (about 70% reduction) by applying TTL-high level and then the outputs are in a high impedance state, independent of the $\overline{OE}$ inputs.

PROGRAM MODE

Initially, when received by customers, all bits of the TMM24256BP/BF are in the "1" state which is erased state.
Therefore the program operation is to introduce "0's" data into the desired bit locations by electrically programming.
The TMM24256BP/BF is in the programming mode when the V_{PP} input is at 12.5V or 12.75V and $\overline{CE}$ is at TTL-Low level under $\overline{OE}=V_{IH}$.
The TMM24256BP/BF can be programmed any location at anytime either individually, sequentially, or at random.

PROGRAM VERIFY MODE

The verify mode is to check that desired data is correctly programmed on the programmed bits.
The verify is accomplished with $\overline{OE}$ at V_{IL} and $\overline{CE}$ at V_{IH} or V_{IL}.

PROGRAM INHIBIT MODE

Under the condition that the program voltage (12.5V or 12.75V) is applied to V_{PP} terminal, a TTL high level $\overline{CE}$ input inhibits the TMM24256BP/BF from being programmed.
Programming of two or more TMM24256BP/BF's in parallel with different data is easily accomplished. That is, all inputs except for $\overline{CE}$ and $\overline{OE}$ may be commonly connected, and a TTL Low level program pulse is applied to the $\overline{CE}$ of the desired device only and TTL high level signal is applied to the other devices.

HIGH SPEED PROGRAMMING MODE I

This high speed programming mode I is performed at V_{CC}=6.0V and V_{PP}=12.5V. The programming is achieved by applying a single TTL low level 1ms pulse to the $\overline{CE}$ input after addresses and data are stable. Then the programmed data is verified by using Program Verify Mode.

If the programmed data is not correct, another program pulse of 1ms is applied and then the programmed data is verified. This should be repeated until the program operates correctly (max. 25 times).

After correctly programming the selected address, the additional program pulse with pulse width 3 times that needed for initial programming is applied.

When programming has been completed, the data in all addresses should be verified with V_{CC}=V_{PP}=5V.

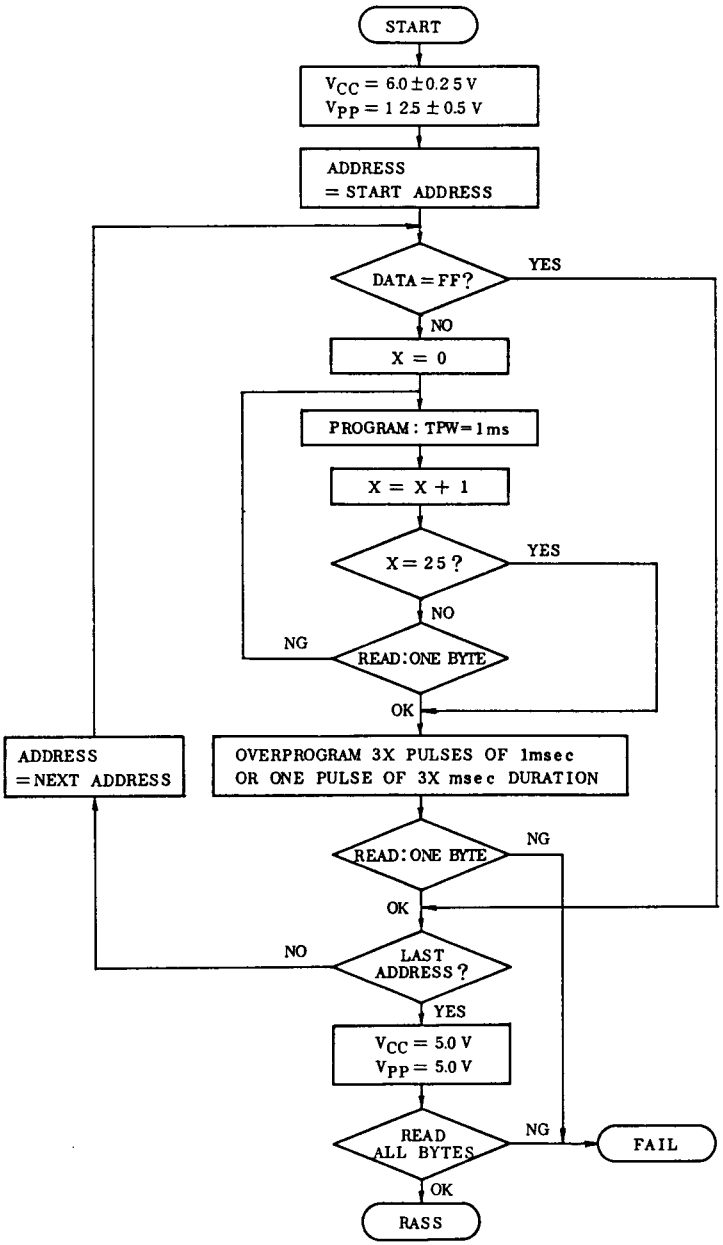
HIGH SPEED PROGRAMMING MODE II

The program time can be greatly decreased by using this high speed programming mode II. This high speed programming mode II is performed at V_{CC}=6.25V and V_{PP}=12.75V. The programming is achieved by applying a single TTL low level 0.1ms pulse to the $\overline{CE}$ input after addresses and data are stable. Then the programmed data is verified by using Program Verify Mode.

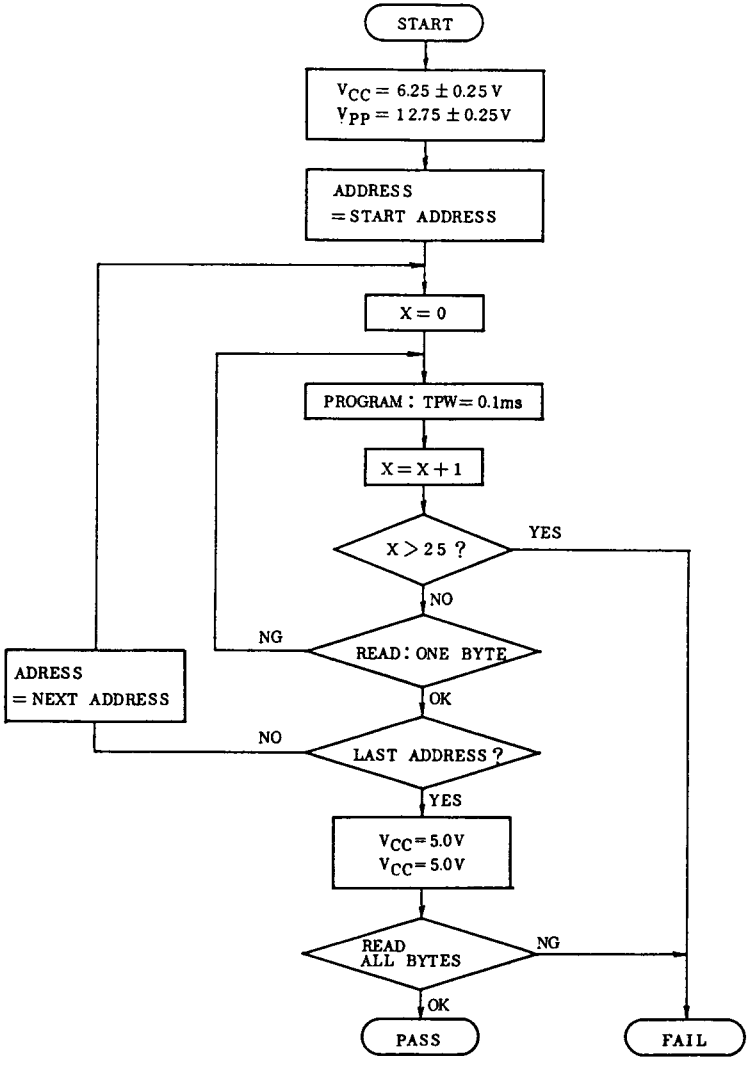
If the programmed data is not correct, another program pulse of 0.1ms is applied and then the programmed data is verified. This should be repeated until the program operates correctly (max. 25 times).

When programming has been completed, the data in all addresses should be verified with V_{CC}=V_{PP}=5V.

HIGH SPEED PROGRAMMING MODE I FLOW CHART



HIGH SPEED PROGRAMMING MODE II FLOW CHART



ELECTRIC SIGNATURE MODE

Electric signature mode allows to read out a code from TMM24256BP/BF which identifies its manufacturer and device type.

The programming equipment may read out manufacturer code and device code from TMM24256BP/BF by using this mode before program operation and automatically set program voltage (Vpp) and algorithm.

Electric Signature mode is set up when 12V is applied to address line A9 and the rest of address lines is set to V_{IL} in read operation. Data ouptut in this conditions is manufacturer code. Device code is identified when address A0 is set to V_{IH}. These two codes possess an odd parity with the parity bit of MSB (O7).

The following table shows electric signature of TMM24256BP/BF.

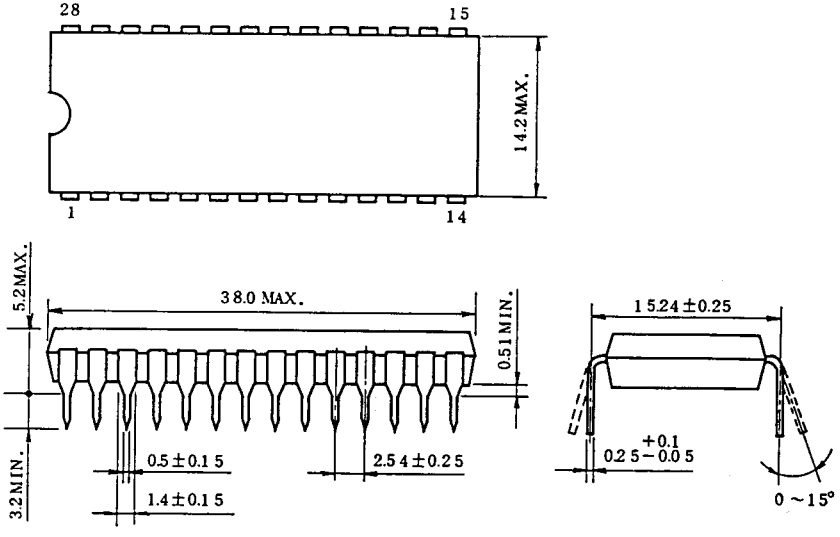
PINS / SIGNATURE	A0 (10)	O7 (19)	O6 (18)	O5 (17)	O4 (16)	O3 (15)	O2 (13)	O1 (12)	O0 (11)	HEX. DATA
Manufacture Code	V_{IL}	1	0	0	1	1	0	0	0	98
Device Code	V_{IH}	0	1	0	1	0	1	0	0	54

Notes: A9=12V±0.5V

A1 ∿ A8, A10 ∿ A14, $\overline{CE}$, $\overline{OE}$=V_{IL}

OUTLINE DRAWINGS (TMM24256BP)

Unit in mm



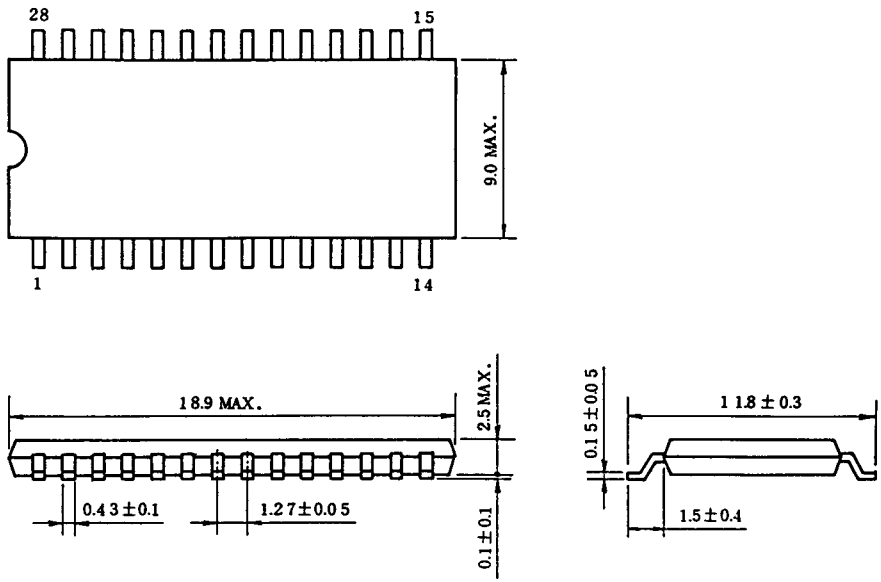
Note 1. Each lead pitch is 2.54mm. All leads are located within 0.25mm of their true longitudinal position with respect No.1 and No.28 leads.

2. This value is measured at the end of leads.

3. All dimensions are in millimeters.

OUTLINE DRAWINGS (TMM24256BF)

Unit in mm



Note: Lead pitch is 1.27 and tolerance is ±0.12 against theoretical center of each lead that is obtained on the basis of No.1 and No.28 leads.