



Am29C821A/Am29C823A

High-Performance CMOS Bus Interface Registers

DISTINCTIVE CHARACTERISTICS

- Proprietary edge-rate controlled outputs dramatically reduce undershoots, overshoots and ground bounce
- High-speed parallel positive edge-triggered registers with D-type flip-flops
 - CP-Y propagation delay = 5 ns typical
- Low standby power
- Very high output drive
 - I_{OL} = 48 mA Commercial, 32 mA Military
- Extra-wide (9- and 10-bit) data paths
- Power-up/down disable circuit provides for glitch-free power supply sequencing
- Can be powered off while in 3-state, ideal for card edge interface applications
- Minimal speed degradation with multiple outputs switching
- JEDEC FCT-compatible specs

GENERAL DESCRIPTION

The Am29C821A and Am29C823A CMOS Bus Interface Registers are designed to eliminate the extra devices required to buffer stand alone registers and to provide extra data width for wider address/data paths or buses carrying parity. The Am29C800A registers are produced with AMD's exclusive CMOS process, and feature typical propagation delays of 5 ns, as well as an output current drive of 48 mA.

The Am29C821A is a buffered, 10-bit version of the popular '374/'534 function. The Am29C823A is a 9-bit buffered register with Clock Enable (\overline{EN}) and Clear (\overline{CLR})—ideal for parity bus interfacing in high-performance microprogrammed systems.

The Am29C821A and Am29C823A incorporate AMD's proprietary edge-controlled outputs in order to minimize simultaneous switching noise (ground bounce), undershoots and overshoots. By controlling the output transient currents, ground bounce and output ringing have

been greatly reduced. A modified AMD output provides a stable, usable voltage level in less time than a non-controlled output.

Additionally, speed degradation due to increasing number of outputs switching is reduced. Together, these benefits of edge-rate control result in significant increase in system performance despite a minor increase in device propagation delay.*

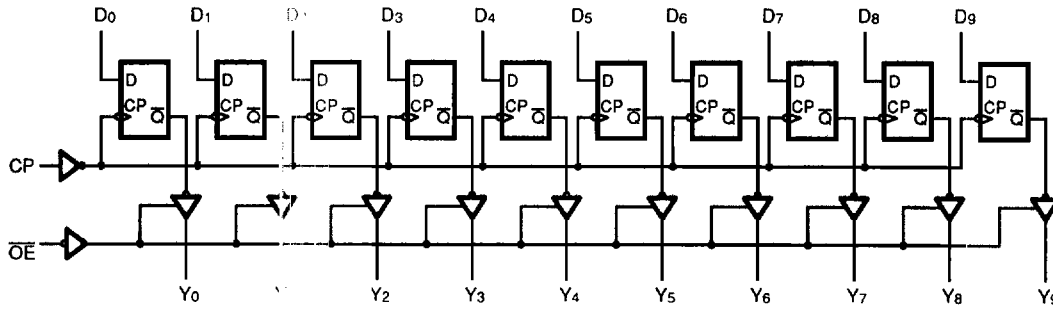
A unique I/O circuitry, which utilizes n-channel pull-up transistors (eliminating the parasitic diode to V_{CC}), provides for high-impedance outputs during power-off and power-up/down sequencing, thus providing glitch-free operation for card-edge and other active bus applications.

The Am29C821A and Am29C823A are available in the standard package options: DIPs, PLCCs, and SOICs.

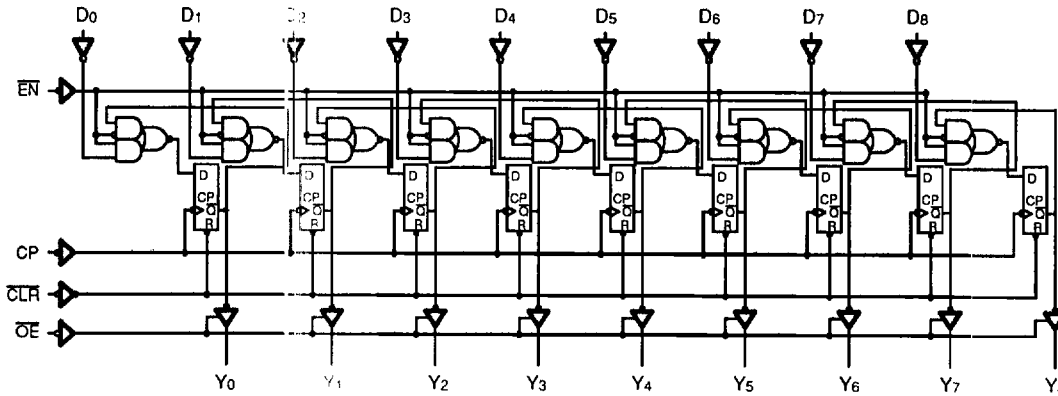
*For more details refer to a Minimization of Ground Bounce Through Output Edge-Rate Control Application Note (See Chapter 3).



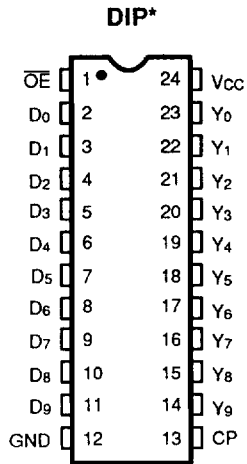
BLOCK DIAGRAMS
Am29C821A



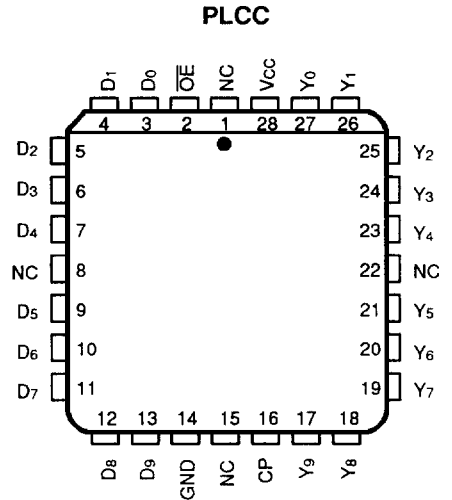
Am29C823A



CONNECTION DIAGRAMS (Top View)
Am29C821A

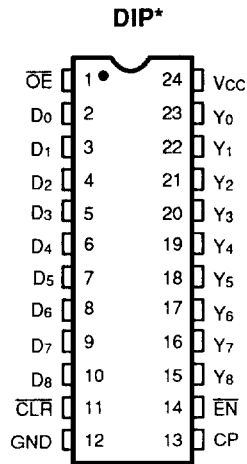


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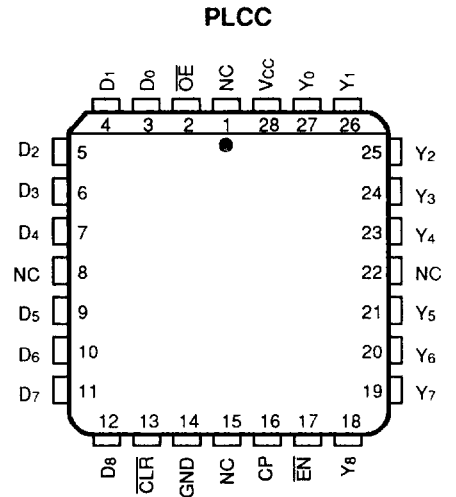


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Am29C823A



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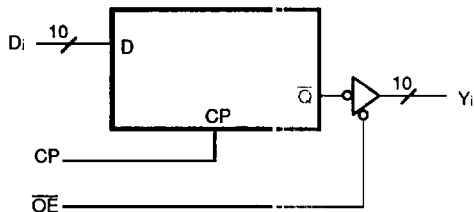


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*Also available in 24-Pin Small Outline package; pinout identical to DIPs.

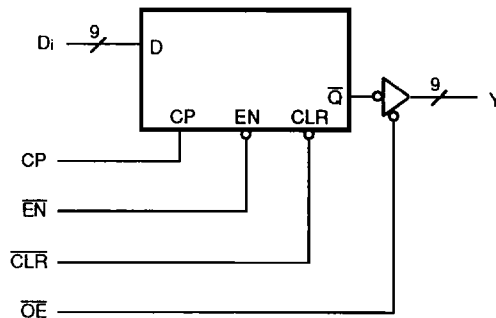
LOGIC SYMBOLS

Am29C821A



11227-007A

Am29C823A



11227-008A

FUNCTION TABLES

Am29C821A

Inputs			Internal	Outputs	Function
\overline{OE}	D	CP	\overline{Q}_i	Y_i	
H	L	\uparrow	H	Z	Hi-Z
H	H	\uparrow	L	Z	
L	L	\uparrow	H	L	Load
L	H	\uparrow	L	H	

Am29C823A

Inputs					Internal	Outputs	Function
\overline{OE}	\overline{CLR}	\overline{EN}	D_i	CP	\overline{Q}_i	Y_i	
H	H	L	L	\uparrow	H	Z	Hi-Z
H	H	L	H	\uparrow	L	Z	
H	L	X	X	X	H	Z	Clear
L	L	X	X	X	H	L	
H	H	H	X	X	NC	Z	Hold
L	H	H	X	X	NC	NC	
H	H	L	L	\uparrow	H	Z	Load
H	H	L	H	\uparrow	L	Z	
L	H	L	L	\uparrow	H	L	
L	H	L	H	\uparrow	L	H	

H = HIGH
L = LOW
X = Don't Care

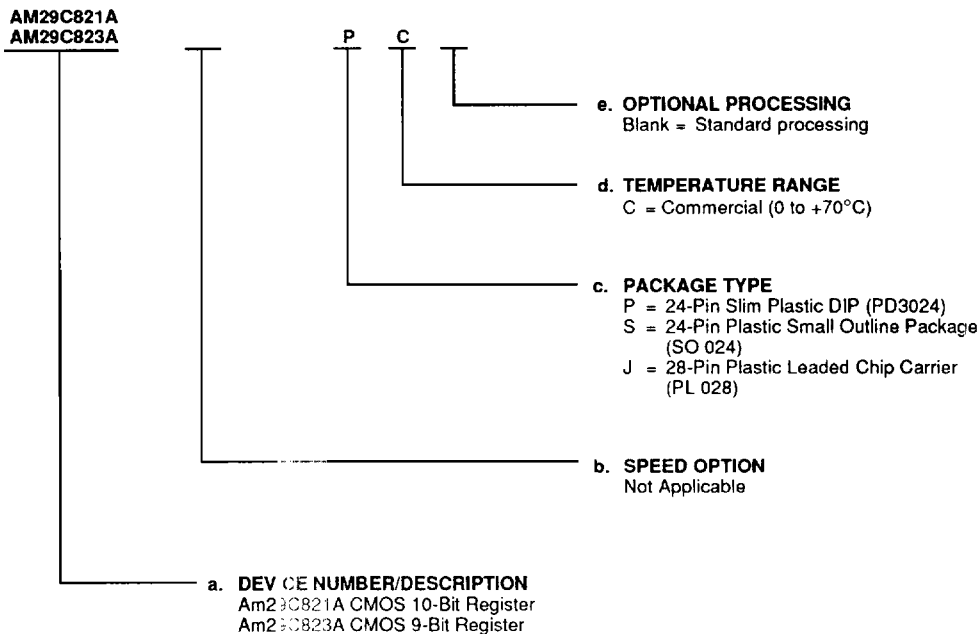
NC = No Change
 \uparrow = LOW-to-HIGH Transition
Z = High Impedance

ORDERING INFORMATION

Standard Products

AMD standard products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of:

- a. Device Number
- b. Speed Option (if applicable)
- c. Package Type
- d. Temperature Range
- e. Optional Processing



Valid Combinations	
AM29C821A	PC, SO, JC
AM29C823A	

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations or to check on newly released combinations, and to obtain additional data on AMD's standard military grade products.

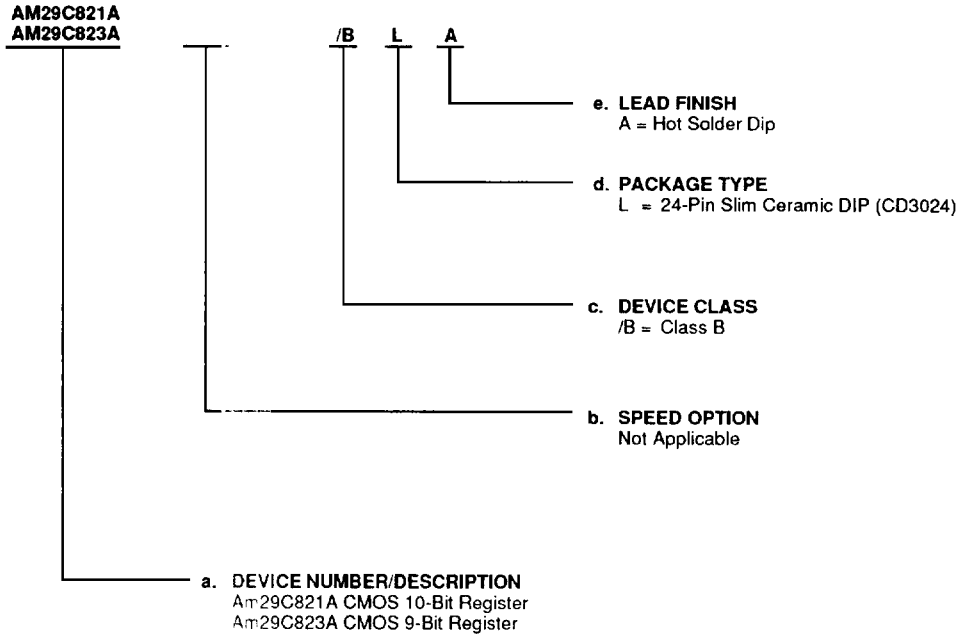


MILITARY ORDERING INFORMATION

APL Products

AMD products for Aerospace and Defense applications are available in several packages and operating ranges. APL (Approved Products List) products are fully compliant with MIL-STD-883C requirements. The order number (Valid Combination) is formed by a combination of:

- a. Device Number
- b. Speed Option (if applicable)
- c. Device Class
- d. Package Type
- e. Lead Finish



Valid Combinations	
AM29C821A	-BLA
AM29C823A	

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations, or to check on newly released combinations.

Group A Tests

Group A tests consist of Subgroups 1, 2, 3, 7, 8, 9, 10, 11.

PIN DESCRIPTION**Am29C821A/Am29C823A** **D_i** **Data Input (Input)** D_i are the register data inputs. **CP** **Clock Pulse (Input, LOW-to-HIGH Transition)**

Clock Pulse is the clock input for the registers. Data is entered into the registers on the LOW-to-HIGH transitions.

 Y_i **Data Outputs (Output)** Y_i are the three-state outputs. **\overline{OE}** **Output Enable (Input, Active LOW)**When the \overline{OE} input is HIGH, the Y_i outputs are in the high-impedance state. When \overline{OE} is LOW, the register data is present at the Y_i outputs.**Am29C823A only** **\overline{EN}** **Clock Enable (Input, Active LOW)**When \overline{EN} is LOW, data on the D_i inputs are transferred to the Q_i outputs on the LOW-to-HIGH clock transition. When \overline{EN} is HIGH, the Q_i outputs do not change state, regardless of the data or clock input transitions. **\overline{CLR}** **Clear (Input, Active LOW)**When \overline{CLR} is LOW, the internal register is cleared. When \overline{CLR} is LOW and \overline{OE} is LOW, the Q_i outputs are HIGH. When \overline{CLR} is HIGH, data can be entered into the register.

ABSOLUTE MAXIMUM RATINGS

Storage Temperature	-65 to +150°C
Supply Voltage to Ground Potential Continuous	-0.5 V to +7.0 V
DC Output Voltage	-0.5 V to +6.0 V
DC Input Voltage	-0.5 V to +6.0 V
DC Output Diode Current:	
Into Output	+50 mA
Out of Output	-50 mA
DC Input Diode Current:	
Into Input	+20 mA
Out of Input	-20 mA
DC Output Current:	
Into Output	+100 mA
Out of Output	-100 mA
Total DC Ground Current	
(n x I _{OL} + m x I _{OCT}) mA (Note 1)	
Total DC V _{CC} Current	
(n x I _{OH} + m x I _{OCT}) mA (Note 1)	

Note:

1. n = number of outputs, m = number of inputs.

Stresses above those listed under Absolute Maximum Ratings may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

OPERATING RANGES

Commercial (C) Devices

Ambient Temperature (T _A)	0 to +70°C
Supply Voltage (V _{CC})	+4.5 to +5.5 V

Military (M) Devices

Ambient Temperature (T _A)	-55 to +125°C
Supply Voltage (V _{CC})	+4.5 to +5.5 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

**DC CHARACTERISTICS over operating ranges unless otherwise specified
(for APL Products, Group A, Subgroups 1, 2, 3 are tested unless otherwise noted)**

Parameter Symbol	Parameter Description	Test Conditions		Min.	Max.	Unit
V _{OH}	Output HIGH Voltage	V _{CC} = 4.5 V V _{IN} = V _{IH} or V _{IL}	I _{OH} = -15 mA	2.4		V
V _{OL}	Output LOW Voltage	V _{CC} = 4.5 V V _{IN} = V _{IH} or V _{IL}	MIL I _{OL} = 32 mA		0.5	V
			COM'L I _{OL} = 48 mA		0.5	V
V _{IH}	Input HIGH Voltage	Guaranteed Input Logical HIGH Voltage for All Inputs (Note 1)		2.0		V
V _{IL}	Input LOW Voltage	Guaranteed Input Logical LOW Voltage for All Inputs (Note 1)			0.8	V
V _I	Input Clamp Voltage	V _{CC} = 4.5 V, I _{IN} = -18 mA			-1.2	V
I _{IL}	Input LOW Current	V _{CC} = 5.5 V, V _{IN} = GND			-5	μA
I _{IH}	Input HIGH Current	V _{CC} = 5.5 V, V _{IN} = 5.5 V			5	μA
I _{ozH}	Output Off-State Current (High Impedance)	V _{CC} = 5.5 V, V _O = 5.5 V			+10	μA
I _{ozL}		V _{CC} = 5.5 V, V _O = GND			-10	μA
I _{sc}	Output Short-Circuit Current	V _{CC} = 5.5 V, V _O = 0 V (Note 2)		-60		mA
I _{ccQ}	Static Supply Current	V _{CC} = 5.5 V Outputs Open	V _{IN} = V _{CC} or GND	MIL	1.5	mA
I _{ccT}			V _{IN} = 3.4 V	COM'L	1.2	
				Data Input	1.5	mV/Bit
	OE, CLR, CP, EN	3.0				
I _{ccdT}	Dynamic Supply Current	V _{CC} = 5.5 V (Note 3)		Outputs Open	275	μA/MHz/Bit
				Outputs Loaded	400	

Notes:

1. Input thresholds are tested in combination with other DC parameters or by correlation.
 2. Not more than one output shorted at a time. Duration should not exceed 100 milliseconds.
 3. Measured at a frequency ≤ 10 MHz; with 50% duty cycle.
- † Not included in Group A tests.



SWITCHING CHARACTERISTICS for light capacitive loading over operating ranges unless otherwise specified (for APL Products, Group A, Subgroups 9, 10, 11 are tested unless otherwise noted)

Symbol	Parameter Description	Test Conditions*	Commercial		Military		Unit	
			Min.	Max.	Min.	Max.		
t _{PLH}	Propagation Delay Clock to Y _i	C _L = 50 pF R ₁ = 500 Ω R ₂ = 500 Ω	2	8.5	2	9.5	ns	
t _{PHL}	(\overline{OE} = LOW) (Note 1)		3	8.5	3	9.5	ns	
t _S	Data to CP Setup Time		3		3		ns	
t _H	Data to CP Hold Time		2		2		ns	
t _S	Enable (\overline{EN}) to CP Setup Time		4		4		ns	
t _S	Enable (\overline{EN}) to CP Setup Time		4		4		ns	
t _H	Enable (\overline{EN}) Hold Time		0		0		ns	
t _{PHL}	Propagation Delay, Clear to Y _i		3	10	3	10.5	ns	
t _{REC}	Clear (\overline{CLR}) to CP Setup Time		6		6		ns	
t _{PWH}	Clock Pulse Width		HIGH	6		6		ns
t _{PWL}			LOW	6		6		ns
t _{PWL}	Clear Pulse Width		LOW	6		6		ns
t _{ZH}	Output Enable Time: \overline{OE} to Y _i		1	8.5	1	9	ns	
t _{ZL}			3	12	3	13	ns	
t _{HZ}	Output Disable Time: \overline{OE} to Y _i		2	8	2	8.5	ns	
t _{LZ}			2	8	2	8.5	ns	

SWITCHING CHARACTERISTICS for heavy capacitive loading over operating ranges unless otherwise specified (Note 2)

Symbol	Parameter Description	Test Conditions*	Commercial		Military		Unit
			Min.	Max.	Min.	Max.	
t _{PLH}	Propagation Delay Clock to Y _i	C _L = 300 pF R ₁ = 500 Ω R ₂ = 500 Ω	2	15.5	2	17.5	ns
t _{PHL}	(\overline{OE} = LOW) (Note 1)		3	15.5	3	17.5	ns
t _{ZH}	Output Enable Time: \overline{OE} to Y _i		2	15	2	15.5	ns
t _{ZL}			3	18.5	3	19.5	ns
t _{HZ}	Output Disable Time: \overline{OE} to Y _i	C _L = 5 pF R ₁ = 500 Ω R ₂ = 500 Ω	2	6.5	2	7	ns
t _{LZ}		2	6.5	2	7	ns	

*See Test Circuit and Waveforms listed in Chapter 2.

Notes:

- For more details refer to a Minimization of Ground Bounce Through Output Edge-Rate Control Application Note (See Chapter 3).
- These parameters are guaranteed by characterization but not production tested.