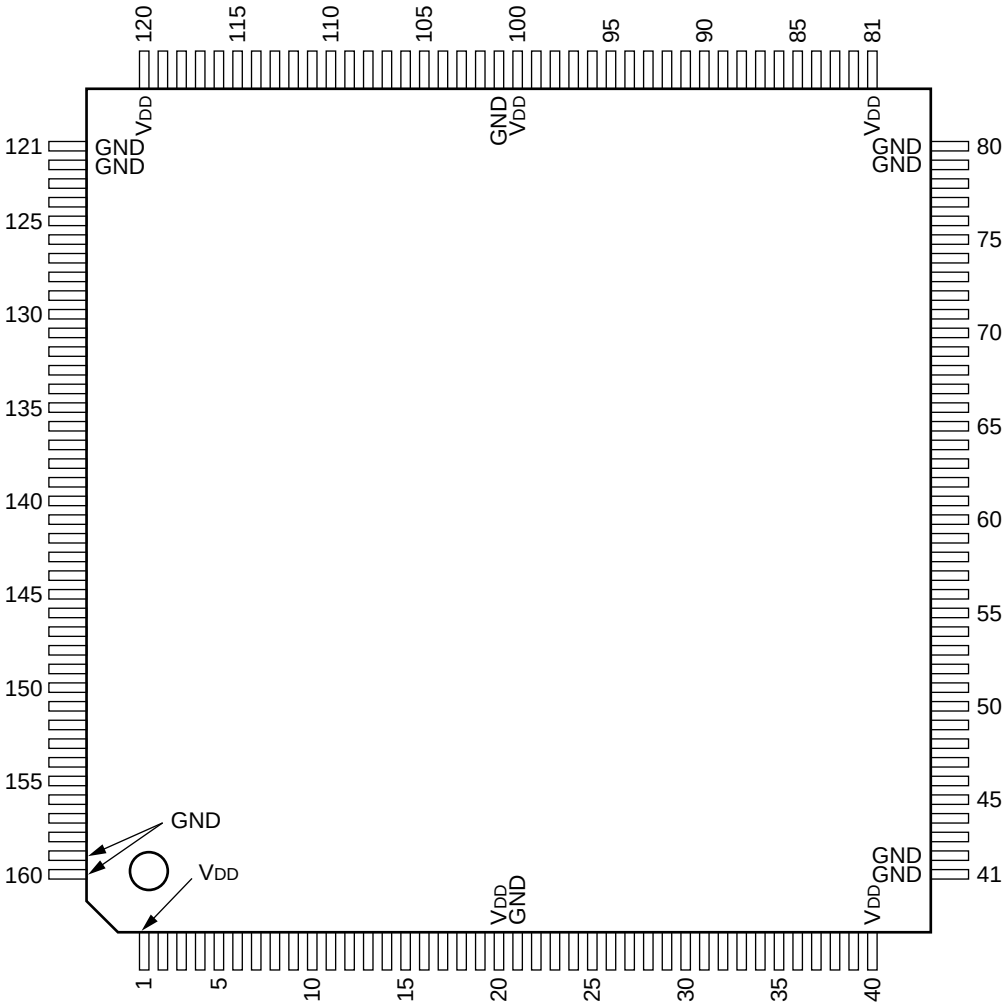
C-MOS VITERBI AND INNER DECODER

—TOP VIEW—



PIN NO.	I/O	SIGNAL	PIN NO.	I/O	SIGNAL	PIN NO.	I/O	SIGNAL	PIN NO.	I/O	SIGNAL
1	—	VDD	41	—	GND	81	—	VDD	121	—	GND
2	I	VID0	42	—	GND	82	I	VIA0	122	—	GND
3	I	VID1	43	I	CK27	83	I	VIA1	123	I	BYB0
4	I	VID2	44	I	SMC	84	I	VIA2	124	I	BYB1
5	I	VID3	45	I	RESET	85	I	VIA3	125	I	BYB2
6	I	VID4	46	O	PRTY	86	I	VIA4	126	I	BYB3
7	I	VID5	47	I	TMC1	87	I	VIA5	127	I	BYB4
8	I	CKVD	48	I	TMC2	88	I	CKVA	128	I	BYB5
9	I	SWPD	49	O	OUT0	89	I	SWPA	129	I	BYB6
10	O	PED0	50	O	OUT1	90	O	PEA0	130	I	BYB7
11	O	PED1	51	O	OUT2	91	O	PEA1	131	I	BYSTB
12	O	PED2	52	O	OUT3	92	O	PEA2	132	I	BYA0
13	O	PED3	53	O	OUT4	93	O	PEA3	133	I	BYA1
14	O	GED0	54	O	OUT5	94	O	GEA0	134	I	BYA2
15	O	GED1	55	O	OUT6	95	O	GEA1	135	I	BYA3
16	O	VSOD	56	O	OUT7	96	O	VSOA	136	I	BYA4
17	O	CKSD	57	O	STP	97	O	CKSA	137	I	BYA5
18	O	CKPDO	58	I	MDTES	98	O	CKPAO	138	I	BYA6
19	I	CKPDI	59	I	AMC	99	I	CKPAI	139	I	BYA7
20	—	VDD	60	I	SCK	100	—	VDD	140	I	BYSTA
21	—	GND	61	I/O	BUS0	101	—	GND	141	I	BYC0
22	I	VIC0	62	I/O	BUS1	102	I	VIB0	142	I	BYC1
23	I	VIC1	63	I/O	BUS2	103	I	VIB1	143	I	BYC2
24	I	VIC2	64	I/O	BUS3	104	I	VIB2	144	I	BYC3
25	I	VIC3	65	I/O	BUS4	105	I	VIB3	145	I	BYC4
26	I	VIC4	66	I/O	BUS5	106	I	VIB4	146	I	BYC5
27	I	VIC5	67	I/O	BUS6	107	I	VIB5	147	I	BYC6
28	I	CKVC	68	I/O	BUS7	108	I	CKVB	148	I	BYC7
29	I	SWPC	69	I	STT0	109	I	SWPB	149	I	BYSTC
30	O	PEC0	70	I	STT1	110	O	PEB0	150	I	BYD0
31	O	PEC1	71	I	STRB	111	O	PEB1	151	I	BYD1
32	O	PEC2	72	I	SCS	112	O	PEB2	152	I	BYD2
33	O	PEC3	73	I	EEIA	113	O	PEB3	153	I	BYD3
34	O	GEC0	74	I	EEIB	114	O	GEB0	154	I	BYD4
35	O	GEC1	75	I	EEIC	115	O	GEB1	155	I	BYD5
36	O	VSOC	76	I	EEID	116	O	VSOB	156	I	BYD6
37	O	CKSC	77	I	EEIP	117	O	CKSB	157	I	BYD7
38	O	CKPCO	78	I	CKEE	118	O	CKPBO	158	I	BYSTD
39	I	CKPCI	79	—	GND	119	I	CKPBI	159	—	GND
40	—	VDD	80	—	GND	120	—	VDD	160	—	GND

INPUT

AMC	;	SCAN TEST
BYA0 - BYA7	;	CH-A BYPASS DATA
BYB0 - BYB7	;	CH-B BYPASS DATA
BYC0 - BYC7	;	CH-C BYPASS DATA
BYD0 - BYD7	;	CH-D BYPASS DATA
BYSTA	;	CH-A BYPASS START PULSE
BYSTB	;	CH-B BYPASS START PULSE
BYSTC	;	CH-C BYPASS START PULSE
BYSTD	;	CH-D BYPASS START PULSE
CK27	;	27MHz CLOCK
CKEE	;	EE CLOCK
CKPAI	;	CH-A PARALLEL CLOCK
CKPBI	;	CH-B PARALLEL CLOCK
CKPCI	;	CH-C PARALLEL CLOCK
CKPDI	;	CH-D PARALLEL CLOCK
CKVA	;	CH-A VITERBI CLOCK
CKVB	;	CH-B VITERBI CLOCK
CKVC	;	CH-C VITERBI CLOCK
CKVD	;	CH-D VITERBI CLOCK
EEIA - EEID	;	EE DATA
EEIP	;	EE PARITY
MDTES	;	TEST MODE
RESET	;	CHIP RESET
SCK	;	SCAN TEST
SCS	;	CPU INTERFACE CHIP SELECT
SMC	;	SCAN TEST
STRB	;	CPU INTERFACE STROBE
STT0, STT1	;	CPU INTERFACE STATUS
SWPA	;	CH-A SWITCHING PULSE
SWPB	;	CH-B SWITCHING PULSE
SWPC	;	CH-C SWITCHING PULSE
SWPD	;	CH-D SWITCHING PULSE
TMC1 - TMC2	;	TEST MODE
VIA0 - VIA5	;	CH-A VITERBI DATA
VIB0 - VIB5	;	CH-B VITERBI DATA
VIC0 - VIC5	;	CH-C VITERBI DATA
VID0 - VID5	;	CH-D VITERBI DATA

OUTPUT

CKPAO	;	CH-A VITERBI PARALLEL CLOCK
CKPBO	;	CH-B VITERBI PARALLEL CLOCK
CKPCO	;	CH-C VITERBI PARALLEL CLOCK
CKPDO	;	CH-D VITERBI PARALLEL CLOCK
CKSA	;	CH-A VITERBI SERIAL CLOCK
CKSB	;	CH-B VITERBI SERIAL CLOCK
CKSC	;	CH-C VITERBI SERIAL CLOCK
CKSD	;	CH-D VITERBI SERIAL CLOCK
GEA0, GEA1	;	CH-A GAIN ERROR
GEB0, GEB1	;	CH-B GAIN ERROR
GEC0, GEC1	;	CH-C GAIN ERROR
GED0, GED1	;	CH-D GAIN ERROR
OUT0 - OUT7	;	INNER DATA
PEA0 - PEA3	;	CH-A PHASE ERROR
PEB0 - PEB3	;	CH-B PHASE ERROR
PEC0 - PEC3	;	CH-C PHASE ERROR
PED0 - PED3	;	CH-D PHASE ERROR
PRTY	;	INNER PARITY
STP	;	INNER SYNC
VSOA	;	CH-A VITERBI DATA
VSOB	;	CH-B VITERBI DATA
VSOC	;	CH-C VITERBI DATA
VSOD	;	CH-D VITERBI DATA

INPUT/OUTPUT

BUS0 - BUS7	;	CPU INTERFACE DATA