Preliminary

OKI Semiconductor

This version: Nov. 1997
Previous version: Jul. 1996

MSM9201-xx

Fluorescent Display Tube Controller Driver

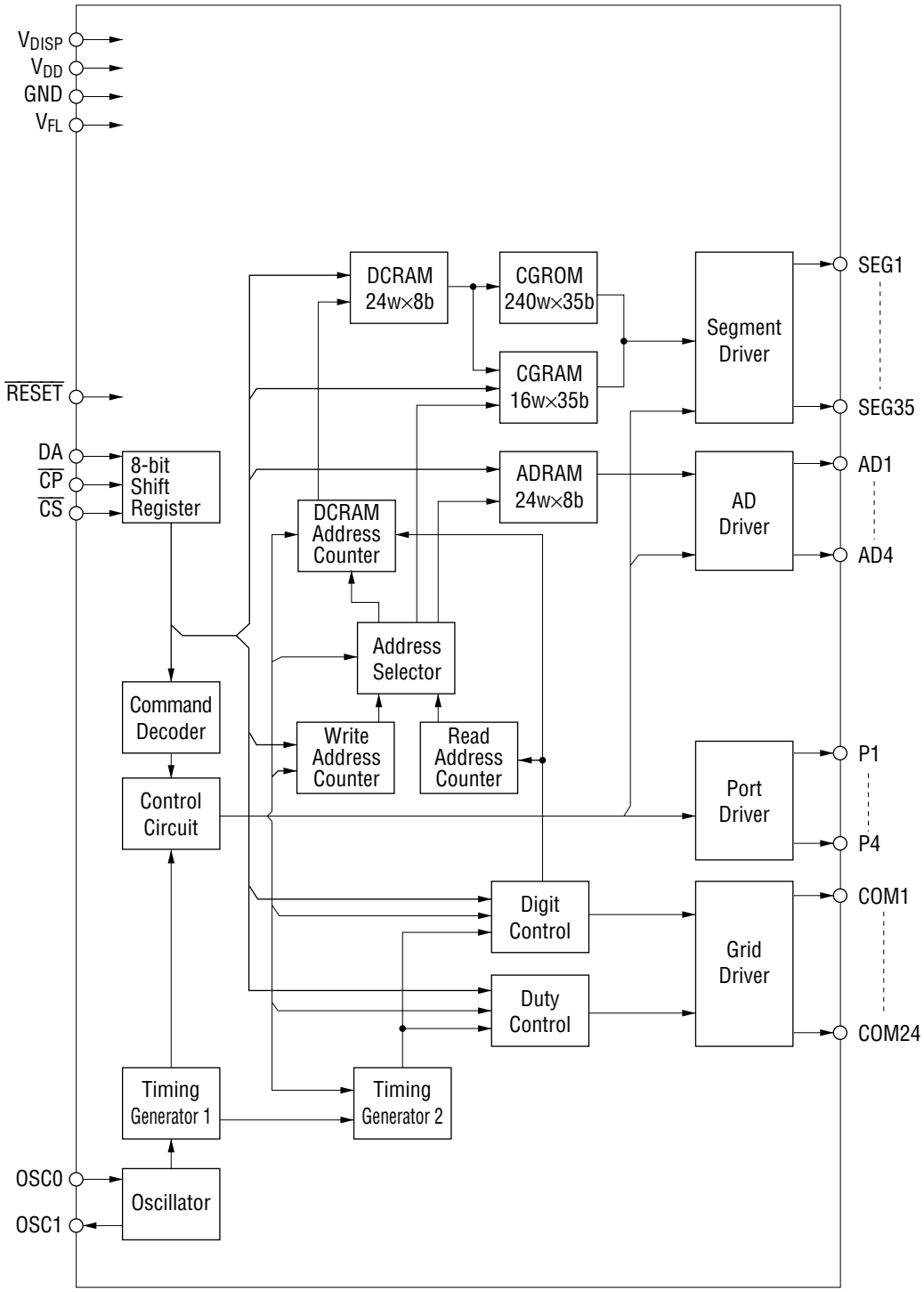
GENERAL DESCRIPTION

The MSM9201-xx is a dot matrix fluorescent display tube controller driver IC which displays characters, numerics and symbols.
Dot matrix fluorescent display tube drive signals are generated by serial data sent from a microcontroller. A display system is easily realized by internal ROM and RAM for character display.
The MSM9201-xx has low power consumption since it is made by CMOS process technology.
-01 is available as a general code.
Custom codes are provided on customer's request.

FEATURES

- Logic power supply (V_{DD}) : 3.3 V±10%/5.0 V±10%
- Fluorescent display tube drive power supply (V_{DISP}) : 3.3 V±10%/5.0 V±10%
- Fluorescent display tube drive power supply (V_{FL}) : –20 to –60 V
- VFD driver output current
  (VFD driver output can directly be connected to the fluorescent display tube. No pull-down resistor is required.)
  - Segment driver (SEG1 to SEG35) : –5.0 mA (V_{FL}=–60V)
  - Segment driver (AD1 to AD8) : –10.0 mA (V_{FL}=–60V)
  - Grid driver (COM1 to COM16) : –20.0 mA (V_{FL}=–60V)
- General output port output current
  - Output driver (P1-4) : ±1.0 mA (V_{DD}=3.3V±10%)
    ±2.0 mA (V_{DD}=5.0V±10%)
- Content of display
  - CGROM 5×7 dots, 240 types (character data)
  - CGRAM 5×7 dots, 16 types (character data)
  - ADRAM 24 (display digit) ×4 bits (symbol data)
  - DCRAM 24 (display digit) ×8 bits (register for character data display)
  - General output port 4 bits (static mode)
- Display control function
  - Display digit : 9 to 24 digits
  - Display duty (contrast adjustment) : 8 stages
  - All lights ON/OFF
- 3 interfaces with microcontroller : DA, $\overline{CS}$, $\overline{CP}$ (4 interfaces if $\overline{RESET}$ is added)
- 1-byte instruction execution (excluding data write to RAM)
- Built-in oscillation circuit (external C and R)
- Package options:
  80-pin plastic QFP (QFP80-P-1414-0.65-K) (Product name: MSM9201-xxGS-K)
  80-pin plastic QFP (QFP80-P-1420-0.80-BK) (Product name: MSM9201-xxGS-BK)
  xx indicates the code number.

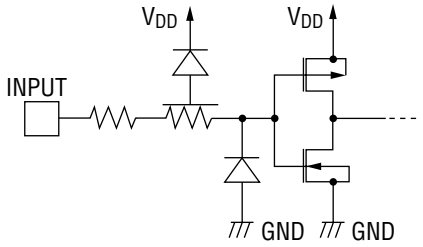
BLOCK DIAGRAM



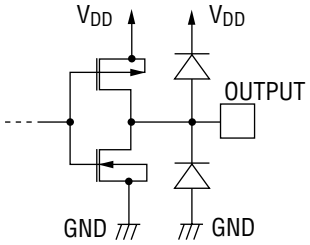
INPUT AND OUTPUT CONFIGURATION

Schematic Diagrams of Logic Portion Input and Output Circuits

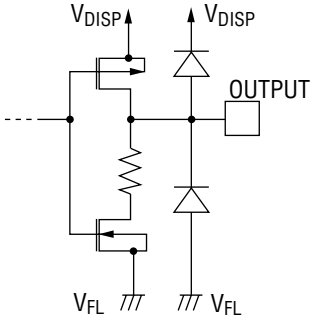
Input pin



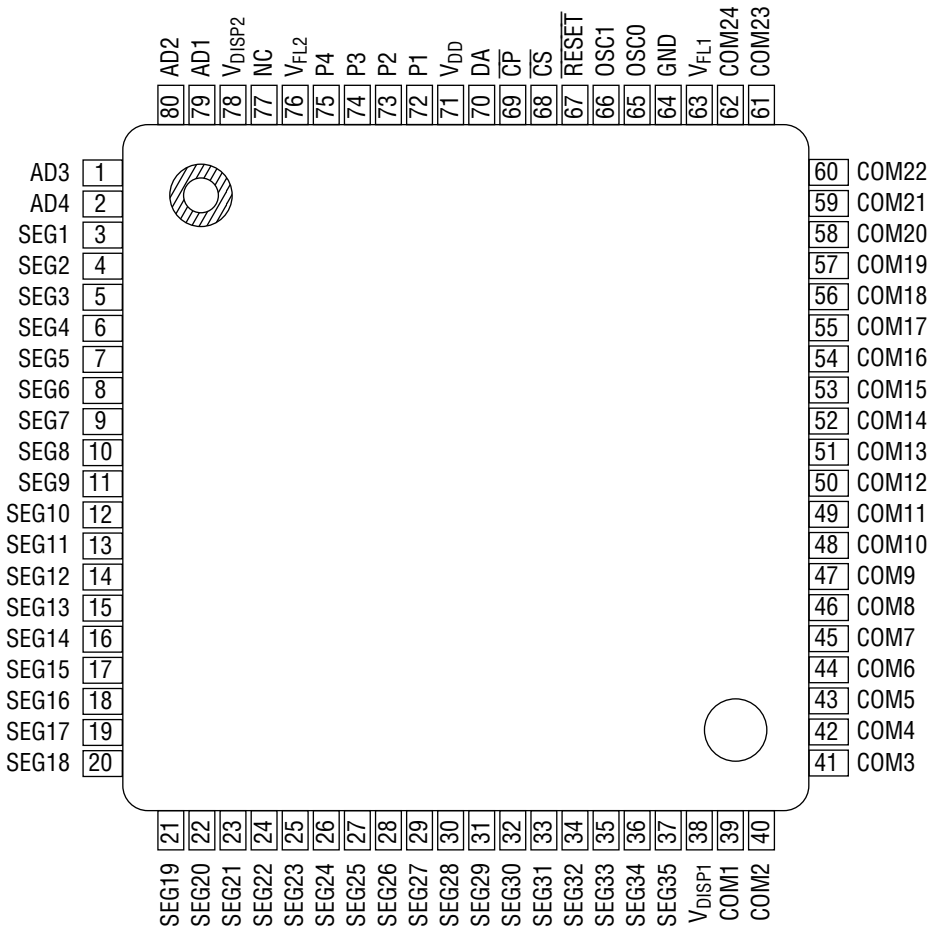
Output pin



Schematic Diagram of Driver Output Circuit

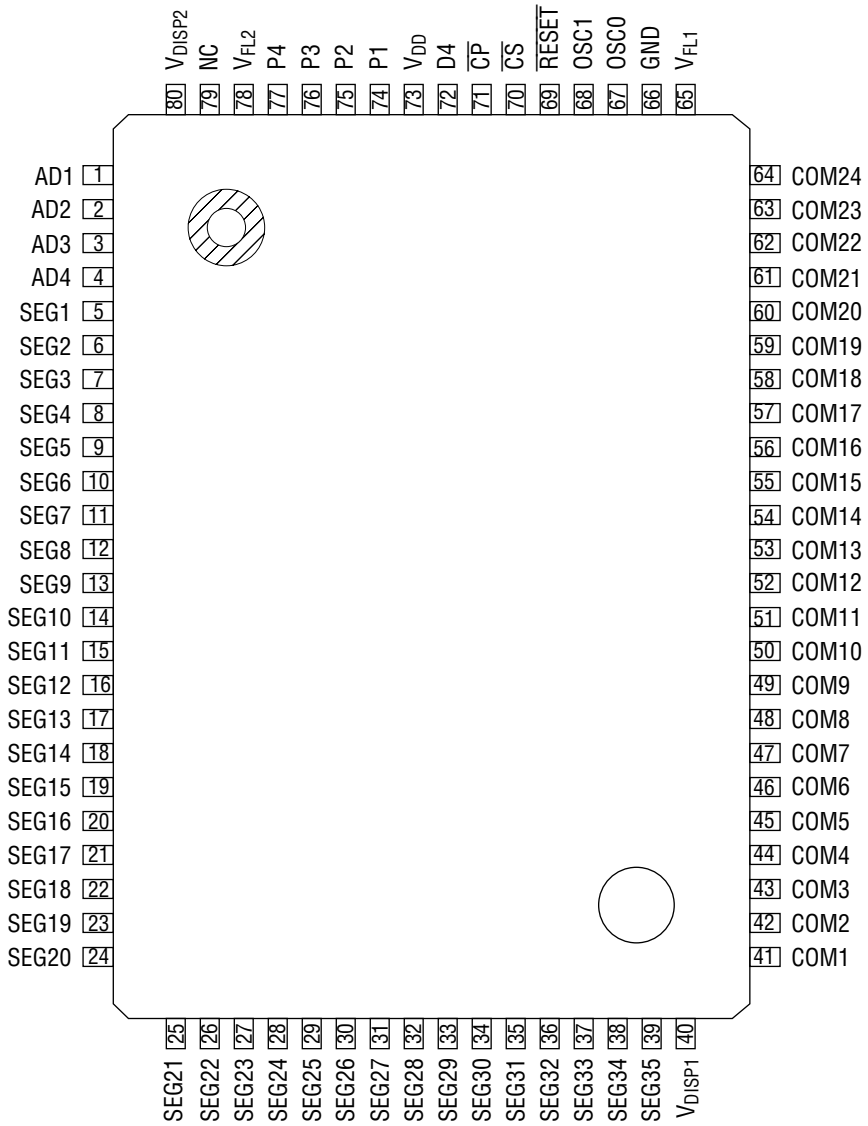


PIN CONFIGURATION (TOP VIEW)



NC: No connection

80-Pin Plastic QFP
(QFP80-P-1414-0.65-K)



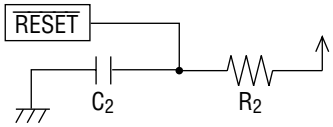
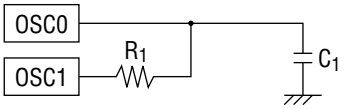
NC: No connection

80-Pin Plastic QFP
(QFP80-P-1420-0.80-BK)

PIN DESCRIPTIONS

Pin		Symbol	Type	Connects to:	Description
QFP-1*	QFP-2*				
3-27	5-39	SEG1-35	O	Fluorescent tube anode electrode	Fluorescent display tube anode electrode drive output. Directly connected to fluorescent display tube. No pull-down resistor is required. I_{OH}>–5.0 mA
39-62	41-64	COM1-24	O	Fluorescent tube grid electrode	Fluorescent display tube grid electrode drive output. Directly connected to fluorescent display tube. No pull-down resistor is required. I_{OH}>–20.0 mA
1, 2, 79, 80	1-4	AD1-4	O	Fluorescent tube anode electrode	Fluorescent display tube anode electrode drive output. Directly connected to fluorescent display tube. No pull-down resistor is required. I_{OH}>–10.0 mA
72-75	74-77	P1-4	O	LED drive control terminals	General port output. Output of these pins in static operation, so these pins can drive the LED. I_{OH}>–2.0 mA
71	73	V_{DD}	—	Power supply	V_{DD}-GND are power supplies for internal logic. V_{DISP}-V_{FL} are power supplies for driving fluorescent tubes. Use the same power supply for V_{DD} and V_{DISP}.
38, 78	40, 80	$V_{DISP1-2}$	—		
64	66	GND	—		
63, 76	65, 78	V_{FL1-2}	—		
70	72	DA	I	Micro-controller	Serial data input (positive logic). Input from LSB.
69	71	$\overline{CP}$	I	Micro-controller	Shift clock input. Serial data is shifted on the rising edge of $\overline{CP}$.
68	70	$\overline{CS}$	I	Micro-controller	Chip select input. Setting this pin to "H" disables serial data transfer.

* QFP-1 : QFP80-P-1414-0.65-K
QFP-2 : QFP80-P-1420-0.80-BK

Pin		Symbol	Type	Connects to:	Description
QFP-1*	QFP-2*				
67	69	$\overline{\text{RESET}}$	I	Micro-controller or C_2, R_2	Reset input. Setting this pin to "Low" initializes all the functions. The initial status is as follows. • Address of each RAM ····· address "00"H • Data of each RAM ····· Content is undefined • Number of display digits ····· 24 digits • Contrast adjusment ····· 8/16 • All lights ON or OFF OFF mode • All outputs ····· "Low" level  (Circuit when R and C are connected externally) See Application Circuit.
65	67	OSC0	I	C_1, R_1	External RC pin for RC oscillation. Connect R and C externally. The RC time constant depends on the V_{DD} voltage used. Set the target oscillation frequency to 2 MHz.  (RC oscillation circuit) See Application Circuit.
66	68	OSC1	O		

* QFP-1 : QFP80-P-1414-0.65-K
QFP-2 : QFP80-P-1420-0.80-BK

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Condition		Rating	Unit
Supply Voltage 1	V_{DD}	(*1)		–0.3 to +6.5	V
	V_{DISP}	(*1)		–0.3 to +6.5	V
Supply Voltage 2	V_{FL}	—		–80 to V_{DISP}+0.3	V
Input Voltage	V_{IN}	—		–80 to V_{DD}+0.3	V
Power Dissipation	P_D	Ta≤25°C	QFP80-P-1414-0.65-K	565	mW
			QFP80-P-1420-0.80-BK	643	
Storage Temperature	T_{STG}	—		–55 to +150	°C
Output Current	I_{O1}	COM1-COM24		–30 to 0.0	mA
	I_{O2}	AD1-AD4		–20 to 0.0	
	I_{O3}	SEG1-SEG35		–10 to 0.0	
	I_{O4}	P1-P4		–4.0 to +4.0	

*1 Use the same power supply for V_{DD} and V_{DISP}.

RECOMMENDED OPERATING CONDITIONS (1)

When the power supply voltage is 5V (typ)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Supply Voltage 1	V_{DD} V_{DISP}	—	4.5	5.0	5.5	V
Supply Voltage 2	V_{FL}	—	–60	—	–20	V
High Level Input Voltage	V_{IH}	All input pins excluding OSC0 pin	0.7V_{DD}	—	—	V
Low Level Input Voltage	V_{IL}	All input pins excluding OSC0 pin	—	—	0.3V_{DD}	V
$\overline{CP}$ Frequency	f_C	—	—	—	1.0	MHz
Oscillation Frequency	f_{OSC}	R=3.3kΩ, C=47pF	1.5	2.0	2.5	MHz
Frame Frequency	f_{FR}	DIGIT=1-24, R=3.3kΩ, C=47pF	122	163	204	Hz
Operating Temperature	T_{op}	—	–40	—	85	°C

RECOMMENDED OPERATING CONDITIONS (2)

When the power supply voltage is 3.3V (typ)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Supply Voltage 1	V_{DD} V_{DISP}	—	3.0	3.3	3.6	V
Supply Voltage 2	V_{FL}	—	–60	—	–20	V
High Level Input Voltage	V_{IH}	All input pins excluding OSC0 pin	0.8V_{DD}	—	—	V
Low Level Input Voltage	V_{IL}	All input pins excluding OSC0 pin	—	—	0.2V_{DD}	V
$\overline{CP}$ Frequency	f_C	—	—	—	1.0	MHz
Oscillation Frequency	f_{OSC}	R=3.3kΩ, C=39pF	1.5	2.0	2.5	MHz
Frame Frequency	f_{FR}	DIGIT=1–24, R=3.3kΩ, C=39pF	122	163	204	Hz
Operating Temperature	T_{op}	—	–40	—	85	°C

ELECTRICAL CHARACTERISTICS

DC Characteristics (1)

(V_{DD}=V_{DISP}=5.0V±10%, V_{FL}=–60V, Ta=–40 to +85°C, unless otherwise specified)

Parameter	Symbol	Applied pin	Condition		Min.	Max.	Unit
High Level Input Voltage	V_{IH}	$\overline{CS}$, $\overline{CP}$, DA, $\overline{RESET}$	—		0.7V_{DD}	—	V
Low Level Input Voltage	V_{IL}	$\overline{CS}$, $\overline{CP}$, DA, $\overline{RESET}$	—		—	0.3V_{DD}	V
High Level Input Current	I_{IH}	$\overline{CS}$, $\overline{CP}$, DA, $\overline{RESET}$	V_{IH}=V_{DD}		–1.0	1.0	µA
Low Level Input Current	I_{IL}	$\overline{CS}$, $\overline{CP}$, DA, $\overline{RESET}$	V_{IL}=0.0V		–1.0	1.0	µA
High Level Output Voltage	V_{OH1}	COM1-24	I_{OH1}=–20.0mA		V_{DISP}–1.5	—	V
	V_{OH2}	AD1-4	I_{OH2}=–10.0mA		V_{DISP}–1.5	—	V
	V_{OH3}	SEG1-35	I_{OH3}=–5.0mA		V_{DISP}–1.5	—	V
	V_{OH4}	P1-4	I_{OH4}=–2.0mA		V_{DD}–1.0	—	V
Low Level Output Voltage	V_{OL1}	COM1-24 AD1-4 SEG1-35	—		—	V_{FL}+1.0	V
	V_{OL2}	P1-4	I_{OL1}=2mA		—	1.0	V
Supply Current	I_{DD1}	V_{DD}, V_{DISP}	f_{OSC}= 2MHz, no load	Duty=15/16 Digit=1–24 All outputs go ON	—	4	mA
	I_{DD2}			Duty=8/16 Digit=1–9 All outputs go OFF	—	3	mA

DC Characteristics (2)

(V_{DD}=V_{DISP}=3.3V±10%, V_{FL}=–60V, Ta=–40 to +85°C, unless otherwise specified)

Parameter	Symbol	Applied pin	Condition		Min.	Max.	Unit
High Level Input Voltage	V_{IH}	$\overline{CS}$, $\overline{CP}$, DA, $\overline{RESET}$	—		0.8V_{DD}	—	V
Low Level Input Voltage	V_{IL}	$\overline{CS}$, $\overline{CP}$, DA, $\overline{RESET}$	—		—	0.2V_{DD}	V
High Level Input Current	I_{IH}	$\overline{CS}$, $\overline{CP}$, DA, $\overline{RESET}$	V_{IH}=V_{DD}		–1.0	1.0	µA
Low Level Input Current	I_{IL}	$\overline{CS}$, $\overline{CP}$, DA, $\overline{RESET}$	V_{IL}=0.0V		–1.0	1.0	µA
High Level Output Voltage	V_{OH1}	COM1-24	I_{OH1}=–20.0mA		V_{DISP}–1.5	—	V
	V_{OH2}	AD1-4	I_{OH2}=–10.0mA		V_{DISP}–1.5	—	V
	V_{OH3}	SEG1-35	I_{OH3}=–5.0mA		V_{DISP}–1.5	—	V
	V_{OH4}	P1-4	I_{OH4}=–1.0mA		V_{DD}–1.0	—	V
Low Level Output Voltage	V_{OL1}	COM1-24 AD1-4 SEG1-35	—		—	V_{FL}+1.0	V
	V_{OL2}	P1-4	I_{OL1}=2mA		—	1.0	V
Supply Current	I_{DD1}	V_{DD}, V_{DISP}	f_{OSC}= 2MHz, no load	Duty=15/16 Digit=1–24 All outputs go ON	—	3	mA
	I_{DD2}			Duty=8/16 Digit=1–9 All outputs go OFF	—	2	mA

AC Characteristics (1)

(V_{DD}, V_{DISP}=5.0V±10%, V_{FL}=–60V, Ta=–40 to +85°C, unless otherwise specified)

Parameter	Symbol	Condition		Min.	Max.	Unit
$\overline{CP}$ Frequncy	f_C	—		—	1.0	MHz
$\overline{CP}$ Pulse Width	t_{CW}	—		300	—	ns
DA Setup Time	t_{DS}	—		300	—	ns
DA Hold Time	t_{DH}	—		300	—	ns
$\overline{CS}$ Setup Time	t_{CSS}	—		300	—	ns
$\overline{CS}$ Hold Time	t_{CSH}	R_1=3.3kΩ, C_1=47pF		16	—	µs
$\overline{CS}$ Wait Time	t_{CSW}	—		300	—	ns
Data Processing Time	t_{DOFF}	R_1=3.3kΩ, C_1=47pF		8	—	µs
$\overline{RESET}$ Pulse Width	t_{WRES}	When $\overline{RESET}$ signal is input externally		300	—	ns
DA Wait Time	t_{RSOFF}	—		300	—	µs
Slew Rate (All Drivers)	t_R	C_l=100pF	t_R=20% to 80%	—	4.0	µs
	t_F		t_F=80% to 20%	—	4.0	µs
V_{DD} Rise Time	t_{PRZ}	When mounted on the unit		—	100	µs
V_{DD} Off Time	t_{POF}	When mounted on the unit, V_{DD}=0.0V		5.0	—	ms

AC Characteristics (2)

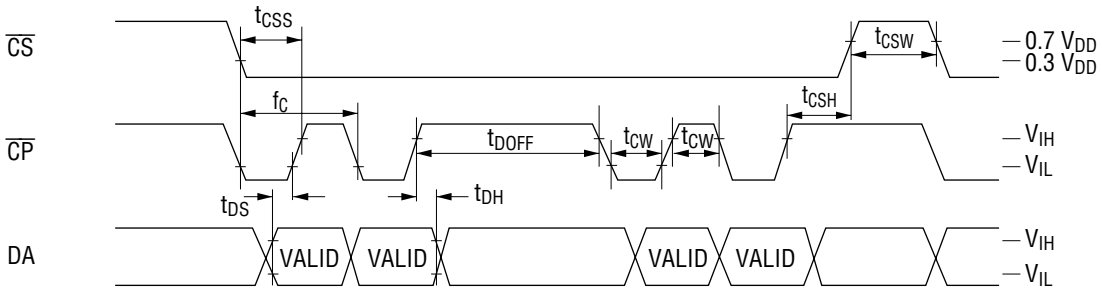
(V_{DD}, V_{DISP}=3.3V±10%, V_{FL}=–60V, Ta=–40 to +85°C, unless otherwise specified)

Parameter	Symbol	Condition		Min.	Max.	Unit
$\overline{CP}$ Frequncy	f_C	—		—	1.0	MHz
$\overline{CP}$ Pulse Width	t_{CW}	—		300	—	ns
DA Setup Time	t_{DS}	—		300	—	ns
DA Hold Time	t_{DH}	—		300	—	ns
$\overline{CS}$ Setup Time	t_{CSS}	—		300	—	ns
$\overline{CS}$ Hold Time	t_{CSH}	R_1=3.3kΩ, C_1=39pF		16	—	µs
$\overline{CS}$ Wait Time	t_{CSW}	—		300	—	ns
Data Processing Time	t_{DOFF}	R_1=3.3kΩ, C_1=39pF		8	—	µs
$\overline{RESET}$ Pulse Width	t_{WRES}	When $\overline{RESET}$ signal is input externally		300	—	ns
DA Wait Time	t_{RSOFF}	—		300	—	µs
Slew Rate (All Drivers)	t_R	C_l=100pF	t_R=20% to 80%	—	4.0	µs
	t_F		t_F=80% to 20%	—	4.0	µs
V_{DD} Rise Time	t_{PRZ}	When mounted on the unit		—	100	µs
V_{DD} Off Time	t_{POF}	When mounted on the unit, V_{DD}=0.0V		5.0	—	ms

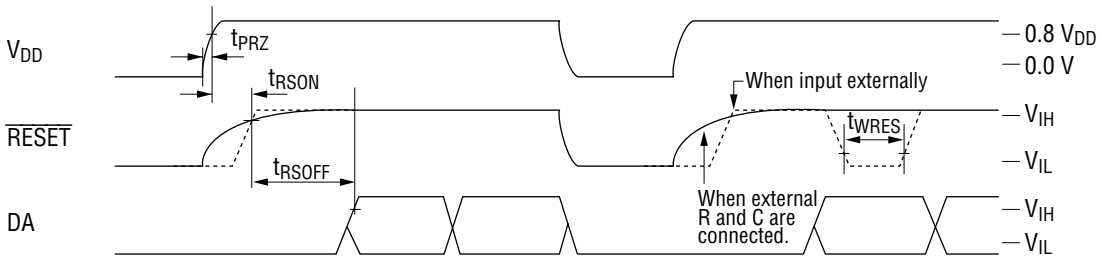
TIMING DIAGRAM

Symbol	V_{DD}=3.3V±10%	V_{DD}=5.0V±10%
V_{IH}	0.8 V_{DD}	0.7 V_{DD}
V_{IL}	0.2 V_{DD}	0.3 V_{DD}

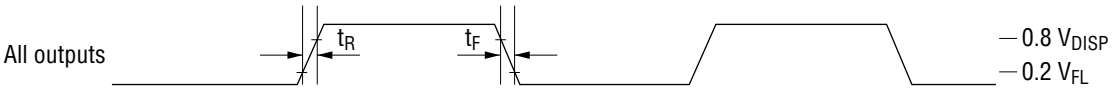
• Data Timing



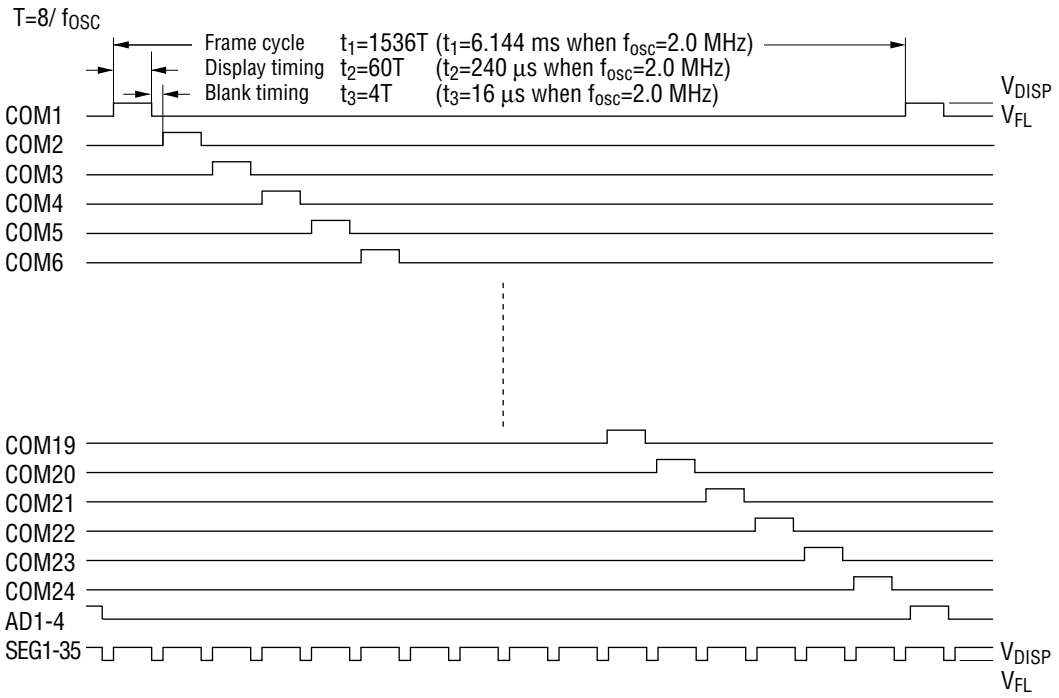
• Reset Timing



• Output Timing



Digit Output Timing (for 24-digit display, at a duty of 15/16)



FUNCTIONAL DESCRIPTION

Command List

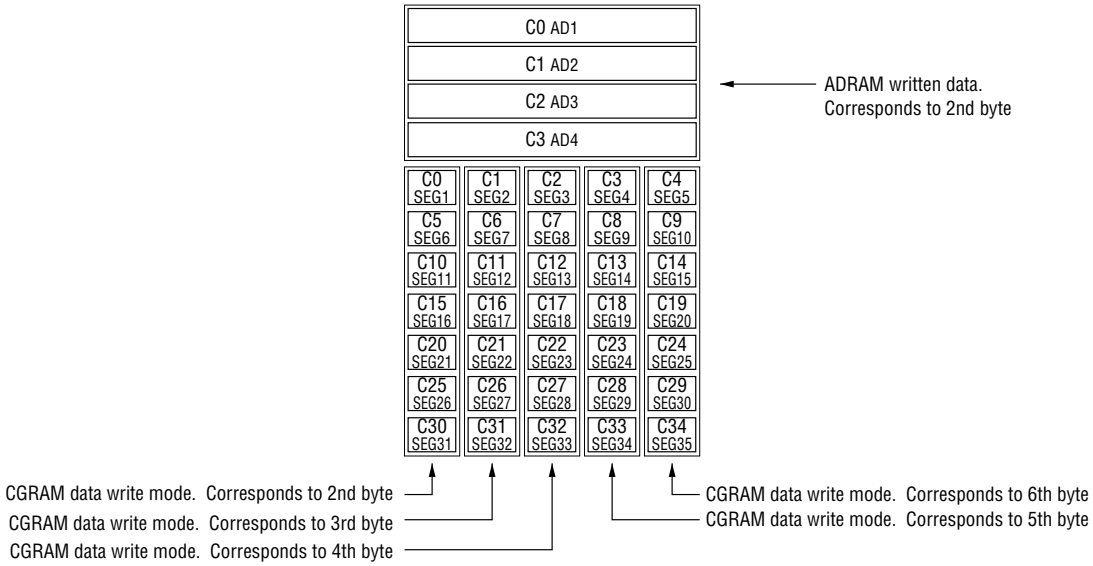
	Command	1st byte LSB							MSB	2nd byte LSB							MSB	
		B0	B1	B2	B3	B4	B5	B6	B7	B0	B1	B2	B3	B4	B5	B6	B7	
1	DCRAM data write	X0	X1	X2	X3	X4	1	0	0	C0	C1	C2	C3	C4	C5	C6	C7	
2	CGRAM data write 1	X0	X1	X2	X3	*	0	1	0	C0	C5	C10	C15	C20	C25	C30	*	2nd byte
										C1	C6	C11	C16	C21	C26	C31	*	3rd byte
										C2	C7	C12	C17	C22	C27	C32	*	4th byte
										C3	C8	C13	C18	C23	C28	C33	*	5th byte
										C4	C9	C14	C19	C24	C29	C34	*	6th byte
3	ADRAM data write	X0	X1	X2	X3	X4	1	1	0	C0	C1	C2	C3	*	*	*	*	
4	General output port set	P1	P2	P3	P4	*	0	0	1									
5	Display duty set	D0	D1	D2	*	*	1	0	1									
6	Number of display digits set	K0	K1	K2	K3	*	0	1	1									
7	All lights ON/OFF	L	H	*	*	*	1	1	1									
	Test mode																	

* : Don't care
Xn : Address specification for each RAM
Cn : Character code specification for each RAM
Pn : General output port status specification
Dn : Display duty specification
Kn : Number of display digits specification
H : All lights ON instruction
L : All lights OFF instruction

When data is written to RAM (DCRAM, CGRAM, ADRAM) continuously, addresses are internally incremented automatically.
Therefore it is not necessary to specify the 1st byte when RAM data for the 2nd and later bytes is written.

Note: The test mode is used for inspection before shipment.
It is not a user function.

Positional Relationship Between SEGn and ADn (one digit)

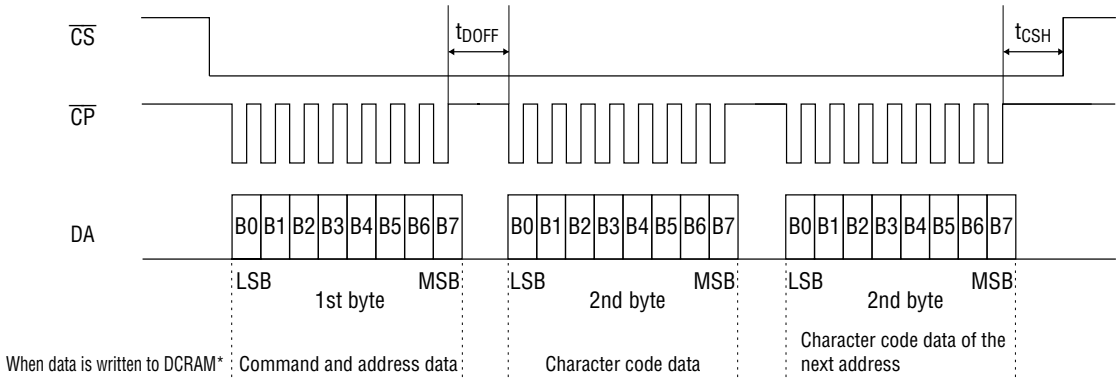


Data Transfer Method and Command Write Method

Display control command and data are written by an 8-bit serial transfer.
Write timing is shown in the figure below.

Setting the $\overline{CS}$ pin to "Low" level enables a data transfer.
Data is 8 bits and is sequentially input into the DA pin from LSB (LSB first).
As shown in the figure below, data is read by the shift register at the rise of the shift clock, which is input into the $\overline{CP}$ pin. If 8-bit data is input, internal load signals are automatically generated and data is written to each register and RAM.
Therefore it is not necessary to input load signals from the outside.

Setting the $\overline{CS}$ pin to "High" disables data transfer. Data input from the point when the $\overline{CS}$ pin changes from "High" to "Low" is recognized in 8-bit units.



* When data is written to RAM (DCRAM, ADRAM, CGRAM) continuously, addresses are internally incremented automatically.
Therefore it is not necessary to specify the 1st byte to write RAM data for the 2nd and later bytes.

Reset Function

Reset is executed when the $\overline{RESET}$ pin is set to "L", (when turning power on, for example,) which initializes all functions.
The initial status is as follows.

- Address of each RAM ..... address "00"H
- Data of each RAM ..... All contents are undefined
- General output port ..... All general output ports go "Low"
- Number of display digits ..... 24 digits
- Contrast adjustment 8/16
- All display lights ON or OFF ..... OFF mode
- Segment output ..... All segment outputs go "Low"
- AD output ..... All AD outputs go "Low"

After reset is executed, perform settings again according to "Initial Setting Flowchart" shown later.

Description of Commands and Functions

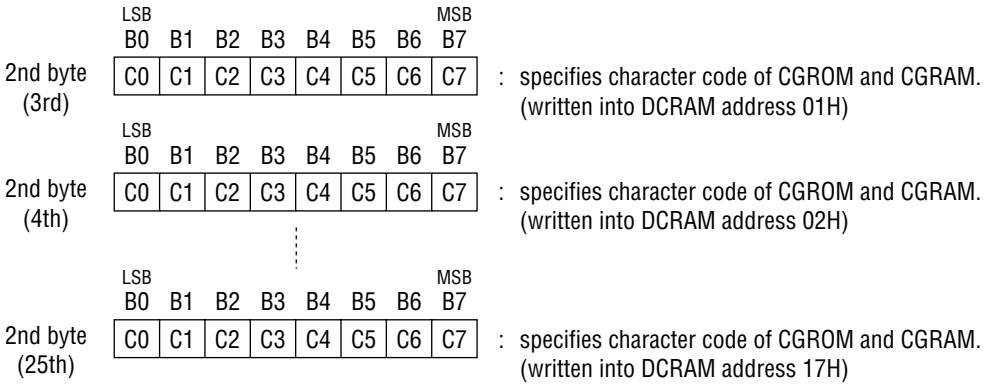
1. DCRAM data write
   (Specifies the address (00H to 1FH) of DCRAM and writes the character code of CGROM and CGRAM.)

DCRAM (Data Control RAM) has 5-bit addresses to store character code of CGROM and CGRAM.
The character code specified in DCRAM is converted to a 5×7 dot matrix character pattern via CGROM or CGRAM.
The DCRAM can store 24 characters.

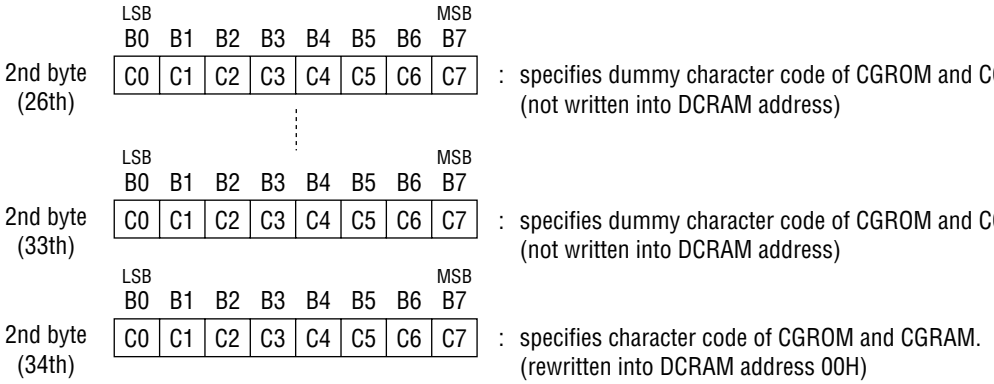
[Command format]

	LSB B0	B1	B2	B3	B4	B5	B6	MSB B7	
1st byte (1st)	X0	X1	X2	X3	X4	1	0	0	: selects DCRAM data write mode and specifies DCRAM address. (Ex: Specifies DCRAM address 00H)
	LSB B0	B1	B2	B3	B4	B5	B6	MSB B7	
2nd byte (2nd)	C0	C1	C2	C3	C4	C5	C6	C7	: specifies character code of CGROM and CGRAM. (written into DCRAM address 00H)

To specify the character code of CGROM and CGRAM continuously to the next address, specify only character codes as follows.
Since the addresses of DCRAM are automatically incremented, they do not need to be specified.



Setting of CGROM and CGRAM character codes for up to 24 digits is now complete.
To further specify character codes continuously from DCRAM address 00H, dummy character codes must be specified for DCRAM address 18H to 1FH (so that DCRAM address will be incremented automatically and will be reset to 00H).



X0 (LSB) to X4 (MSB): DCRAM address (5 bits: 24 characters)
C0 (LSB) to C7 (MSB): Character code of CGROM and CGRAM (8 bits: 256 characters)

[COM positions and set DCRAM address]

HEX	X0	X1	X2	X3	X4	COM position	HEX	X0	X1	X2	X3	X4	COM position
00	0	0	0	0	0	COM1	10	0	0	0	0	1	COM17
01	1	0	0	0	0	COM2	11	1	0	0	0	1	COM18
02	0	1	0	0	0	COM3	12	0	1	0	0	1	COM19
03	1	1	0	0	0	COM4	13	1	1	0	0	1	COM20
04	0	0	1	0	0	COM5	14	0	0	1	0	1	COM21
05	1	0	1	0	0	COM6	15	1	0	1	0	1	COM22
06	0	1	1	0	0	COM7	16	0	1	1	0	1	COM23
07	1	1	1	0	0	COM8	17	1	1	1	0	1	COM24
08	0	0	0	1	0	COM9	18	0	0	0	1	1	—
09	1	0	0	1	0	COM10	19	1	0	0	1	1	—
0A	0	1	0	1	0	COM11	1A	0	1	0	1	1	—
0B	1	1	0	1	0	COM12	1B	1	1	0	1	1	—
0C	0	0	1	1	0	COM13	1C	0	0	1	1	1	—
0D	1	0	1	1	0	COM14	1D	1	0	1	1	1	—
0E	0	1	1	1	0	COM15	1E	0	1	1	1	1	—
0F	1	1	1	1	0	COM16	1F	1	1	1	1	1	—

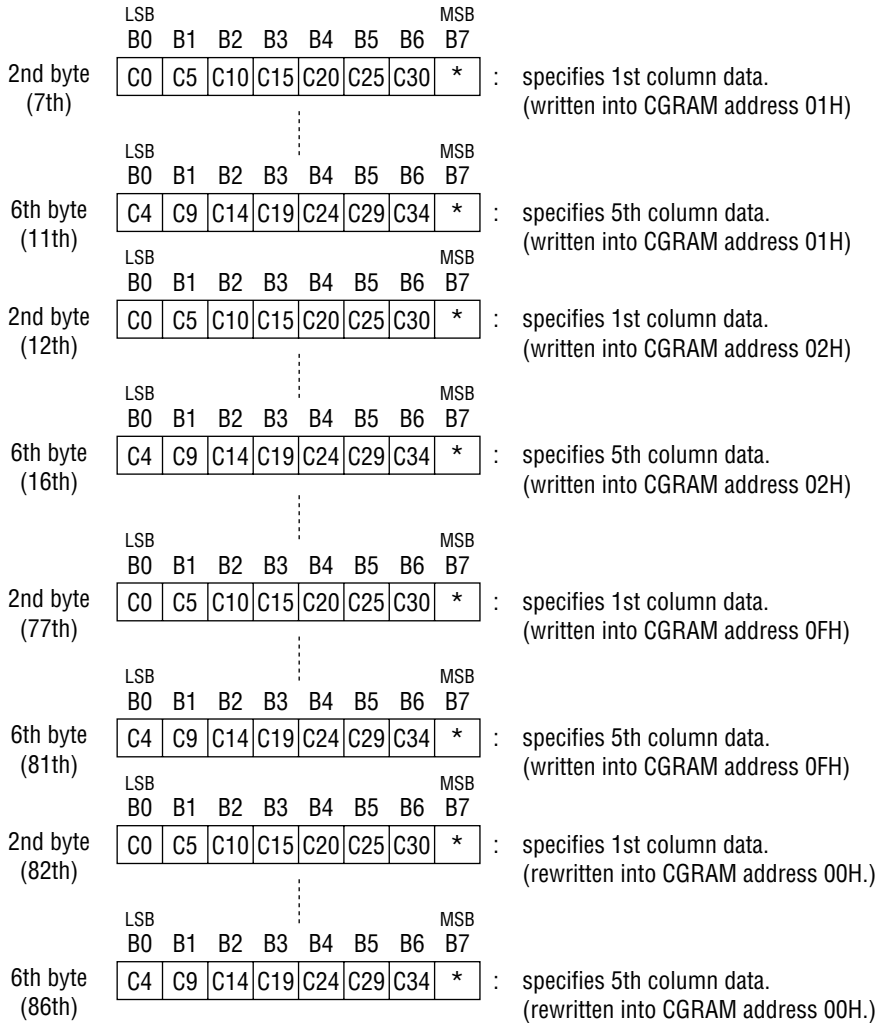
2. CGRAM data write
(Specifies the addresses 00H to 0FH of CGRAM and writes character pattern data.)

CGRAM (Character Generator RAM) has 4-bit addresses to store 5×7 dot matrix character patterns.
A character pattern stored in CGRAM can be displayed by specifying the character code (address) in DCRAM.
The addresses of CGRAM are assigned to 00H to 0FH. (All the other addresses are the CGROM addresses.)
(The CGRAM can store 16 types of character patterns.)

[Command format]

	LSB B0	B1	B2	B3	B4	B5	B6	MSB B7		
1st byte (1st)	X0	X1	X2	X3	*	0	1	0	:	selects CGRAM data write mode and specifies CGRAM address. (Ex: specifies CGRAM address 00H)
2nd byte (2nd)	C0	C5	C10	C15	C20	C25	C30	*	:	specifies 1st column data. (written into CGRAM address 00H)
3rd byte (3rd)	C1	C6	C11	C16	C21	C26	C31	*	:	specifies 2nd column data. (written into CGRAM address 00H)
4th byte (4th)	C2	C7	C12	C17	C22	C27	C32	*	:	specifies 3rd column data. (written into CGRAM address 00H)
5th byte (5th)	C3	C8	C13	C18	C23	C28	C33	*	:	specifies 4th column data. (written into CGRAM address 00H)
6th byte (6th)	C4	C9	C14	C19	C24	C29	C34	*	:	specifies 5th column data. (written into CGRAM address 00H)

To specify character pattern data continuously to the next address, specify only character pattern data as follows.
Since the addresses of CGRAM are automatically incremented, they do not need to be specified.
The 2nd to 6th byte (character pattern data) are regarded as one data item, so 300 ns is sufficient for t_{DOFF} time between bytes.



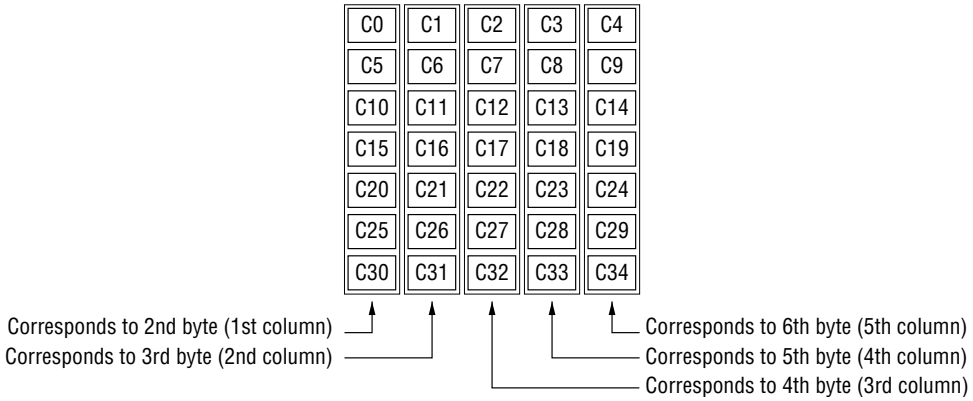
X0 (LSB) to X3 (MSB): CGRAM address (4 bits: 16 characters)
C0 (LSB) to C34 (MSB): Character pattern data (35 bits: 35 outputs per digit)

[CGROM addresses and set CGRAM addresses]

Refer to ROM CODE

HEX	X0	X1	X2	X3	CGROM address	HEX	X0	X1	X2	X3	CGROM address
00	0	0	0	0	RAM00(00000000B)	08	0	0	0	0	RAM08(00001000B)
01	1	0	0	0	RAM01(00000001B)	09	1	0	0	0	RAM09(00001001B)
02	0	1	0	0	RAM02(00000010B)	0A	0	1	0	0	RAM0A(00001010B)
03	1	1	0	0	RAM03(00000011B)	0B	1	1	0	0	RAM0B(00001011B)
04	0	0	1	0	RAM04(00000100B)	0C	0	0	1	0	RAM0C(00001100B)
05	1	0	1	0	RAM05(00000101B)	0D	1	0	1	0	RAM0D(00001101B)
06	0	1	1	0	RAM06(00000110B)	0E	0	1	1	0	RAM0E(00001110B)
07	1	1	1	0	RAM07(00000111B)	0F	1	1	1	0	RAM0F(00001111B)

Positional relationship between the output area of CGROM and that of CGRAM

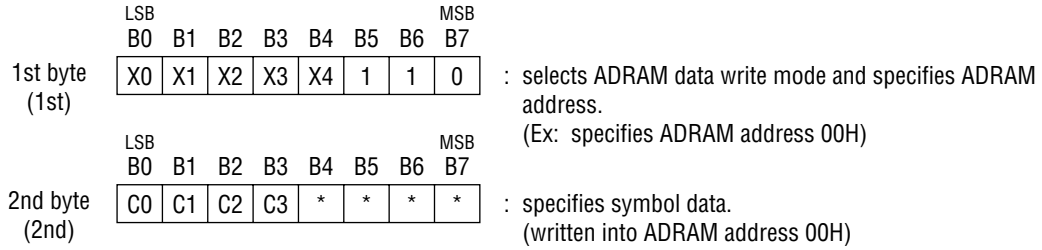


Note: CGROM (Character Generator ROM) has 8-bit addresses to generate 5×7 dot matrix character patterns.
CGRAM can store 240 types opf character patterns.
General-purpose code-01 is available and custom codes are provided on customer's request.

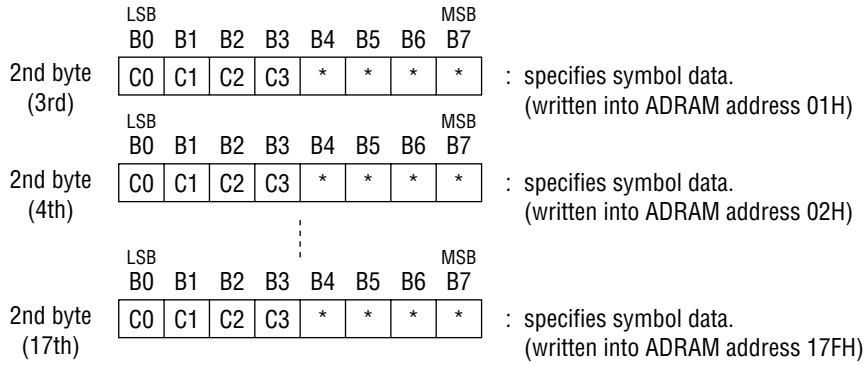
3. ADRAM data write
(specifies address of ADRAM and writes symbol data)

ADRAM (Additional Data RAM) has 4-bit addresses to store symbol data.
Symbol data specified in ADRAM is directly output without CGROM and CGRAM.
(The DRAM can store 4 types of symbol patterns for each digit.)
The terminal to which the contents of ADRAM are output can be used as a cursor.

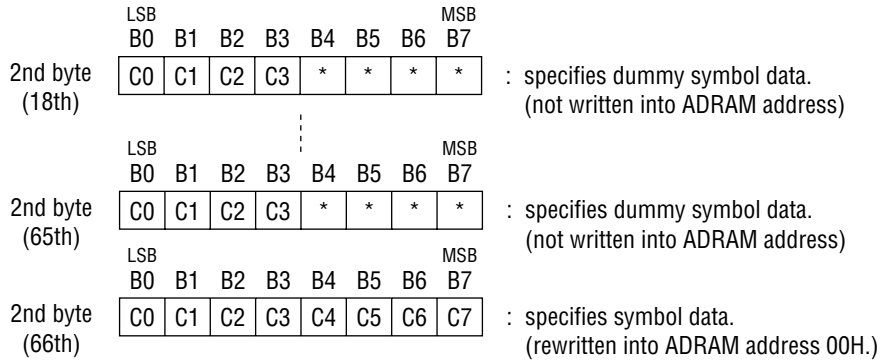
[Command format]



To specify symbol data continuously to the next address, specify only symbol data as follows. The addresses of ADRAM are automatically incremented. Specification of ADRAM addresses is therefore unnecessary.



Setting of symbol data for up to 24 digits is now complete.
To further specify symbol data continuously from DCRAM address 00H, dummy symbol data must be specified for ADRAM addresses 18H to 1FH (so that the ADRAM address will be incremented automatically and will be reset to 00H).



X0 (LSB) to X4 (MSB): ADRAM addresses (5 bits: 24 characters)
C0 (LSB) to C3 (MSB): Symbol data (4 bits: 4-symbol data per digit)

[COM positions and ADRAM addresses]

HEX	X0	X1	X2	X3	X4	COM position	HEX	X0	X1	X2	X3	X4	COM position
00	0	0	0	0	0	COM1	10	0	0	0	0	1	COM17
01	1	0	0	0	0	COM2	11	1	0	0	0	1	COM18
02	0	1	0	0	0	COM3	12	0	1	0	0	1	COM19
03	1	1	0	0	0	COM4	13	1	1	0	0	1	COM20
04	0	0	1	0	0	COM5	14	0	0	1	0	1	COM21
05	1	0	1	0	0	COM6	15	1	0	1	0	1	COM22
06	0	1	1	0	0	COM7	16	0	1	1	0	1	COM23
07	1	1	1	0	0	COM8	17	1	1	1	0	1	COM24
08	0	0	0	1	0	COM9	18	0	0	0	1	1	—
09	1	0	0	1	0	COM10	19	1	0	0	1	1	—
0A	0	1	0	1	0	COM11	1A	0	1	0	1	1	—
0B	1	1	0	1	0	COM12	1B	1	1	0	1	1	—
0C	0	0	1	1	0	COM13	1C	0	0	1	1	1	—
0D	1	0	1	1	0	COM14	1D	1	0	1	1	1	—
0E	0	1	1	1	0	COM15	1E	0	1	1	1	1	—
0F	1	1	1	1	0	COM16	1F	1	1	1	1	1	—

4. General output port set
(specifies the general output port status)

The general output port is an output for 4-bit static operation.
It is used to control other I/O devices and turn on LED. (Static operation.)
The fluorescent display tube cannot be driven by this output port, because when at the "High" level this output becomes the V_{DD} voltage and when at the "Low" level it becomes the ground potential.

[Command format]

	LSB B0	B1	B2	B3	B4	B5	B6	MSB B7	
1st byte	P1	P2	P3	P4	*	0	0	1	: selects general output port and specifies the output status.

P1-P4 : general output ports
* : don't care

[Set data and set state of general output port]

Pn	Display state of general output port
0	Sets P1-P4 to Low
1	Sets P1-P4 to High

(The state when power is applied or when $\overline{\text{RESET}}$ is input)

5. Display duty set
(writes display duty value to duty cycle register)

Display duty adjusts contrast in 8 stages using 3-bit data.
At the time power is turned on or the $\overline{\text{RESET}}$ signal is input, the duty cycle register value is "0". Always execute this instruction before turning the display on, then set a desired duty value.

[Command format]

	LSB B0	B1	B2	B3	B4	B5	B6	MSB B7	
1st byte	D0	D1	D2	*	*	1	0	1	: selects display duty set mode and sets duty value.

D0 (LSB) to D2 (MSB) : display duty data (3 bits: 8 stages)
* : don't care

[Relation between setup data and controlled COM duty]

HEX	D2	D1	D0	COM duty
0	0	0	0	8/16
1	0	0	1	9/16
2	0	1	0	10/16
3	0	1	1	11/16
4	1	0	0	12/16
5	1	0	1	13/16
6	1	1	0	14/16
7	1	1	1	15/16

(The state at the time power is turned on or $\overline{\text{RESET}}$ signal is input)

6. Number of display digits set
(writes the number of display digits to the display digit register)

The number of display digits set can display 9 to 24 digits using 4-bit data.
At the time power is turned on or a $\overline{\text{RESET}}$ signal is input, the display digit register value is "0". Always execute this instruction to change the number of digits before turning the dispaly on.

[Command format]

	LSB B0	B1	B2	B3	B4	B5	B6	MSB B7	
1st byte	K0	K1	K2	K3	*	0	1	1	: selects the number of display digits set mode and specifies the number of digits value.

K0 (LSB) to K3 (MSB): number of display digits data (4 bits: 16 digits)

[Relation between setup data and controlled COM]

HEX	K0	K1	K2	K3	Number of digits of COM	HEX	K0	K1	K2	K3	Number of digits of COM
0	0	0	0	0	COM1-24	8	0	0	0	1	COM1-16
1	1	0	0	0	COM1-9	9	1	0	0	1	COM1-17
2	0	1	0	0	COM1-10	A	0	1	0	1	COM1-18
3	1	1	0	0	COM1-11	B	1	1	0	1	COM1-19
4	0	0	1	0	COM1-12	C	0	0	1	1	COM1-20
5	1	0	1	0	COM1-13	D	1	0	1	1	COM1-21
6	0	1	1	0	COM1-14	E	0	1	1	1	COM1-22
7	1	1	1	0	COM1-15	F	1	1	1	1	COM1-23

→ The state at the time power is turned on or $\overline{\text{RESET}}$ signal is input

7. All display lights ON/OFF set
(Turns all display lights ON or OFF)

The all display lights ON mode is used primarily for display testing.
The all display lights OFF mode is primarily used to prevent malfunction on power-up.

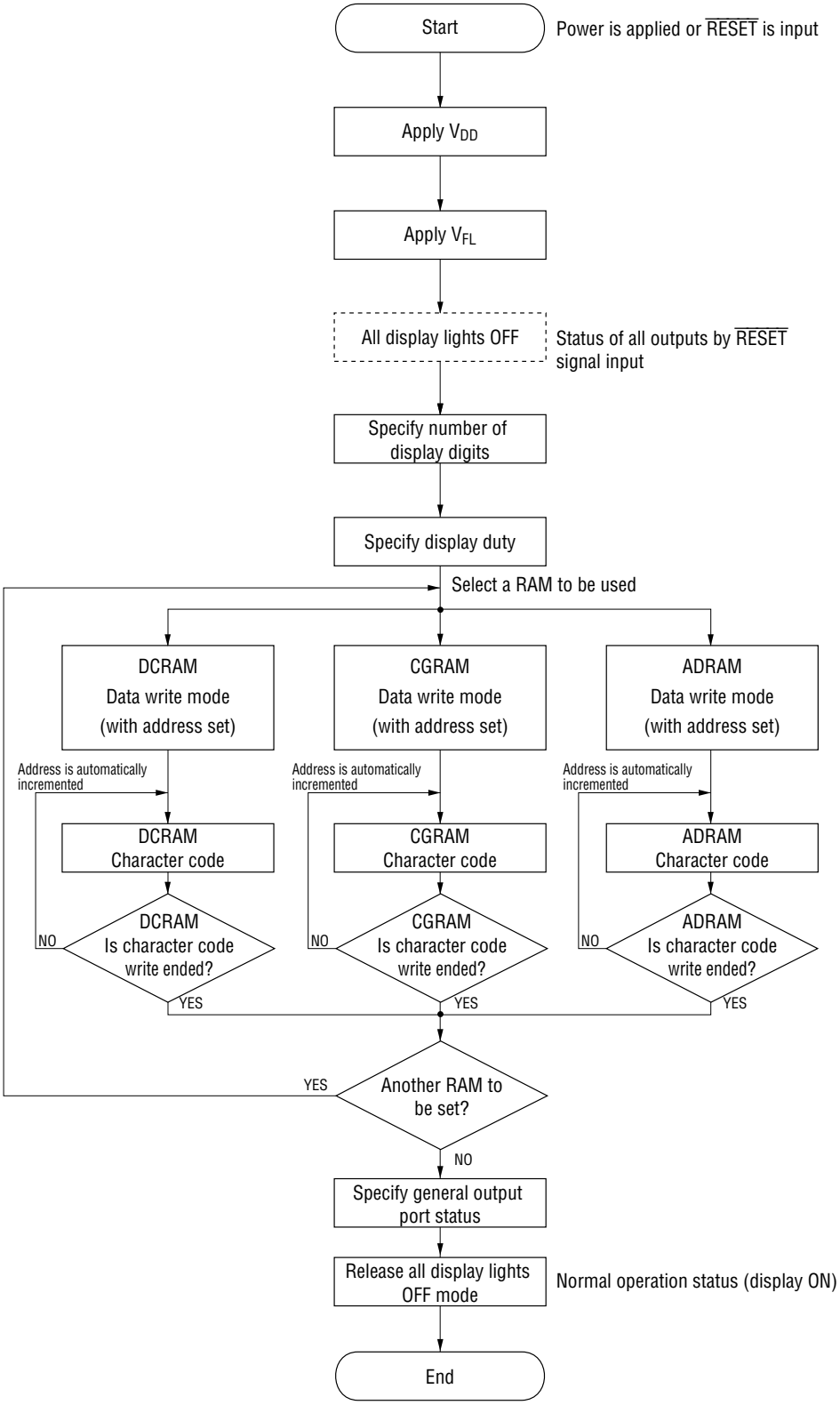
[Command format]

	LSB B0	B1	B2	B3	B4	B5	B6	MSB B7	
1st byte	L	H	*	*	*	1	1	1	: selects all display lights ON or OFF mode.

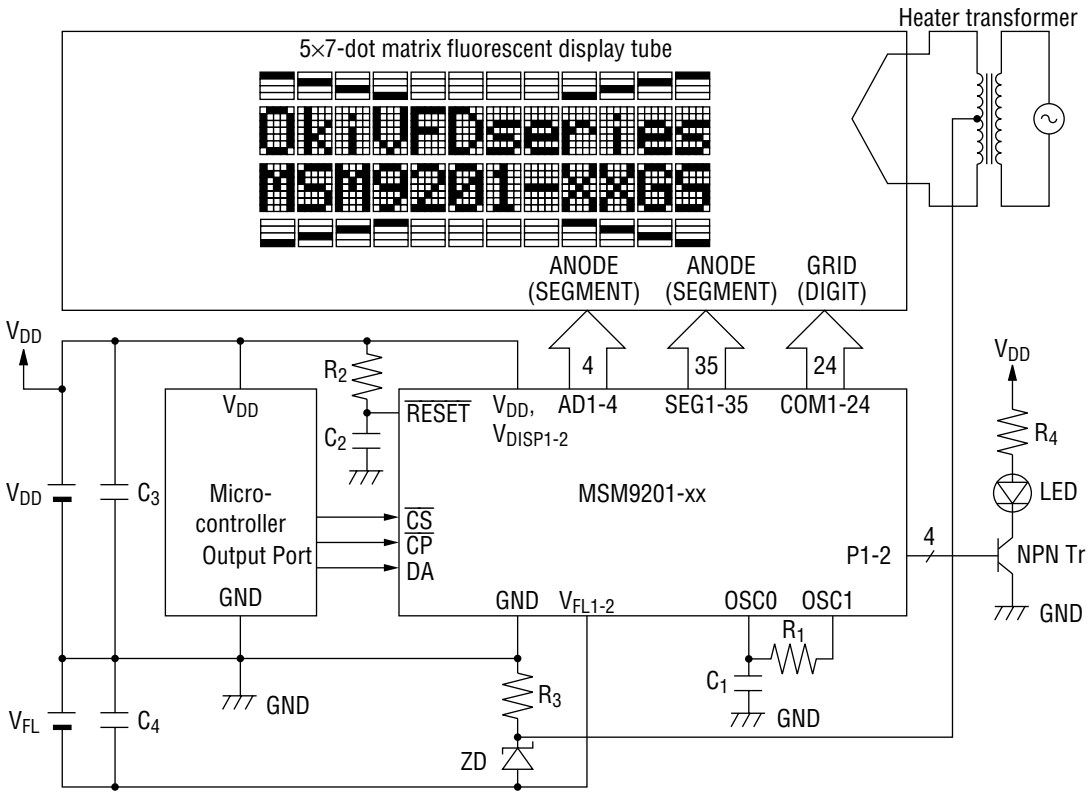
[Set data and display state of SEG and AD]

L	H	Display state of SEG and AD	
0	0	All outputs maintain current states	
1	0	Sets all outputs to Low	(The state at the time power is applied or $\overline{\text{RESET}}$ is input)
0	1	Sets all outputs to High	
1	1	Sets all outputs to High	(All lights ON mode has priority.)

Initial Setting Flowchart



APPLICATION CIRCUIT



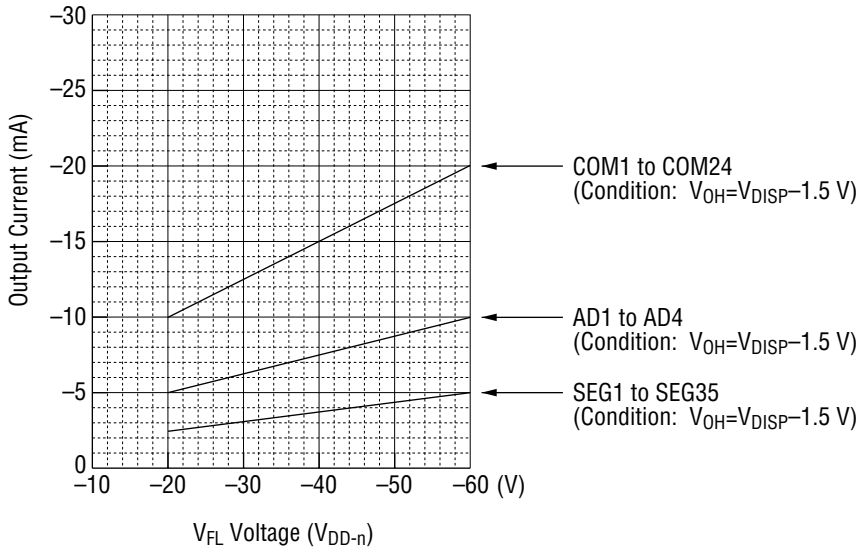
Notes: 1. The V_{DD} value depends on the power supply voltage of the microcontroller used. Adjust the values of the constants R_1, R_2, R_4, C_1, and C_2 to the power supply voltage used.

2. The V_{FL} value depends on the fluorescent display tube used. Adjust the values of the constants R_3 and ZD to the power supply voltage used.

Reference data

The figure below shows the relationship between the V_{FL} voltage and the output current of each driver.
Take care that the total power consumption to be used does not exceed the power dissipation.

V_{FL} Voltage vs. Output Current of Each Driver



MSM9201-01 ROM CODE

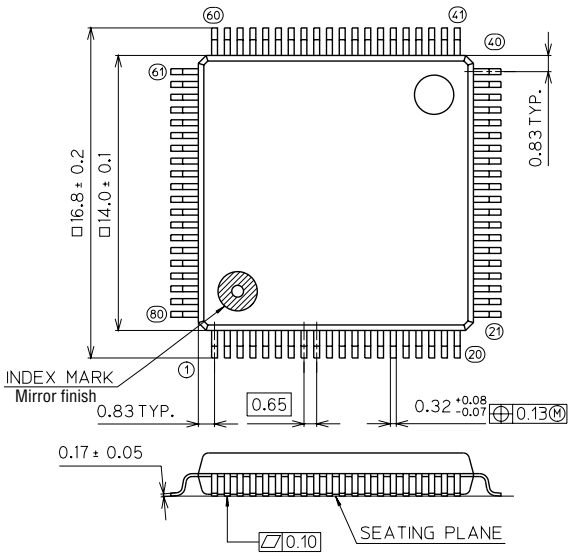
00000000B (00H) to 00001111B (0FH) are the CGRAM addresses.

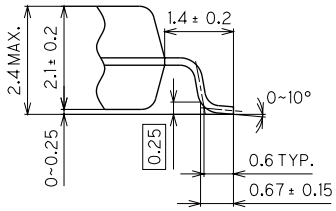
MSB / LSB	0000	0001	0010	0011	0100	0101	0110	0111	1000	1001	1010	1011	1100	1101	1110	1111
0000	RAM0															
0001	RAM1															
0010	RAM2															
0011	RAM3															
0100	RAM4															
0101	RAM5															
0110	RAM6															
0111	RAM7															
1000	RAM8															
1001	RAM9															
1010	RAMA															
1011	RAMB															
1100	RAMC															
1101	RAMD															
1110	RAME															
1111	RAMF															

PACKAGE DIMENSIONS

(Unit : mm)

QFP80-P-1414-0.65-K





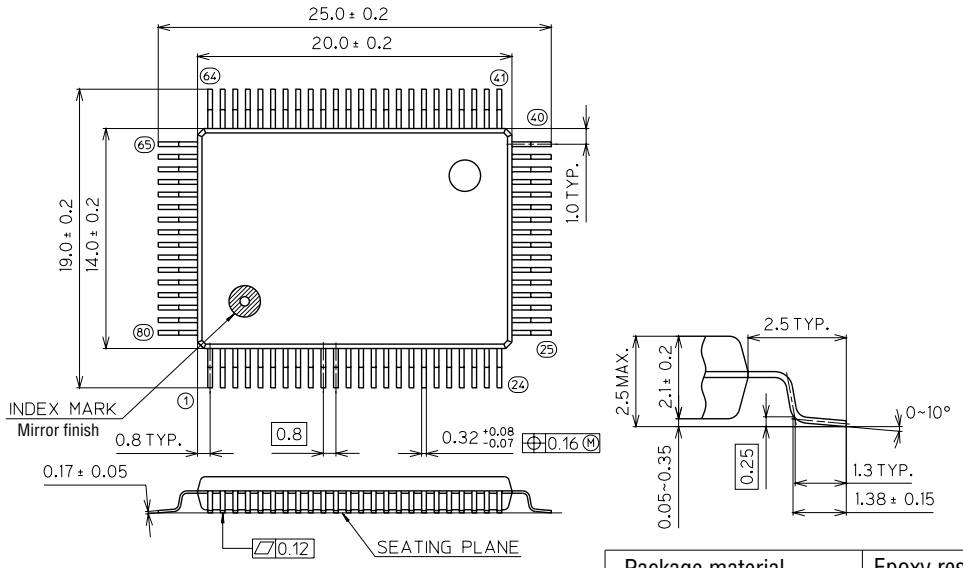
Package material	Epoxy resin
Lead frame material	42 alloy
Pin treatment	Solder plating
Solder plate thickness	5 μm or more
Package weight (g)	0.85 TYP.

Notes for Mounting the Surface Mount Type Package

The SOP, QFP, TSOP, SOJ, QFJ (PLCC), SHP and BGA are surface mount type packages, which are very susceptible to heat in reflow mounting and humidity absorbed in storage.
Therefore, before you perform reflow mounting, contact Oki's responsible sales person for the product name, package name, pin number, package code and desired mounting conditions (reflow method, temperature and times).

(Unit : mm)

QFP80-P-1420-0.80-BK



Package material	Epoxy resin
Lead frame material	42 alloy
Pin treatment	Solder plating
Solder plate thickness	5 μm or more
Package weight (g)	1.27 TYP.

Notes for Mounting the Surface Mount Type Package

The SOP, QFP, TSOP, SOJ, QFJ (PLCC), SHP and BGA are surface mount type packages, which are very susceptible to heat in reflow mounting and humidity absorbed in storage.
Therefore, before you perform reflow mounting, contact Oki's responsible sales person for the product name, package name, pin number, package code and desired mounting conditions (reflow method, temperature and times).