DDR SDRAM DIMM MODULE

MT8VDDT1664A, MT16VDDT3264A

For the latest data sheet, please refer to the Micron Web site: www.micron.com/mti/msp/html/datasheet.html

FEATURES

- 184-pin dual in-line memory modules (DIMM)
- Utilizes 100 MHz and 133 MHz DDR SDRAM components
- ECC-optimized pinout
- 128MB (16 Meg x 64), 256MB (32 Meg x 64)
- V_{DD} = +2.5V ±0.2V, V_{DDQ} = +2.5V ±0.2V
- 2.5V I/O (SSTL_2 compatible)
- Commands entered on each positive CK edge
- DQS edge-aligned with data for READs; center-aligned with data for WRITEs
- Internal, pipelined double data rate (DDR) architecture; two data accesses per clock cycle
- Bidirectional data strobe (DQS) transmitted/received with data, i.e., source-synchronous data capture
- Differential clock inputs (CK0 and CK0#)
- Four internal banks for concurrent operation
- Programmable burst lengths: 2, 4 or 8
- Auto Precharge option
- Auto Refresh and Self Refresh Modes
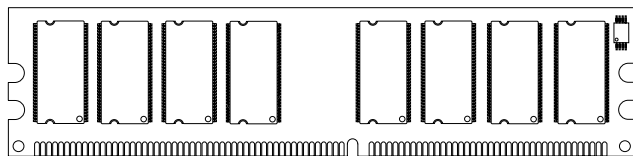- 15.6µs maximum average periodic refresh interval

OPTIONS   MARKING

- Package
  184-pin DIMM (gold)   G

- Frequency/CAS Latency
  266 MHz/CL = 2 (133 MHz DDR SDRAMs)   -262
  266 MHz/CL = 2.5 (133 MHz DDR SDRAMs)   -265
  200 MHz/CL = 2 (100 MHz DDR SDRAMs)   -202

184-Pin DIMM (front view)

PIN ASSIGNMENT

PIN	SYMBOL	PIN	SYMBOL	PIN	SYMBOL	PIN	SYMBOL
1	V_{REF}	47	DQS8	93	V_{SS}	139	V_{SS}
2	DQ0	48	A0	94	DQ4	140	DQS17
3	V_{SS}	49	CB2	95	DQ5	141	A10
4	DQ1	50	V_{SS}	96	V_{DDQ}	142	CB6
5	DQS0	51	CB3	97	DQS9	143	V_{DDQ}
6	DQ2	52	BA1	98	DQ6	144	CB7
7	V_{DD}	53	DQ32	99	DQ7	145	V_{SS}
8	DQ3	54	V_{DDQ}	100	V_{SS}	146	DQ36
9	NC	55	DQ33	101	NC	147	DQ37
10	NC	56	DQS4	102	NC	148	V_{DD}
11	V_{SS}	57	DQ34	103	NC (A13)	149	DQS13
12	DQ8	58	V_{SS}	104	V_{DDQ}	150	DQ38
13	DQ9	59	BA0	105	DQ12	151	DQ39
14	DQS1	60	DQ35	106	DQ13	152	V_{SS}
15	V_{DDQ}	61	DQ40	107	DQS10	153	DQ44
16	CK1	62	V_{DDQ}	108	V_{DD}	154	RAS#
17	CK1#	63	WE#	109	DQ14	155	DQ45
18	V_{SS}	64	DQ41	110	DQ15	156	V_{DDQ}
19	DQ10	65	CAS#	111	CKE1	157	S0#
20	DQ11	66	V_{SS}	112	V_{DDQ}	158	S1#
21	CKE0	67	DQS5	113	NC (BA2)	159	DQS14
22	V_{DDQ}	68	DQ42	114	DQ20	160	V_{SS}
23	DQ16	69	DQ43	115	NC (A12)	161	DQ46
24	DQ17	70	V_{DD}	116	V_{SS}	162	DQ47
25	DQS2	71	NC (S2#)	117	DQ21	163	NC (S3#)
26	V_{SS}	72	DQ48	118	A11	164	V_{DDQ}
27	A9	73	DQ49	119	DQS11	165	DQ52
28	DQ18	74	V_{SS}	120	V_{DD}	166	DQ53
29	A7	75	CK2#	121	DQ22	167	NC (FETEN)
30	V_{DDQ}	76	CK2	122	A8	168	V_{DD}
31	DQ19	77	V_{DDQ}	123	DQ23	169	DQS15
32	A5	78	DQS6	124	V_{SS}	170	DQ54
33	DQ24	79	DQ50	125	A6	171	DQ55
34	V_{SS}	80	DQ51	126	DQ28	172	V_{DDQ}
35	DQ25	81	V_{SS}	127	DQ29	173	NC
36	DQS3	82	V_{DDID}	128	V_{DDQ}	174	DQ60
37	A4	83	DQ56	129	DQS12	175	DQ61
38	V_{DD}	84	DQ57	130	A3	176	V_{SS}
39	DQ26	85	V_{DD}	131	DQ30	177	DQS16
40	DQ27	86	DQS7	132	V_{SS}	178	DQ62
41	A2	87	DQ58	133	DQ31	179	DQ63
42	V_{SS}	88	DQ59	134	CB4	180	V_{DDQ}
43	A1	89	V_{SS}	135	CB5	181	SA0
44	CB0	90	WP	136	V_{DDQ}	182	SA1
45	CB1	91	SDA	137	CK0	183	SA2
46	V_{DD}	92	SCL	138	CK0#	184	V_{DDSPD}

NOTE: Symbols in parentheses are not used on this module but may be used for other modules in this product family. They are for reference only.

KEY DDR SDRAM COMPONENT TIMING PARAMETERS

MODULE MARKING	SPEED GRADE	CLOCK FREQUENCY (1/tCK)	
		CL = 2*	CL = 2.5*
-262/-265	-7	133 MHz	143 MHz
-202	-75	100 MHz	133 MHz

*CL = CAS (READ) latency

PART NUMBERS

PART NUMBER	CONFIGURATION	SYSTEM BUS SPEED
MT8VDDT1664AG-262__	16 Meg x 64	CL = 2, 266 MHz
MT8VDDT1664AG-265__	16 Meg x 64	CL = 2.5, 266 MHz
MT8VDDT1664AG-202__	16 Meg x 64	CL = 2, 200 MHz
MT16VDDT3264AG-262__	32 Meg x 64	CL = 2, 266 MHz
MT16VDDT3264AG-265__	32 Meg x 64	CL = 2.5, 266 MHz
MT16VDDT3264AG-202__	32 Meg x 64	CL = 2, 200 MHz

NOTE: All part numbers end with a two-place code (not shown), designating component and PCB revisions. Consult factory for current revision codes. Example: MT16VDDT3264AG-262A1

GENERAL DESCRIPTION

The MT8VDDT1664A and MT16VDDT3264A are high-speed CMOS, dynamic random-access, 64MB and 128MB memories organized in a x64 configuration. These modules use internally configured quad-bank DDR SDRAMs.

These DDR SDRAM modules use a double data rate architecture to achieve high-speed operation. The double data rate architecture is essentially a 2n-prefetch architecture with an interface designed to transfer two data words per clock cycle at the I/O pins. A single read or write access for the DDR SDRAM module effectively consists of a single 2n-bit wide, one-clock-cycle data transfer at the internal DRAM core and two corresponding n-bit wide, one-half-clock-cycle data transfers at the I/O pins.

A bidirectional data strobe (DQS) is transmitted externally, along with data, for use in data capture at the receiver. DQS is an intermittent strobe transmitted by the DDR SDRAM during READs and by the memory controller during WRITEs. DQS is edge-aligned with data for READs and center-aligned with data for WRITEs.

These DDR SDRAM modules operate from a differential clock (CK0 and CK0#); the crossing of CK0 going HIGH and CK0# going LOW will be referred to as the positive edge of CK0. Commands (address and control signals) are registered at every positive edge of CK0. Input data is registered on both edges of DQS, and output data is referenced to both edges of DQS, as well as to both edges of CK0.

Read and write accesses to the DDR SDRAM modules are burst oriented; accesses start at a selected location and continue for a programmed number of locations in a programmed sequence. Accesses begin with the registration of an ACTIVE command, which is then followed by a READ or WRITE command. The address bits registered coincident with the ACTIVE command are used to select the bank and row to be accessed. The address bits registered coincident with the READ or WRITE command are used to select the bank and the starting column location for the burst access.

These DDR SDRAM modules provide for programmable READ or WRITE burst lengths of 2, 4 or 8 locations. An auto precharge function may be enabled to provide a self-timed row precharge that is initiated at the end of the burst access.
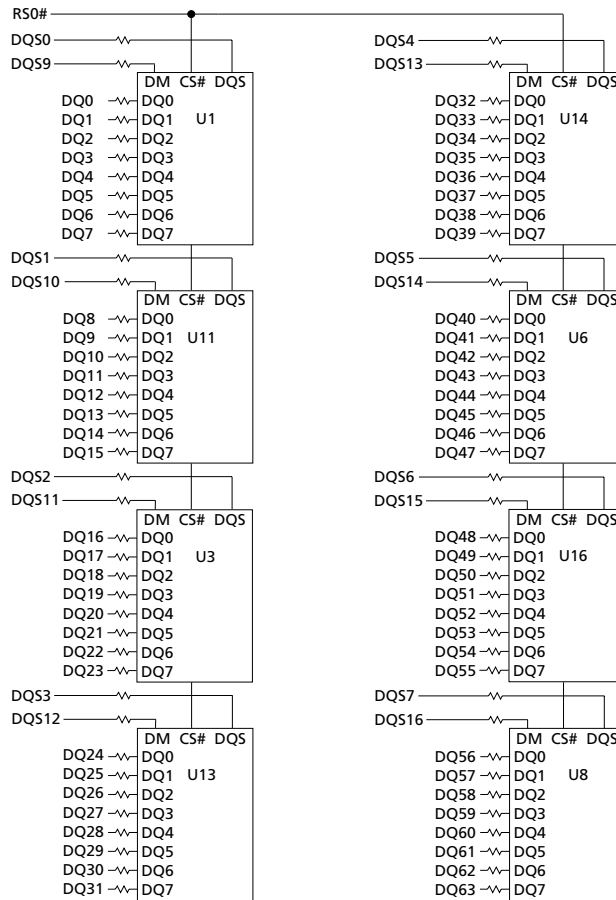
As with standard SDR SDRAM modules, the pipelined, multibank architecture of DDR SDRAM modules allows for concurrent operation, thereby providing high effective bandwidth by hiding row precharge and activation time.

An auto refresh mode is provided, along with a power-saving power-down mode. All inputs are compatible with the JEDEC Standard for SSTL_2. All outputs are SSTL_2, Class II compatible. For more information regarding DDR SDRAM operation, refer to the 128Mb x4, x8, x16 DDR SDRAM data sheet.
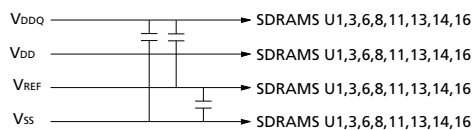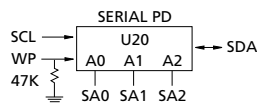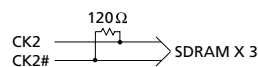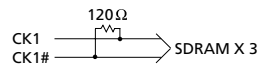
SERIAL PRESENCE-DETECT OPERATION

The DDR SDRAM modules incorporate serial presence-detect (SPD). The SPD function is implemented using a 2,048-bit EEPROM. This nonvolatile storage device contains 256 bytes. The first 128 bytes can be programmed by Micron to identify the module type and various SDRAM organizations and timing parameters. The remaining 128 bytes of storage are available for use by the customer. System READ/WRITE operations between the master (system logic) and the slave EEPROM device (DIMM) occur via a standard IIC bus using the DIMM's SCL (clock) and SDA (data) signals, together with SA(2:0), which provide eight unique DIMM/EEPROM addresses.

MICRON
SEMICONDUCTOR PRODUCTS, INC.

FUNCTIONAL BLOCK DIAGRAM
MT8VDDT1664A (128MB)

RS0#
DQS0
DQS9

DM CS# DQS
DQ0 — DQ0
DQ1 — DQ1   U1
DQ2 — DQ2
DQ3 — DQ3
DQ4 — DQ4
DQ5 — DQ5
DQ6 — DQ6
DQ7 — DQ7

DQS1
DQS10

DM CS# DQS
DQ8 — DQ0
DQ9 — DQ1   U11
DQ10 — DQ2
DQ11 — DQ3
DQ12 — DQ4
DQ13 — DQ5
DQ14 — DQ6
DQ15 — DQ7

DQS2
DQS11

DM CS# DQS
DQ16 — DQ0
DQ17 — DQ1   U3
DQ18 — DQ2
DQ19 — DQ3
DQ20 — DQ4
DQ21 — DQ5
DQ22 — DQ6
DQ23 — DQ7

DQS3
DQS12

DM CS# DQS
DQ24 — DQ0
DQ25 — DQ1   U13
DQ26 — DQ2
DQ27 — DQ3
DQ28 — DQ4
DQ29 — DQ5
DQ30 — DQ6
DQ31 — DQ7

DQS4
DQS13

DM CS# DQS
DQ32 — DQ0
DQ33 — DQ1   U14
DQ34 — DQ2
DQ35 — DQ3
DQ36 — DQ4
DQ37 — DQ5
DQ38 — DQ6
DQ39 — DQ7

DQS5
DQS14

DM CS# DQS
DQ40 — DQ0
DQ41 — DQ1   U6
DQ42 — DQ2
DQ43 — DQ3
DQ44 — DQ4
DQ45 — DQ5
DQ46 — DQ6
DQ47 — DQ7

DQS6
DQS15

DM CS# DQS
DQ48 — DQ0
DQ49 — DQ1   U16
DQ50 — DQ2
DQ51 — DQ3
DQ52 — DQ4
DQ53 — DQ5
DQ54 — DQ6
DQ55 — DQ7

DQS7
DQS16

DM CS# DQS
DQ56 — DQ0
DQ57 — DQ1   U8
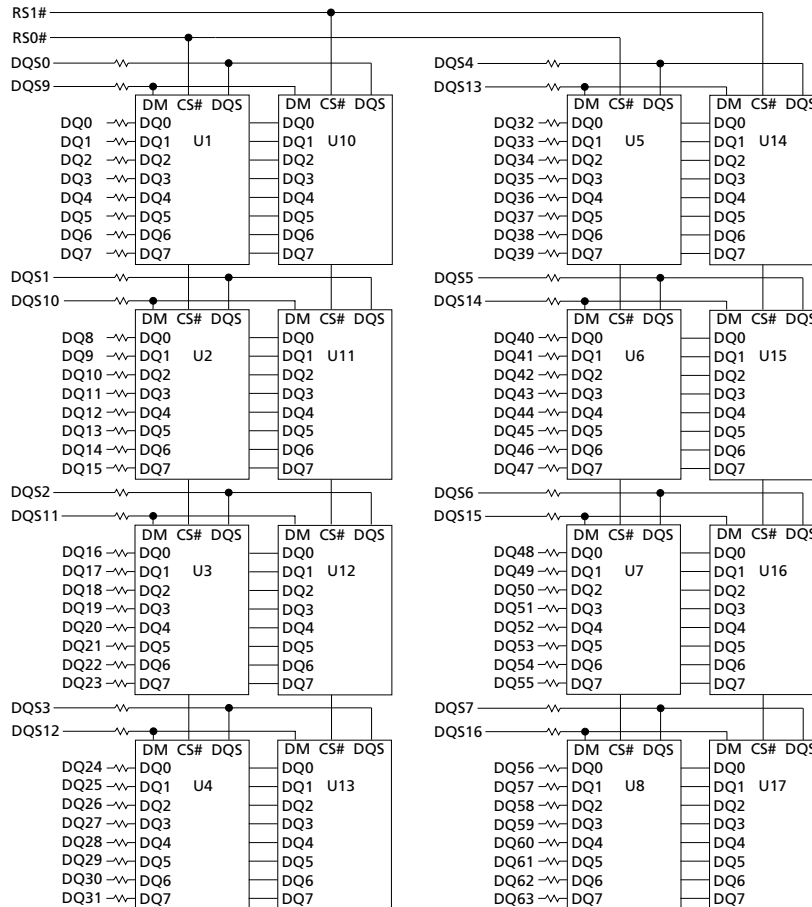DQ58 — DQ2
DQ59 — DQ3
DQ60 — DQ4
DQ61 — DQ5
DQ62 — DQ6
DQ63 — DQ7

BA0, BA1 → BA0, BA1: SDRAMS U1,3,6,8,11,13,14,16
A0-A11 → A0-A11: SDRAMS U1,3,6,8,11,13,14,16
RAS# → RAS#: SDRAMS U1,3,6,8,11,13,14,16
CAS# → CAS#: SDRAMS U1,3,6,8,11,13,14,16
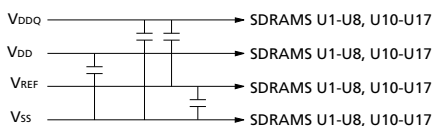CKE0 → CKE0: SDRAMS U1,3,6,8,11,13,14,16
WE# → WE#: SDRAMS U1,3,6,8,11,13,14,16

120Ω
CK0
CK0# → SDRAM X 2

120Ω
CK1
CK1# → SDRAM X 3

120Ω
CK2
CK2# → SDRAM X 3

SERIAL PD
SCL   U20   → SDA
WP   A0   A1   A2
47K
      SA0 SA1 SA2

V_{DDQ} → SDRAMS U1,3,6,8,11,13,14,16
V_{DD} → SDRAMS U1,3,6,8,11,13,14,16
V_{REF} → SDRAMS U1,3,6,8,11,13,14,16
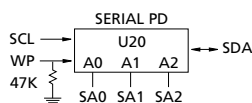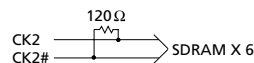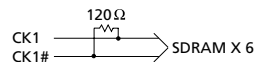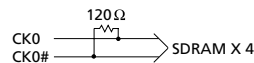V_{SS} → SDRAMS U1,3,6,8,11,13,14,16
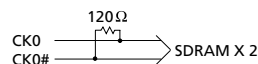
NOTE: All resistor values are 22 ohms unless otherwise specified.   U1,3,6,8,11,13,14,16 = MT46V16M8TG DDR SDRAMs

MICRON®
SEMICONDUCTOR PRODUCTS, INC.

FUNCTIONAL BLOCK DIAGRAM
MT16VDDT3264A (256MB)

RS1#
RS0#
DQS0
DQS9

DM CS# DQS	DM CS# DQS
DQ0 — DQ0	DQ0
DQ1 — DQ1 U1	DQ1 U10
DQ2 — DQ2	DQ2
DQ3 — DQ3	DQ3
DQ4 — DQ4	DQ4
DQ5 — DQ5	DQ5
DQ6 — DQ6	DQ6
DQ7 — DQ7	DQ7

DQS4
DQS13

DM CS# DQS	DM CS# DQS
DQ32 — DQ0	DQ0
DQ33 — DQ1 U5	DQ1 U14
DQ34 — DQ2	DQ2
DQ35 — DQ3	DQ3
DQ36 — DQ4	DQ4
DQ37 — DQ5	DQ5
DQ38 — DQ6	DQ6
DQ39 — DQ7	DQ7

DQS1
DQS10

DM CS# DQS	DM CS# DQS
DQ8 — DQ0	DQ0
DQ9 — DQ1 U2	DQ1 U11
DQ10 — DQ2	DQ2
DQ11 — DQ3	DQ3
DQ12 — DQ4	DQ4
DQ13 — DQ5	DQ5
DQ14 — DQ6	DQ6
DQ15 — DQ7	DQ7

DQS5
DQS14

DM CS# DQS	DM CS# DQS
DQ40 — DQ0	DQ0
DQ41 — DQ1 U6	DQ1 U15
DQ42 — DQ2	DQ2
DQ43 — DQ3	DQ3
DQ44 — DQ4	DQ4
DQ45 — DQ5	DQ5
DQ46 — DQ6	DQ6
DQ47 — DQ7	DQ7

DQS2
DQS11

DM CS# DQS	DM CS# DQS
DQ16 — DQ0	DQ0
DQ17 — DQ1 U3	DQ1 U12
DQ18 — DQ2	DQ2
DQ19 — DQ3	DQ3
DQ20 — DQ4	DQ4
DQ21 — DQ5	DQ5
DQ22 — DQ6	DQ6
DQ23 — DQ7	DQ7

DQS6
DQS15

DM CS# DQS	DM CS# DQS
DQ48 — DQ0	DQ0
DQ49 — DQ1 U7	DQ1 U16
DQ50 — DQ2	DQ2
DQ51 — DQ3	DQ3
DQ52 — DQ4	DQ4
DQ53 — DQ5	DQ5
DQ54 — DQ6	DQ6
DQ55 — DQ7	DQ7

DQS3
DQS12

DM CS# DQS	DM CS# DQS
DQ24 — DQ0	DQ0
DQ25 — DQ1 U4	DQ1 U13
DQ26 — DQ2	DQ2
DQ27 — DQ3	DQ3
DQ28 — DQ4	DQ4
DQ29 — DQ5	DQ5
DQ30 — DQ6	DQ6
DQ31 — DQ7	DQ7

DQS7
DQS16

DM CS# DQS	DM CS# DQS
DQ56 — DQ0	DQ0
DQ57 — DQ1 U8	DQ1 U17
DQ58 — DQ2	DQ2
DQ59 — DQ3	DQ3
DQ60 — DQ4	DQ4
DQ61 — DQ5	DQ5
DQ62 — DQ6	DQ6
DQ63 — DQ7	DQ7

BA0, BA1 → BA0, BA1: SDRAMS U1-U8, U10-U17
A0-A11 → A0-A11: SDRAMS U1-U8, U10-U17
RAS# → RAS#: SDRAMS U1-U8, U10-U17
CAS# → CAS#: SDRAMS U1-U8, U10-U17
CKE0 → CKE0: SDRAMS U1-U8
CKE1 → CKE1: SDRAMS U10-U17
WE# → WE#: SDRAMS U1-U8, U10-U17

CK0 — 120Ω → SDRAM X 4
CK0#

CK1 — 120Ω → SDRAM X 6
CK1#

CK2 — 120Ω → SDRAM X 6
CK2#

SERIAL PD
SCL → U20
WP → A0 A1 A2 ← SDA
47K
SA0 SA1 SA2

V_{DDQ} → SDRAMS U1-U8, U10-U17
V_{DD} → SDRAMS U1-U8, U10-U17
V_{REF} → SDRAMS U1-U8, U10-U17
V_{SS} → SDRAMS U1-U8, U10-U17

NOTE: All resistor values are 22 ohms unless otherwise specified.   U1-U8, U10-U17 = MT46V16M8TG DDR SDRAMs

PIN DESCRIPTIONS

PIN NUMBERS	SYMBOL	TYPE	DESCRIPTION
63, 65, 154	WE#, CAS#, RAS#	Input	Command Inputs: WE#, CAS# and RAS# (along with S0#, S1#) define the command being entered.
137, 138, 16, 17, 76, 75	CK0, CK0#, CK1, CK1#, CK2, CK2#	Input	Clocks: CK and CK# are differential clock inputs. All address and control input signals are sampled on the crossing of the positive edge of CK and negative edge of CK#. Output data (DQs and DQS) is referenced to the crossings of CK and CK#.
21, 111	CKE0, CKE1	Input	Clock Enables: CKE0 and CKE1 activate (HIGH) and deactivate (LOW) internal clock signals, and device input buffers and output drivers. Deactivating the clock provides PRECHARGE POWER-DOWN and SELF REFRESH operation (all banks idle), or ACTIVE POWER-DOWN (row ACTIVE in any bank). CKE0 and CKE1 are synchronous for all functions except for disabling outputs, which is achieved asynchronously. CKE0 and CKE1 must be maintained HIGH throughout read and write accesses. Input buffers (excluding CK0, CK0# and CKE) are disabled during POWER-DOWN. Input buffers (excluding CKE0 and CKE1) are disabled during SELF REFRESH. CKE0 and CKE1 are SSTL_2 inputs but will detect an LVCMOS LOW level after V_{DD} is applied.
157, 158	S0#, S1#	Input	Chip Selects: S0# and S1# enable (registered LOW) and disable (registered HIGH) the command decoder. All commands are masked when S0# and S1# are registered HIGH. S0# and S1# provide for external bank selection on systems with multiple banks. S0# and S1# are considered part of the command code.
59, 52	BA0, BA1	Input	Bank Addresses: BA0 and BA1 define to which bank an ACTIVE, READ, WRITE or PRECHARGE command is being applied.
48, 43, 41, 130, 37, 32, 125, 29, 122, 27, 141, 118	A0-A11	Input	Address Inputs: A0-A11 are sampled during the ACTIVE command (row-address A0-A11) and READ/WRITE command (column-address A0-A9, with A10 defining auto precharge) to select one location out of the memory array in the respective bank. A10 is sampled during a PRECHARGE command to determine whether the PRECHARGE applies to one bank (A10 LOW) or all banks (A10 HIGH). The address inputs also provide the op-code during a MODE REGISTER SET command.
1	V_{REF}	Input	SSTL_2 reference voltage.
82	V_{DDID}	Input	V_{DD} identification flag.
90	WP	Input	Write Protect: Serial presence-detect hardware write protect.
92	SCL	Input	Serial Clock for Presence-Detect: SCL is used to synchronize the presence-detect data transfer to and from the module.

PIN DESCRIPTIONS

PIN NUMBERS	SYMBOL	TYPE	DESCRIPTION
181, 182, 183	SA0-SA2	Input	Presence-Detect Address Inputs: These pins are used to configure the presence-detect device.
44, 45, 49, 51, 134, 135, 142, 144	CB0-CB7	Input/Output	Data I/Os: Check bits.
5, 14, 25, 36, 56, 67, 78, 86, 47, 97, 107, 119, 129, 149, 159, 169, 177, 140	DQS0-DQS17	Input/Output	Data Strobes: Output with read data, input with write data. Edge-aligned with read data, centered in write data. Used to capture write data.
2, 4, 6, 8, 12, 13, 19, 20, 23, 24, 28, 31, 33, 35, 39, 40, 53, 55, 57, 60, 61, 64, 68, 69, 72, 73, 79, 80, 83, 84, 87, 88, 94, 95, 98, 99, 105, 106, 109, 110, 114, 117, 121, 123, 126, 127, 131, 133, 146, 147, 150, 151, 153, 155, 161, 162, 165, 166, 170, 171, 174, 175, 178, 179	DQ0-DQ63	Input/Output	Data I/Os: Data bus.
91	SDA	Input/Output	Serial Presence-Detect Data: SDA is a bidirectional pin used to transfer addresses and data into and out of the presence-detect portion of the module.
15, 22, 30, 54, 62, 77, 96, 104, 112, 128, 136, 143, 156, 164, 172, 180	$V_{DD}Q$	Supply	DQ Power Supply: +2.5V $\pm$0.2V.
7, 38, 46, 70, 85, 108, 120, 148, 168	V_{DD}	Supply	Power Supply: +2.5V $\pm$0.2V.
3, 11, 18, 26, 34, 42, 50, 58, 66, 74, 81, 89, 93, 100, 116, 124, 132, 139, 145, 152, 160, 176	V_{SS}	Supply	Ground.
184	V_{DDSPD}	Supply	Serial EEPROM positive power supply: 2.2V to 3.7V. This supply is isolated from the V_{DD}/$V_{DD}Q$ supply.
9, 10, 71, 101, 102, 103, 113, 115, 163, 167, 173	NC	–	No Connects.

SPD CLOCK AND DATA CONVENTIONS

Data states on the SDA line can change only during SCL LOW. SDA state changes during SCL HIGH are reserved for indicating start and stop conditions (Figures 1 and 2).

SPD START CONDITION

All commands are preceded by the start condition, which is a HIGH-to-LOW transition of SDA when SCL is HIGH. The SPD device continuously monitors the SDA and SCL lines for the start condition and will not respond to any command until this condition has been met.

SPD STOP CONDITION

All communications are terminated by a stop condition, which is a LOW-to-HIGH transition of SDA when SCL is HIGH. The stop condition is also used to place the SPD device into standby power mode.
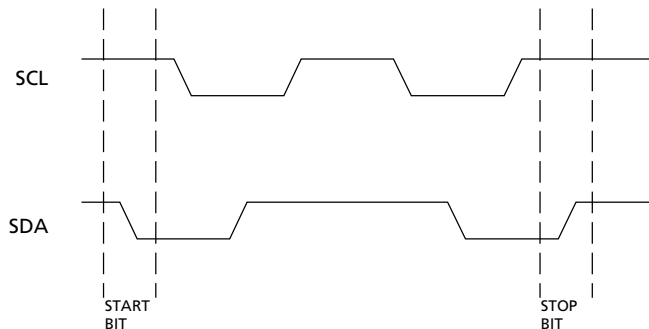
SPD ACKNOWLEDGE

Acknowledge is a software convention used to indicate successful data transfers. The transmitting device, either master or slave, will release the bus after transmitting eight bits. During the ninth clock cycle, the receiver will pull the SDA line LOW to acknowledge that it received the eight bits of data (Figure 3).

The SPD device will always respond with an acknowledge after recognition of a start condition and its slave address. If both the device and a WRITE operation have been selected, the SPD device will respond with an acknowledge after the receipt of each subsequent eight-bit word. In the read mode the SPD device will transmit eight bits of data, release the SDA line and monitor the line for an acknowledge. If an acknowledge is detected and no stop condition is generated by the master, the slave will continue to transmit data. If an acknowledge is not detected, the slave will terminate further data transmissions and await the stop condition to return to standby power mode.
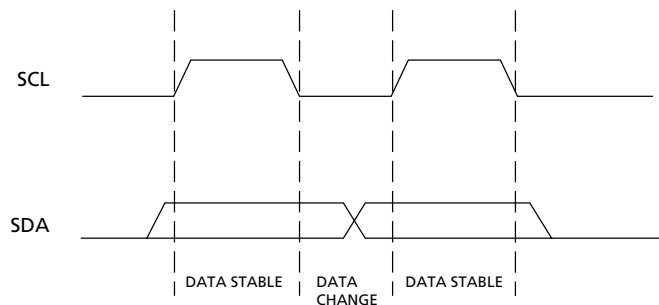
**Figure 1
Data Validity**

**Figure 2
Definition of Start and Stop**
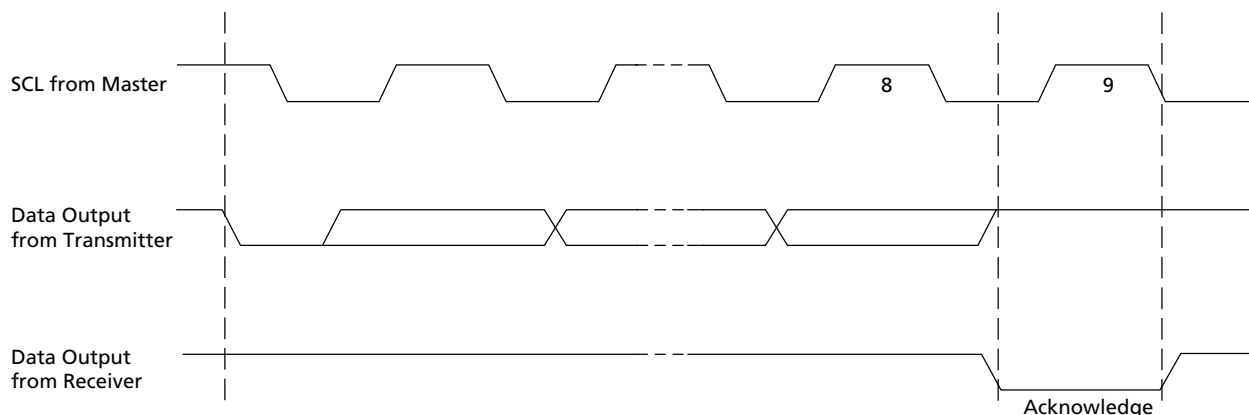
**Figure 3
Acknowledge Response From Receiver**

SERIAL PRESENCE-DETECT MATRIX

BYTE	DESCRIPTION	ENTRY (VERSION)	MT8VDDT1664A	MT16VDDT3264A
0	NUMBER OF BYTES USED BY MICRON	128	80	80
1	TOTAL NUMBER OF SPD MEMORY BYTES	256	08	08
2	MEMORY TYPE	SDRAM DDR	07	07
3	NUMBER OF ROW ADDRESSES	12	0C	0C
4	NUMBER OF COLUMN ADDRESSES	10	0A	0A
5	NUMBER OF BANKS	1 or 2	01	02
6	MODULE DATA WIDTH	64	40	40
7	MODULE DATA WIDTH (continued)	0	00	00
8	MODULE VOLTAGE INTERFACE LEVELS	SSTL 2.5V	04	04
9	SDRAM CYCLE TIME, ^{t}CK (CAS LATENCY = 2.5)	7 (-262) 7.5 (-265) 8 (-202)	70 75 80	70 75 80
10	SDRAM ACCESS FROM CLOCK, ^{t}AC (CAS LATENCY = 2.5)	0.75 (-262/-265) 0.8 (-202)	75 80	75 80
11	MODULE CONFIGURATION TYPE	NON-ECC	00	00
12	REFRESH RATE/TYPE	15.6µs/SELF	80	80
13	SDRAM WIDTH (PRIMARY SDRAM)	8	08	08
14	ERROR-CHECKING SDRAM DATA WIDTH	NONE	00	00
15	MINIMUM CLOCK DELAY, BACK-TO-BACK RANDOM COLUMN ACCESS	1	01	01
16	BURST LENGTHS SUPPORTED	2, 4, 8	0E	0E
17	NUMBER OF BANKS ON SDRAM DEVICE	4	04	04
18	CAS LATENCIES SUPPORTED	2, 2.5	0C	0C
19	CS LATENCY	1	02	02
20	WE LATENCY	1	02	02
21	SDRAM MODULE ATTRIBUTES		20	20
22	SDRAM DEVICE ATTRIBUTES: GENERAL		00	00
23	SDRAM CYCLE TIME, ^{t}CK (CAS LATENCY = 2)	7.5 (-262) 10 (-265/-202)	75 A0	75 A0
24	SDRAM CYCLE TIME, ^{t}CK (CAS LATENCY = 2)	7 (-262) 7.5 (-265) 8 (-202)	70 75 80	70 75 80
25	SDRAM CYCLE TIME, ^{t}CK (CAS LATENCY = 1)	–	00	00
26	SDRAM ACCESS FROM CLK , ^{t}AC (CAS LATENCY = 1)	–	00	00
27	MINIMUM ROW PRECHARGE TIME, ^{t}RP	20	50	50
28	MINIMUM ROW ACTIVE TO ROW ACTIVE, ^{t}RRD	15	3C	3C
29	MINIMUM RAS# TO CAS# DELAY, ^{t}RCD	20	50	50
30	MINIMUM RAS# PULSE WIDTH, ^{t}RAS	45 (-262/-265) 50 (-202)	2D 32	2D 32
31	MODULE BANK DENSITY	128MB	20	20

NOTE: "1"/"0": Serial Data, "driven to HIGH"/"driven to LOW."

SERIAL PRESENCE-DETECT MATRIX (continued)

BYTE	DESCRIPTION	ENTRY (VERSION)	MT8VDDT864A	MT16VDDT1664A
32	ADDRESS AND COMMAND SETUP TIME, ^tIS	0.75 (-262/-265) 1.2 (-202)	75 C0	75 C0
33	ADDRESS AND COMMAND HOLD TIME, ^tIH	0.75 (-262/-265) 1.2 (-202)	75 C0	75 C0
34	DATA/DATA MASK INPUT SETUP TIME, ^tDS	0.5 (-262/-265) 0.6 (-202)	50 60	50 60
35	DATA/DATA MASK INPUT HOLD TIME, ^tDH	0.5 (-262/-265) 0.6 (-202)	50 60	50 60
36-61	RESERVED		00	00
62	SPD REVISION	0	00	00
63	CHECKSUM FOR BYTES 0-62	-262 -265 -202	34 69 45	35 6A 46
64	MANUFACTURER'S JEDEC ID CODE	MICRON	2C	2C
65-71	MANUFACTURER'S JEDEC ID CODE (continued)		FF	FF
72	MANUFACTURING LOCATION		01 02 03 04 05 06 07 08 09	01 02 03 04 05 06 07 08 09
73-90	MODULE PART NUMBER (ASCII)		x	x
91	PCB IDENTIFICATION CODE	1 2 3 4 5 6 7 8 9	01 02 03 04 05 06 07 08 09	01 02 03 04 05 06 07 08 09
92	IDENTIFICATION CODE (continued)	0	00	00
93	YEAR OF MANUFACTURE IN BCD		x	x
94	WEEK OF MANUFACTURE IN BCD		x	x
95-98	MODULE SERIAL NUMBER		x	x
99-127	MANUFACTURER-SPECIFIC DATA (RSVD)		–	–

NOTE: 1. "1"/"0": Serial Data, "driven to HIGH"/"driven to LOW."
       2. x = Variable Data.

COMMANDS

Truth Table 1 provides a general reference of available commands. For a more detailed description of commands and operations, refer to the 128Mb: x4, x8, x16 SDRAM DDR data sheet.

TRUTH TABLE 1 – COMMANDS
(Note: 1)

NAME (FUNCTION)	CS#	RAS#	CAS#	WE#	ADDR	NOTES
DESELECT (NOP)	H	X	X	X	X	9
NO OPERATION (NOP)	L	H	H	H	X	9
ACTIVE (Select bank and activate row)	L	L	H	H	Bank/Row	3
READ (Select bank and column, and start READ burst)	L	H	L	H	Bank/Col	4
WRITE (Select bank and column, and start WRITE burst)	L	H	L	L	Bank/Col	4
BURST TERMINATE	L	H	H	L	X	8
PRECHARGE (Deactivate row in bank or banks)	L	L	H	L	Code	5
AUTO REFRESH or SELF REFRESH (Enter self refresh mode)	L	L	L	H	X	6, 7
LOAD MODE REGISTER	L	L	L	L	Op-Code	2

TRUTH TABLE 1A – DM OPERATION

NAME (FUNCTION)	DM	DQs	NOTES
Write Enable	L	Valid	10
Write Inhibit	H	X	10

NOTE:
1. CKE is HIGH for all commands shown except SELF REFRESH.
2. BA0-BA1 select either the mode register or the extended mode register (BA0 = 0, BA1 = 0 select the mode register; BA0 = 1, BA1 = 0 select extended mode register; other combinations of BA0-BA1 are reserved). A0-A11 provide the op-code to be written to the selected mode register.
3. BA0-BA1 provide bank address and A0-A11 provide row address.
4. BA0-BA1 provide bank address; A0-A9 provide column address; A10 HIGH enables the auto precharge feature (nonpersistent), and A10 LOW disables the auto precharge feature.
5. A10 LOW: BA0-BA1 determine which bank is precharged.
   A10 HIGH: all banks are precharged and BA0-BA1 are "Don't Care."
6. This command is AUTO REFRESH if CKE is HIGH, SELF REFRESH if CKE is LOW.
7. Internal refresh counter controls row addressing; all inputs and I/Os are "Don't Care" except for CKE.
8. Applies only to read bursts with auto precharge disabled; this command is undefined (and should not be used) for READ bursts with auto precharge enabled and for WRITE bursts.
9. DESELECT and NOP are functionally interchangeable.
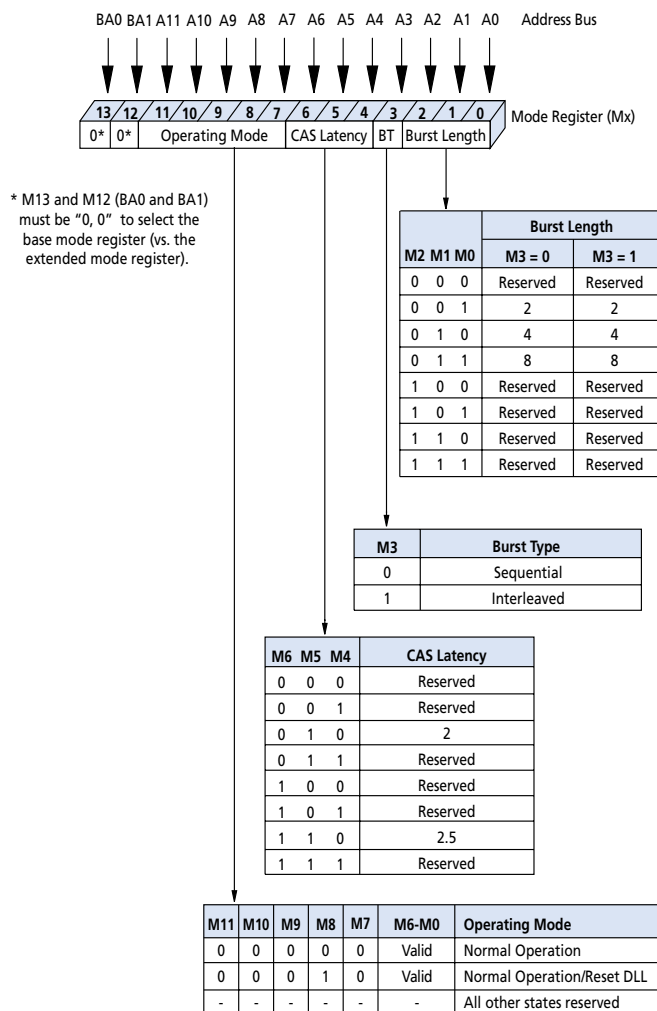10. Used to mask write data; provided coincident with the corresponding data.

BA0 BA1 A11 A10 A9 A8 A7 A6 A5 A4 A3 A2 A1 A0   Address Bus

13	12	11/10/9/8/7	6/5/4	3	2/1/0	Mode Register (Mx)
0*	0*	Operating Mode	CAS Latency	BT	Burst Length	

* M13 and M12 (BA0 and BA1) must be "0, 0" to select the base mode register (vs. the extended mode register).

			Burst Length	
M2	**M1**	**M0**	**M3 = 0**	**M3 = 1**
0	0	0	Reserved	Reserved
0	0	1	2	2
0	1	0	4	4
0	1	1	8	8
1	0	0	Reserved	Reserved
1	0	1	Reserved	Reserved
1	1	0	Reserved	Reserved
1	1	1	Reserved	Reserved

M3	**Burst Type**
0	Sequential
1	Interleaved

M6	**M5**	**M4**	**CAS Latency**
0	0	0	Reserved
0	0	1	Reserved
0	1	0	2
0	1	1	Reserved
1	0	0	Reserved
1	0	1	Reserved
1	1	0	2.5
1	1	1	Reserved

M11	**M10**	**M9**	**M8**	**M7**	**M6-M0**	**Operating Mode**
0	0	0	0	0	Valid	Normal Operation
0	0	0	1	0	Valid	Normal Operation/Reset DLL
-	-	-	-	-	-	All other states reserved

Figure 4
Mode Register Definition

Table 1
Burst Definition

Burst Length	Starting Column Address		Order of Accesses Within a Burst	
			Type = Sequential	Type = Interleaved
2		**A0**		
		0	0-1	0-1
		1	1-0	1-0
4	**A1**	**A0**		
	0	0	0-1-2-3	0-1-2-3
	0	1	1-2-3-0	1-0-3-2
	1	0	2-3-0-1	2-3-0-1
	1	1	3-0-1-2	3-2-1-0
8	**A2**	**A1** **A0**		
	0	0 0	0-1-2-3-4-5-6-7	0-1-2-3-4-5-6-7
	0	0 1	1-2-3-4-5-6-7-0	1-0-3-2-5-4-7-6
	0	1 0	2-3-4-5-6-7-0-1	2-3-0-1-6-7-4-5
	0	1 1	3-4-5-6-7-0-1-2	3-2-1-0-7-6-5-4
	1	0 0	4-5-6-7-0-1-2-3	4-5-6-7-0-1-2-3
	1	0 1	5-6-7-0-1-2-3-4	5-4-7-6-1-0-3-2
	1	1 0	6-7-0-1-2-3-4-5	6-7-4-5-2-3-0-1
	1	1 1	7-0-1-2-3-4-5-6	7-6-5-4-3-2-1-0

NOTE:
1. For a burst length of two, A1-A9 select the two-data-element block; A0 selects the first access within the block.
2. For a burst length of four, A2-A9 select the four-data-element block; A0-A1 select the first access within the block.
3. For a burst length of eight, A3-A9 select the eight-data-element block; A0-A2 select the first access within the block.
4. Whenever a boundary of the block is reached within a given sequence above, the following access wraps within the block.

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ABSOLUTE MAXIMUM RATINGS*

Voltage on V_{DD} Supply
    Relative to V_{SS} .... -1V to +4.6V
Voltage on V_{DDQ} Supply
    Relative to V_{SS} .... -1V to +3.6V
Voltage on V_{REF} and Inputs
    Relative to V_{SS} .... -1V to +3.6V
Voltage on I/O Pins
    Relative to V_{SS} ....-0.5V to V_{DDQ} +0.5V
Operating Temperature, T_A (ambient) ... 0°C to +70°C
Storage Temperature (plastic) .... -55°C to +150°C
Power Dissipation 18W
Short Circuit Output Current 50mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

DC ELECTRICAL CHARACTERISTICS AND OPERATING CONDITIONS

(Notes: 1-6) (0°C ≤ T_A ≤ +70°C; V_{DD} = +2.5V ±0.2V, V_{DDQ} = +2.5V ±0.2V)

PARAMETER/CONDITION		SYMBOL	MIN	MAX	UNITS	NOTES
Supply Voltage		V_{DD}	2.3	2.7	V	
I/O Supply Voltage		V_{DDQ}	2.3	2.7	V	
I/O Reference Voltage		V_{REF}	0.49 x V_{DDQ}	0.51 x V_{DDQ}	V	7
I/O Termination Voltage (system)		V_{TT}	V_{REF} - 0.04	V_{REF} + 0.04	V	8
Input High (Logic 1) Voltage		V_{IH}	V_{REF} + 0.18	V_{DD} + 0.3	V	9
Input Low (Logic 0) Voltage		V_{IL}	-0.3	V_{REF} - 0.18	V	9
Clock Input Voltage Level; CK0 and CK0#		V_{IN}	-0.3	V_{DDQ} + 0.3	V	
Clock Input Differential Voltage; CK0 and CK0#		V_{ID}	0.36	V_{DDQ} + 0.6	V	10
Clock Input Crossing Point Voltage; CK0 and CK0#		V_{IX}	1.15	1.35	V	11
INPUT LEAKAGE CURRENT Any input 0V ≤ V_{IN} ≤ V_{DD} (All other pins not under test = 0V)	WE#, RAS#, CAS#, BA0 BA1	I_{I1}	-32	32	µA	12
	S0#, S1#, CKE0, CKE1	I_{I2}	-16	16	µA	
	CK, CK#	I_{I3}	-12	12	µA	12
OUTPUT LEAKAGE CURRENT (DQs are disabled; 0V ≤ V_{OUT} ≤ V_{DDQ})	DQ0-DQ63, DQS0-DQS17	I_{OZ}	-10	10	µA	12
OUTPUT LEVELS Output High Current (V_{OUT} = 1.95V, maximum V_{TT})		I_{OH}	-15.2	–	mA	
Output Low Current (V_{OUT} = 0.35V, minimum V_{TT})		I_{OL}	15.2	–	mA	

NOTE: 1. All voltages referenced to V_{SS}.
     2. Tests for AC timing, I_{DD}, and electrical AC and DC characteristics may be conducted at nominal reference/supply voltage levels, but the related specifications and device operation are guaranteed for the full voltage range specified.
     3. Outputs measured with equivalent load:

V_{TT}
25Ω
Output ---- 25Ω ---- Timing Reference Point
(V_{OUT})
30pF
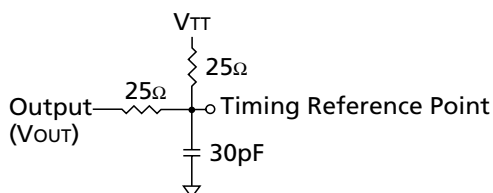
NOTES: (continued)

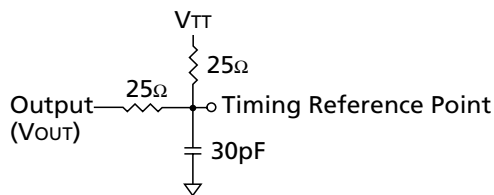4. AC timing and I_{DD} tests may use a V_{IL}-to-V_{IH} swing of up to 1.5V in the test environment, but input timing is still referenced to V_{REF} (or to the crossing point for CK/CK#), and parameter specifications are guaranteed for the specified AC input levels under normal use conditions. The minimum slew rate for the input signals used to test the device is 1V/ns in the range between $V_{IL}(AC)$ and $V_{IH}(AC)$.

5. The AC and DC input level specifications are as defined in the SSTL_2 Standard (i.e., the receiver will effectively switch as a result of the signal crossing the AC input level, and will remain in that state as long as the signal does not ring back above [below] the DC input LOW [HIGH] level).

6. Inputs are not recognized as valid until V_{REF} stabilizes. Exception: during the period before V_{REF} stabilizes, CKE ≤ 0.3 x $V_{DD}Q$ is recognized as LOW.

7. V_{REF} is expected to equal $V_{DD}Q/2$ of the transmitting device and to track variations in the DC level of the same. Peak-to-peak noise on V_{REF} may not exceed ±2 percent of the DC value. Thus, from $V_{DD}Q/2$, V_{REF} is allowed ±25mV for DC error and ±25mV for AC noise.

8. V_{TT} is not applied directly to the device. V_{TT} is a system supply for signal termination resistors, is expected to be set equal to V_{REF} and must track variations in the DC level of V_{REF}.

9. The DC values define where the input slew rate requirements are imposed, and the input signal must not violate these levels in order to maintain a valid level. The inputs require the AC value to be achieved during signal transition edge.

10. V_{ID} is the magnitude of the difference between the input level on CK and the input level on CK#.

11. The value of V_{IX} is expected to equal $V_{DD}Q/2$ of the transmitting device and must track variations in the DC level of the same.

12. 64MB module values will be half of those shown.

AC OPERATING CONDITIONS

(Notes: 1-7) (0°C $\leq$ T$_A$ $\leq$ +70°C; V$_{DD}$ = +2.5V ±0.2V, V$_{DDQ}$ = +2.5V ±0.2V)

PARAMETER/CONDITION	SYMBOL	MIN	MAX	UNITS	NOTES
Input High (Logic 1) Voltage; DQ, DQS and DM signals	V$_{IH}$(AC)	V$_{REF}$ + 0.35	–	V	6, 8
Input Low (Logic 0) Voltage; DQ, DQS and DM signals	V$_{IL}$(AC)	–	V$_{REF}$ - 0.35	V	6, 8
Clock Input Differential Voltage; CK and CK#	V$_{ID}$(AC)	0.7	V$_{DDQ}$ + 0.6	V	9
Clock Input Crossing Point Voltage; CK and CK#	V$_{IX}$(AC)	0.5 x V$_{DDQ}$ - 0.2	0.5 x V$_{DDQ}$ + 0.2	V	10

NOTE:
1. All voltages referenced to V$_{SS}$.
2. Tests for AC timing, I$_{DD}$, and electrical AC and DC characteristics may be conducted at nominal reference/supply voltage levels, but the related specifications and device operation are guaranteed for the full voltage range specified.
3. Outputs measured with equivalent load:

4. AC timing and I$_{DD}$ tests may use a V$_{IL}$-to-V$_{IH}$ swing of up to 1.5V in the test environment, but input timing is still referenced to V$_{REF}$ (or to the crossing point for CK/CK#), and parameter specifications are guaranteed for the specified AC input levels under normal use conditions. The minimum slew rate for the input signals used to test the device is 1V/ns in the range between V$_{IL}$(AC) and V$_{IH}$(AC).
5. The AC and DC input level specifications are as defined in the SSTL_2 Standard (i.e., the receiver will effectively switch as a result of the signal crossing the AC input level, and will remain in that state as long as the signal does not ring back above [below] the DC input LOW [HIGH] level).
6. Input slew rate = 1V/ns. If the slew rate exceeds the maximum specified by 20 percent, functionality is uncertain. If the slew rate exceeds the minimum specified, timing is no longer referenced to the mid-point but to the V$_{IL}$(AC) maximum and V$_{IH}$(AC) minimum points. For slew rates between 0.5V/ns and 1V/ns, ^{t}IS and ^{t}IH must be increased by at least 20 percent.
7. Inputs are not recognized as valid until V$_{REF}$ stabilizes. Exception: during the period before V$_{REF}$ stabilizes, CKE $\leq$ 0.3 x V$_{DDQ}$ is recognized as LOW.
8. The DC values define where the input slew rate requirements are imposed, and the input signal must not violate these levels in order to maintain a valid level. The inputs require the AC value to be achieved during signal transition edge.
9. V$_{ID}$ is the magnitude of the difference between the input level on CK and the input level on CK#.
10. The value of V$_{IX}$ is expected to equal V$_{DDQ}$/2 of the transmitting device and must track variations in the DC level of the same.

MICRON®
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I_{DD} SPECIFICATIONS AND CONDITIONS*

(Notes: 1-8; notes appear below and on next page) (0°C ≤ T_A ≤ +70°C; $V_{DD}Q$ = +2.5V ±0.2V, V_{DD} = +2.5V ±0.2V)

PARAMETER/CONDITION	SYMBOL	SIZE	MAX -262	MAX -265	MAX -202	UNITS	NOTES
OPERATING CURRENT: One bank; Active-Precharge; ^tRC = ^tRC MIN; ^tCK = ^tCK MIN; DQ, DM and DQS inputs changing twice per clock cyle; Address and control inputs changing once per clock cycle; CL = 2.5	I_{DD0}	64MB	1,040	1,000	960	mA	9
		128MB	1,560	1,480	1,440		
OPERATING CURRENT: One bank; Active-Read-Precharge; Burst = 2; ^tRC = ^tRC MIN; CL = 2.5; ^tCK = ^tCK MIN; I_{OUT} = 0mA; Address and control inputs changing once per clock cycle	I_{DD1}	64MB	840	800	800	mA	9
		128MB	1,360	1,280	1,280		
PRECHARGE POWER-DOWN STANDBY CURRENT: All banks idle; Power-down mode; CKE = LOW; ^tCK = ^tCK MIN	I_{DD2P}	64MB	280	240	240	mA	
		128MB	560	480	480		
IDLE STANDBY CURRENT: CS# = HIGH; All banks idle; CKE = HIGH; ^tCK = ^tCK MIN; Address and other control inputs changing once per clock cycle	I_{DD2N}	64MB	480	440	400	mA	
		128MB	960	880	800		
ACTIVE POWER-DOWN STANDBY CURRENT: One bank active; Power-down mode; CKE = LOW; ^tCK = ^tCK MIN	I_{DD3P}	64MB	280	240	240	mA	
		128MB	560	480	480		
ACTIVE STANDBY CURRENT: CS# = HIGH; CKE = HIGH; One bank; Active-Precharge; ^tRC = ^tRAS MAX; ^tCK = ^tCK MIN; DQ, DM and DQS inputs changing twice per clock cycle; Address and other control inputs changing once per clock cycle	I_{DD3N}	64MB	520	480	480	mA	9
		128MB	1,040	960	960		
OPERATING CURRENT: Burst = 2; Reads; Continuous burst; One bank active; Address and control inputs changing once per clock cycle; CL = 2.5; ^tCK = ^tCK MIN; I_{OUT} = 0mA	I_{DD4R}	64MB	1,040	1,000	920	mA	
		128MB	1,560	1,480	1,400		
OPERATING CURRENT: Burst = 2; Writes; Continuous burst; One bank active; Address and control inputs changing once per clock cycle; CL = 2.5; ^tCK = ^tCK MIN; DQ, DM and DQS inputs changing twice per clock cycle	I_{DD4W}	64MB	920	840	800	mA	
		128MB	1,440	1,320	1,280		
AUTO REFRESH CURRENT — ^tRC = ^tRFC MIN	I_{DD5}	64MB	1,240	1,160	1,120	mA	9
		128MB	2,480	2,320	2,240		
AUTO REFRESH CURRENT — ^tRC = 15.625μs	I_{DD6}	64MB	200	200	200	mA	10
		128MB	400	400	400		
SELF REFRESH CURRENT: CKE ≤ 0.2V — Standard	I_{DD7}	64MB	16	16	24	mA	11
		128MB	32	32	48		
SELF REFRESH CURRENT: CKE ≤ 0.2V — Low power (L)	I_{DD8}	64MB	8	8	8	mA	11
		128MB	16	16	16		

*Specifications based on 64Mb DDR SDRAM components.

NOTE:
1. All voltages referenced to V_{SS}.
2. Tests for AC timing, I_{DD}, and electrical AC and DC characteristics may be conducted at nominal reference/supply voltage levels, but the related specifications and device operation are guaranteed for the full voltage range specified.

NOTES: (continued)

3. Outputs measured with equivalent load:

4. AC timing and I_{DD} tests may use a V_{IL}-to-V_{IH} swing of up to 1.5V in the test environment, but input timing is still referenced to V_{REF} (or to the crossing point for CK/CK#), and parameter specifications are guaranteed for the specified AC input levels under normal use conditions. The minimum slew rate for the input signals used to test the device is 1V/ns in the range between V_{IL}(AC) and V_{IH}(AC).

5. The AC and DC input level specifications are as defined in the SSTL_2 Standard (i.e., the receiver will effectively switch as a result of the signal crossing the AC input level, and will remain in that state as long as the signal does not ring back above [below] the DC input LOW [HIGH] level).

6. I_{DD} is dependent on output loading and cycle rates. Specified values are obtained with minimum cycle time and the outputs open.

7. I_{DD} specifications are tested after the device is properly initialized.

8. Input slew rate = 1V/ns. If the slew rate exceeds the maximum specified by 20 percent, functionality is uncertain. If the slew rate exceeds the minimum specified, timing is no longer referenced to the mid-point but to the V_{IL}(AC) maximum and V_{IH}(AC) minimum points. For slew rates between 0.5V/ns and 1V/ns, ^{t}IS and ^{t}IH must be increased by at least 20 percent.

9. MIN (^{t}RC or ^{t}RFC) for I_{DD} measurements is the smallest multiple of ^{t}CK that meets the minimum absolute value for the respective parameter. ^{t}RAS MAX for I_{DD} measurements is the largest multiple of ^{t}CK that meets the maximum absolute value for ^{t}RAS.

10. This limit is actually a nominal value and does not result in a fail value. CKE is HIGH during REFRESH command period (^{t}RFC [MIN]) else CKE is LOW (i.e., during standby).

11. Enables on-chip refresh and address counters.

SDRAM DDR COMPONENT* AC ELECTRICAL CHARACTERISTICS

(Notes: 1-9; notes appear below an don next page) (0°C ≤ T_A ≤ +70°C; V_{DDQ} = +2.5V ±0.2V, V_{DD} = +2.5V ±0.2V)

AC CHARACTERISTICS			-262		-265		-202			
PARAMETER		SYMBOL	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
Access window of DQs from CK/CK#		^tAC	-0.75	+0.75	-0.75	+0.75	-0.8	+0.8	ns	
CK high-level width		^tCH	0.45	0.55	0.45	0.55	0.45	0.55	^tCK	
CK low-level width		^tCL	0.45	0.55	0.45	0.55	0.45	0.55	^tCK	
Clock cycle time	CL = 2.5	^tCK	7	15	7.5	15	8	15	ns	
	CL = 2	^tCK	7.5	15	10	15	10	15	ns	
Auto precharge write recovery plus precharge time		^tDAL	35		35		35		ns	
DQ and DM input hold time		^tDH	0.5		0.5		0.6		ns	
DQ and DM input setup time		^tDS	0.5		0.5		0.6		ns	
DQ and DM input pulse width (for each input)		^tDIPW	1.75		1.75		2		ns	
Access window of DQS from CK/CK#		^tDQSCK	-0.75	+0.75	-0.75	+0.75	-0.8	+0.8	ns	
DQS input high pulse width		^tDQSH	0.35		0.35		0.35		^tCK	
DQS input low pulse width		^tDQSL	0.35		0.35		0.35		^tCK	
DQS-DQ-DQ skew (first to last transition per access)		^tDQSQ		0.5		0.5		0.6	ns	
Write command to first DQS latching transition		^tDQSS	0.75	1.25	0.75	1.25	0.75	1.25	^tCK	
DQS falling edge to CK rising - setup time		^tDSS	0.2		0.2		0.2		^tCK	
DQS falling edge from CK rising - hold time		^tDSH	0.2		0.2		0.2		^tCK	
DQ/DQS output valid window		^tDV	0.35		0.35		0.35		^tCK	10
Data-out high-impedance window from CK/CK#		^tHZ	-0.75	+0.75	-0.75	+0.75	-0.8	+0.8	ns	11
Data-out low-impedance window from CK/CK#		^tLZ	-0.75	+0.75	-0.75	+0.75	-0.8	+0.8	ns	11
Address and control input hold time		^tIH	0.75		0.75		1.1		ns	12
Address and control input setup time		^tIS	0.75		0.75		1.1		ns	12
Address and control input pulse width		^tIPW	2		2		2.5		ns	
LOAD MODE REGISTER command cycle time		^tMRD	15		15		16		ns	
ACTIVE to PRECHARGE command		^tRAS	45	120,000	45	120,000	50	120,000	ns	
ACTIVE to ACTIVE/AUTO REFRESH command period		^tRC	65		65		70		ns	
AUTO REFRESH to ACTIVE/ AUTO REFRESH command period		^tRFC	75		75		80		ns	
REFRESH to REFRESH command interval		^tREFC		31.2		31.2		31.2	μs	13
Average periodic refresh interval		^tREFI		15.6		15.6		15.6	μs	13
ACTIVE to READ or WRITE delay		^tRCD	20		20		20		ns	
PRECHARGE command period		^tRP	20		20		20		ns	
Read preamble		^tRPRE	0.9	1.1	0.9	1.1	0.9	1.1	^tCK	
Read postamble		^tRPST	0.4	0.6	0.4	0.6	0.4	0.6	^tCK	
ACTIVE bank a to ACTIVE bank b command		^tRRD	15		15		15		ns	
Terminating voltage delay to V_{DD}		^tVTD	0		0		0		ns	
DQS Write preamble		^tWPRE	0.25		0.25		0.25		^tCK	
DQS Write preamble setup time		^tWPRES	0		0		0		ns	14, 15
DQS Write postamble		^tWPST	0.4	0.6	0.4	0.6	0.4	0.6	^tCK	16
DQS Write recovery time		^tWR	15		15		15		ns	
Internal WRITE to READ command delay		^tWTR	1		1		1		^tCK	
Exit SELF REFRESH to non-READ command		^tXSNR	75		75		80		ns	
Exit SELF REFRESH to READ command		^tXSRD	200		200		200		^tCK	

*Specifications for the DDR SDRAM components used on the module.

NOTE: 1. All voltages referenced to V_{SS}.
 2. Tests for AC timing, I_{DD}, and electrical AC and DC characteristics may be conducted at nominal reference/supply voltage levels, but the related specifications and device operation are guaranteed for the full voltage range specified.

NOTES: (continued)

3. Outputs measured with equivalent load:

4. AC timing and I_{DD} tests may use a V_{IL}-to-V_{IH} swing of up to 1.5V in the test environment, but input timing is still referenced to V_{REF} (or to the crossing point for CK/CK#), and parameter specifications are guaranteed for the specified AC input levels under normal use conditions. The minimum slew rate for the input signals used to test the device is 1V/ns in the range between $V_{IL}(AC)$ and $V_{IH}(AC)$.

5. The AC and DC input level specifications are as defined in the SSTL_2 Standard (i.e., the receiver will effectively switch as a result of the signal crossing the AC input level, and will remain in that state as long as the signal does not ring back above [below] the DC input LOW [HIGH] level).

6. Input slew rate = 1V/ns. If the slew rate exceeds the maximum specified by 20 percent, functionality is uncertain. If the slew rate exceeds the minimum specified, timing is no longer referenced to the mid-point but to the $V_{IL}(AC)$ maximum and $V_{IH}(AC)$ minimum points. For slew rates between 0.5V/ns and 1V/ns, ^{t}IS and ^{t}IH must be increased by at least 20 percent.

7. The CK/CK# input reference level (for timing referenced to CK/CK#) is the point at which CK and CK# cross; the input reference level for signals other than CK/CK# is V_{REF}.

8. Inputs are not recognized as valid until V_{REF} stabilizes. Exception: during the period before V_{REF} stabilizes, CKE ≤ 0.3 x $V_{DD}Q$ is recognized as LOW.

9. The output timing reference level, as measured at the timing reference point indicated in Note 3, is V_{TT}.

10. ^{t}DV is derived assuming a 45/55 clock HIGH-to-LOW ratio. The ^{t}DV is improved directly proportional to the reduction in the clock HIGH-to-LOW ratio.

11. ^{t}HZ and ^{t}LZ transitions occur in the same access time windows as valid data transitions. These parameters are not referenced to a specific voltage level, but specify when the device output is no longer driving (HZ) or begins driving (LZ).

12. Input slew rate = 1V/ns. If the slew rate exceeds the maximum specified by 20 percent, functionality is uncertain. If the slew rate exceeds the minimum specified, timing is no longer referenced to the mid-point but to the $V_{IL}(AC)$ maximum and $V_{IH}(AC)$ minimum points. For slew rates between 0.5V/ns and 1V/ns, ^{t}IS and ^{t}IH must be increased by at least 20 percent.

13. The refresh period 64ms. This equates to an average refresh rate of 15.625μs. However, an AUTO REFRESH command must be asserted at least once every 31.2μs; burst refreshing or postings greater than 2 are not allowed.

14. The minimum limit for this parameter is not a device limit. The device will operate with a negative value for this parameter, but system performance (bus turnaround) will degrade accordingly.

15. The specific requirement is that DQS be valid (HIGH or LOW) on or before this CK edge. The case shown (DQS going from High-Z to logic LOW) applies when no WRITEs were previously in progress on the bus. If a previous WRITE was in progress, DQS could be HIGH at this time, depending on $^{t}DQSS$.

16. The maximum limit for this parameter is not a device limit. The device will operate with a greater value for this parameter, but system performance (bus turnaround) will degrade accordingly.

CAPACITANCE

(Note: 1)

PARAMETER	SYMBOL	64MB		128MB		UNITS
		MIN	MAX	MIN	MAX	
Input/Output Capacitance: DQs, DQSs, CBs	C_{IO}	5.0	7.0	10.0	14.0	pF
Input Capacitance: CK, CK#	C_{i1}	9	12	18	24	pF
Input Capacitance: A0-A11, BA0/1, RAS#, CAS#, WE#	C_{i2}	22	30	44	60	pF
Input Capacitance: S0#, S1#, CKE0, CKE1	C_{i3}	22	30	22	30	pF

NOTE: 1. This parameter is sampled. V_{DD} = +2.5V ±0.2V, $V_{DD}Q$ = +2.5V ±0.2V, f = 100 MHz, T_A = 25°C, $V_{OUT}(DC)$ = $V_{DD}Q/2$, V_{OUT} (peak to peak) = 0.2V. DM input is grouped with I/O pins, reflecting the fact that they are matched in loading.

SERIAL PRESENCE-DETECT EEPROM DC OPERATING CONDITIONS

(Note: 1) (V_{DD} = +3.3V ±0.3V)

| PARAMETER/CONDITION	SYMBOL	MIN	MAX	UNITS	NOTES
SUPPLY VOLTAGE	V_{DD}	3	3.6	V	
INPUT HIGH VOLTAGE: Logic 1; All inputs	V_{IH}	V_{DD} x 0.7	V_{DD} + 0.5	V	
INPUT LOW VOLTAGE: Logic 0; All inputs	V_{IL}	-1	V_{DD} x 0.3	V	
OUTPUT LOW VOLTAGE: I_{OUT} = 3mA	V_{OL}	–	0.4	V	
INPUT LEAKAGE CURRENT: V_{IN} = GND to V_{DD}	I_{LI}	–	10	µA	
OUTPUT LEAKAGE CURRENT: V_{OUT} = GND to V_{DD}	I_{LO}	–	10	µA	
STANDBY CURRENT: SCL = SDA = V_{DD} - 0.3V; All other inputs = GND or 3.3V +10%	I_{SB}	–	30	µA	
POWER SUPPLY CURRENT: SCL clock frequency = 100 KHz	I_{CC}	–	2	mA	

NOTE: 1. All voltages referenced to V_{SS}.

SERIAL PRESENCE-DETECT EEPROM AC OPERATING CONDITIONS

(Note: 1) (V_{DD} = +3.3V ±0.3V)

PARAMETER/CONDITION	SYMBOL	MIN	MAX	UNITS	NOTES
SCL LOW to SDA data-out valid	^tAA	0.3	3.5	µs	
Time the bus must be free before a new transition can start	^tBUF	4.7		µs	
Data-out hold time	^tDH	300		ns	
SDA and SCL fall time	^tF		300	ns	
Data-in hold time	$^tHD:DAT$	0		µs	
Start condition hold time	$^tHD:STA$	4		µs	
Clock HIGH period	^tHIGH	4		µs	
Noise suppression time constant at SCL, SDA inputs	^tI		100	ns	
Clock LOW period	^tLOW	4.7		µs	
SDA and SCL rise time	^tR		1	µs	
SCL clock frequency	^tSCL		100	KHz	
Data-in setup time	$^tSU:DAT$	250		ns	
Start condition setup time	$^tSU:STA$	4.7		µs	
Stop condition setup time	$^tSU:STO$	4.7		µs	
WRITE cycle time	^tWRC		10	ms	2

NOTE: 1. All voltages referenced to V_{SS}.
2. The SPD EEPROM WRITE cycle time (^tWRC) is the time from a valid stop condition of a WRITE sequence to the end of the EEPROM internal erase/program cycle. During the WRITE cycle, the EEPROM bus interface circuit is disabled, SDA remains HIGH due to pull-up resistor, and the EEPROM does not respond to its slave address.
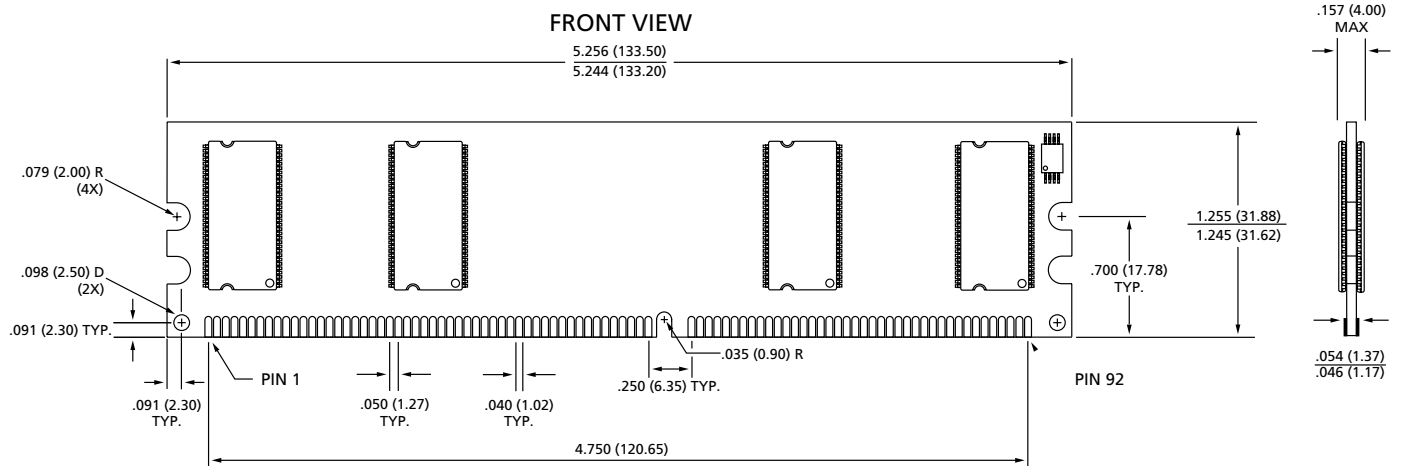
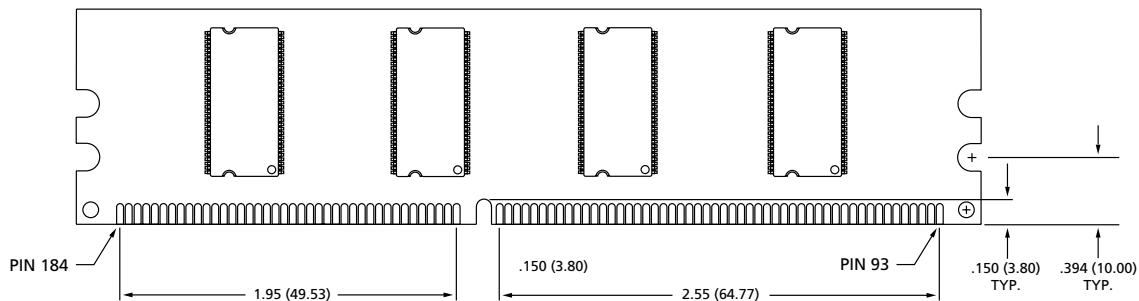## SPD EEPROM

UNDEFINED
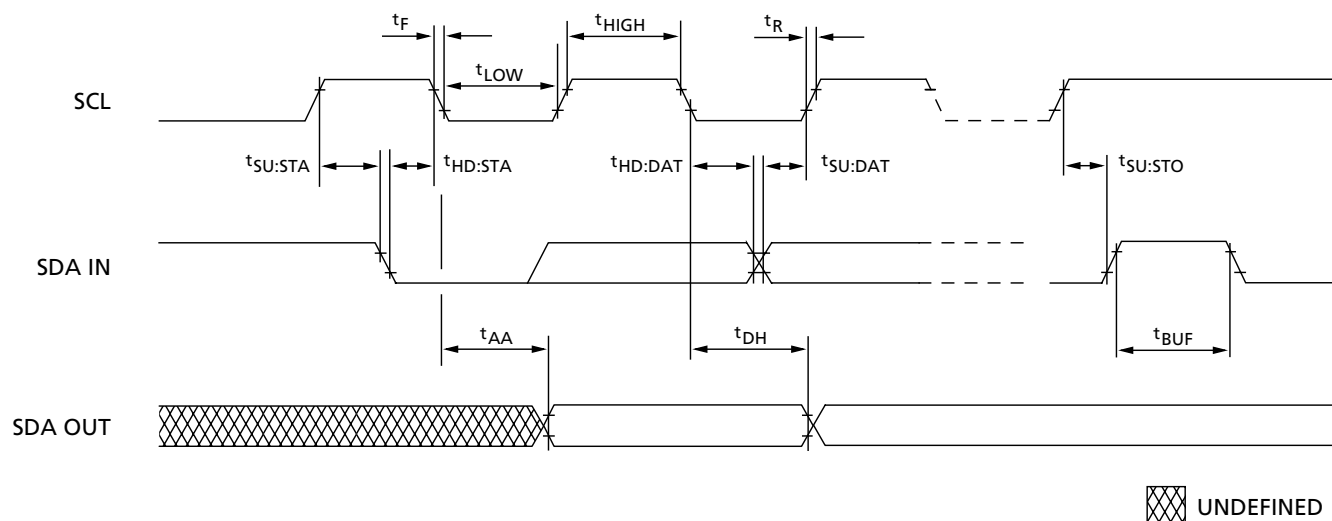
SERIAL PRESENCE-DETECT EEPROM
TIMING PARAMETERS

SYMBOL	MIN	MAX	UNITS
t_{AA}	0.3	3.5	µs
t_{BUF}	4.7		µs
t_{DH}	300		ns
t_F		300	ns
$t_{HD:DAT}$	0		µs
$t_{HD:STA}$	4		µs

SYMBOL	MIN	MAX	UNITS
t_{HIGH}	4		µs
t_{LOW}	4.7		µs
t_R		1	µs
$t_{SU:DAT}$	250		ns
$t_{SU:STA}$	4.7		µs
$t_{SU:STO}$	4.7		µs

MICRON®
SEMICONDUCTOR PRODUCTS, INC.

184-PIN DIMM
(128MB)

FRONT VIEW

.157 (4.00)
MAX

5.256 (133.50)
5.244 (133.20)

.079 (2.00) R
(4X)

.098 (2.50) D
(2X)

.091 (2.30) TYP.

1.255 (31.88)
1.245 (31.62)

.700 (17.78)
TYP.

PIN 1

.035 (0.90) R

PIN 92

.091 (2.30)
TYP.

.050 (1.27)
TYP.

.040 (1.02)
TYP.

.250 (6.35) TYP.

.054 (1.37)
.046 (1.17)

4.750 (120.65)

BACK VIEW

PIN 184

PIN 93

.150 (3.80)

.150 (3.80)
TYP.

.394 (10.00)
TYP.

1.95 (49.53)

2.55 (64.77)

NOTE: All dimensions in inches (millimeters) $\frac{MAX}{MIN}$ or typical where noted.

184-PIN DIMM
(256MB)

FRONT VIEW
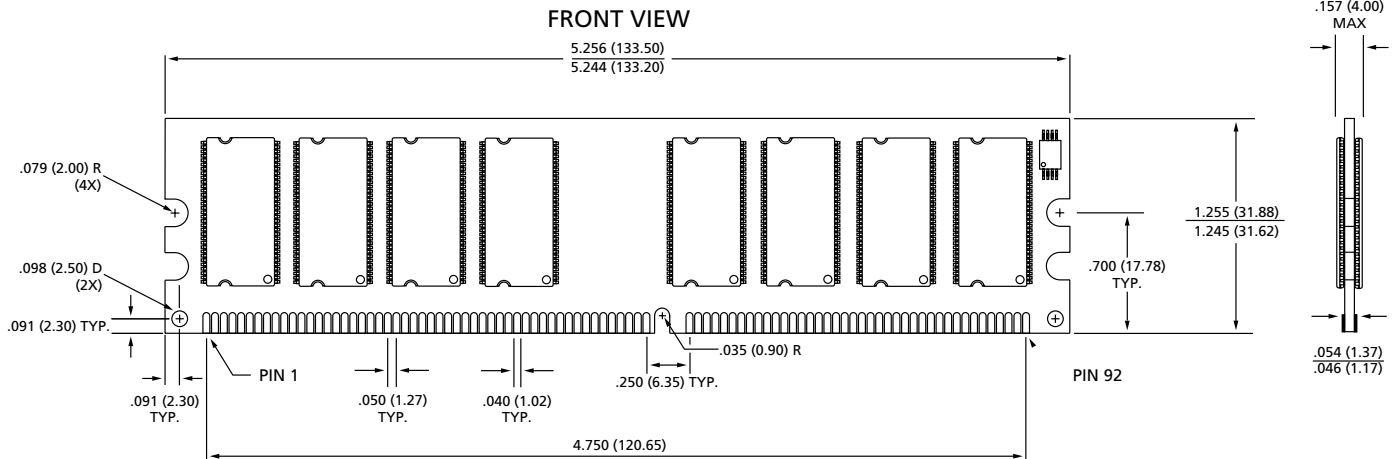
BACK VIEW

NOTE: All dimensions in inches (millimeters) $\frac{MAX}{MIN}$ or typical where noted.