



QUAD TVS/ZENER ARRAY FOR ESD AND LATCH-UP PROTECTION

This Quad TVS/Zener Array family have been designed to Protect Sensitive Equipment against ESD and to prevent Latch-Up events in CMOS circuitry operating at 5V, 12V, 15V and 24V. This TVS array offers an integrated solution to protect up to 4 data lines where the board space is a premium.

SPECIFICATION FEATURES

- 350W Power Dissipation (8/20µs Waveform)
- Low Leakage Current, Maximum of 5µA at rated voltage
- Very Low Clamping Voltage
- IEC61000-4-2 ESD 20kV air, 15kV Contact Compliance
- Industry Standard Surface Mount Package SOT23-6L
- 100% Tin Matte Finish (RoHS Compliance)

APPLICATIONS

- Personal Digital Assistant (PDA)
- SIM Card Port Protection (Mobile Phone)
- Portable Instrumentation
- Mobile Phones and Accessories
- Memory Card Port Protection

TVS Marking Code PJSMS05 M05 PJSMS12 M12 PJSMS15 M15 PJSMS24 M24

2

SOT23-6L

3

MAXIMUM RATINGS (Per Device)

Rating	Symbol	Value	Units
Peak Pulse Power (8/20µs Waveform)	P _{pp}	350	W
ESD Voltage (HBM)	V _{ESD}	>25	kV
Operating Temperature Range	ТЈ	-50 to +125	°C
Storage Temperature Range	T _{stg}	-50 to +150	°C

ELECTRICAL CHARACTERISTICS (Per Device) $T_j = 25^{\circ}C$ PJSMS05

Parameter	Symbol	Conditions	Min	Typical	Max	Units
Reverse Stand-Off Voltage	V_{WRM}				5	V
Reverse Breakdown Voltage	V_{BR}	I _{BR} = 1mA	6			V
Reverse Leakage Current	I _R	V _R =5V			5	μΑ
Clamping Voltage (8/20µs)	Vc	I _{pp} =5A			9.8	V
Clamping Voltage (8/20µs)	V _c	I _{pp} = 24A			13	V
Off State Junction Capacitance	Cj	0 Vdc Bias f = 1MHz Between I/O pins and pin 2, 5			225	pF
Off State Junction Capacitance	Cj	5 Vdc Bias f = 1MHz Between I/O pins and pin 2, 5			125	pF





ELECTRICAL CHARACTERISTICS (Per Device) Tj = 25°C

PJSMS12

Parameter	Symbol	Conditions	Min	Typical	Max	Units
Reverse Stand-Off Voltage	V_{WRM}				12	V
Reverse Breakdown Voltage	V_{BR}	I _{BR} =1mA	13.3			V
Reverse Leakage Current	I _R	V _R =12V			1	μΑ
Clamping Voltage (8/20µs)	Vc	I _{pp} =5A			20	V
Clamping Voltage (8/20µs)	V _c	I _{pp} = 15A			25	V
Off State Junction Capacitance	Cj	0 Vdc Bias f = 1MHz Between I/O pins and pin 2, 5			100	pF

PJSMS15

Parameter	Symbol	Conditions	Min	Typical	Max	Units
Reverse Stand-Off Voltage	V_{WRM}				15	V
Reverse Breakdown Voltage	V_{BR}	I _{BR} =1mA	16.7			V
Reverse Leakage Current	Ι _R	V _R = 15V			1	μΑ
Clamping Voltage (8/20µs)	V _c	I _{pp} =5A			24	V
Clamping Voltage (8/20µs)	V _c	I _{pp} = 12A			29	V
Off State Junction Capacitance	Cj	0 Vdc Bias f = 1MHz Between I/O pins and pin 2, 5			80	pF

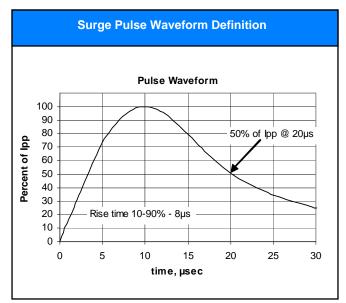
PJSMS24

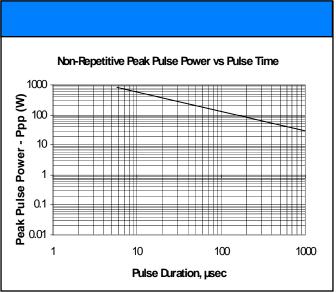
Parameter	Symbol	Conditions	Min	Typical	Max	Units
Reverse Stand-Off Voltage	V_{WRM}				24	V
Reverse Breakdown Voltage	V_{BR}	I _{BR} =1mA	26.7			V
Reverse Leakage Current	I _R	V _R =24V			1	μΑ
Clamping Voltage (8/20µs)	Vc	I _{pp} =5A			40	V
Clamping Voltage (8/20µs)	V _c	I _{pp} = 8A			44	V
Off State Junction Capacitance	Cj	0 Vdc Bias f = 1MHz Between I/O pins and pin 2, 5			60	pF

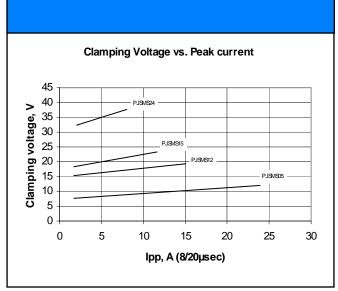


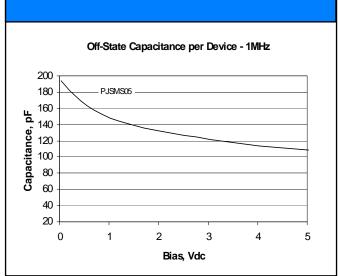


TYPICAL CHARACTERISTICS TJ = 25°C unless otherwise noted





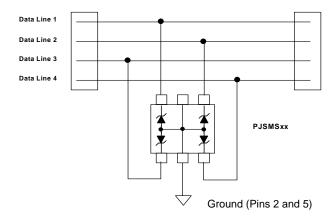


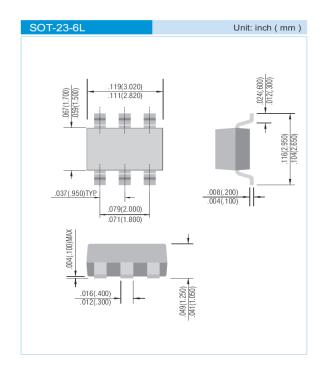


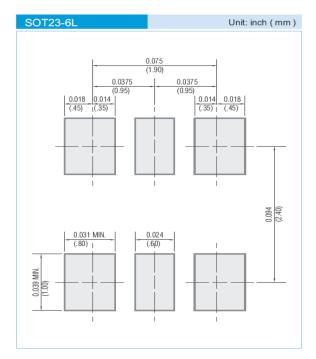




TYPICAL APPLICATION EXAMPLE AND PACKAGE DIMENSIONS







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