QL2020L
20,000 Gate pASIC® 2 FPGA
Low Power 3.3 Volt Operation

ADVANCED DATA

pASIC 2 HIGHLIGHTS

Low Power 3.3V Operation, 5V Tolerant

-3.0 to 3.6 volt supply operation; ultra low standby power
-Supports interface to 5V CMOS, NMOS
-Fully pin-out and function compatible with the high speed 5.0V product

High Speed, High Density

... 20,000 usable gates, 336 I/O pins

-Datapath speeds exceeding 120 MHz
-20,000 to 25,500 usable gates, 336 I/Os

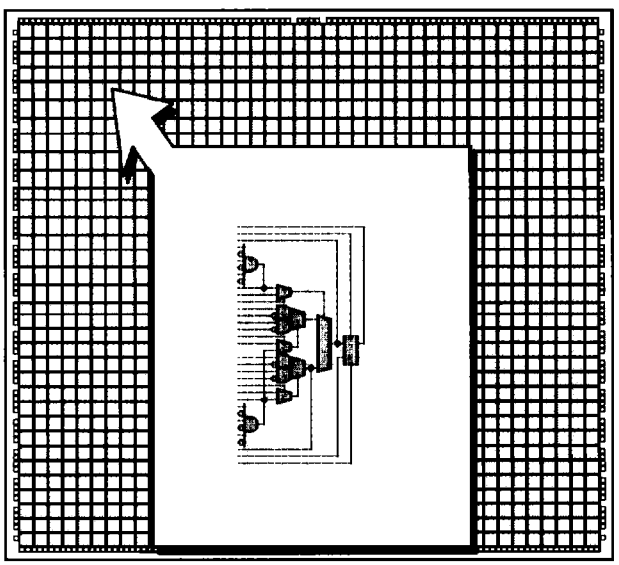
Advanced Logic Cell and I/O Capabilities

-Complex functions (up to 16 inputs) in a single logic cell
-High synthesis gate utilization from logic cell fragments
-Full IEEE Standard 1149.1a JTAG boundary scan capability
-Individually-controlled input/feedback registers and OEs on all I/O pins

Other Important Family Features

-I/O pin-compatibility between different devices in the same packages
-PCI compliant versions
-High design security provided by security fuses

QL2020 Block Diagram



1440 Logic Cells

QUICKLOGIC