

# S98WS064RB0HI001, -002

## Stacked Multi-Chip Product (MCP)

64 Megabit (4 M x 16-Bit), 1.8 Volt-only Simultaneous Read/Write,  
Burst Mode Flash Memory with  
32 Megabit (2M x 16-Bit) CellularRAM

*Data Sheet (Advance Information)*

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## Features

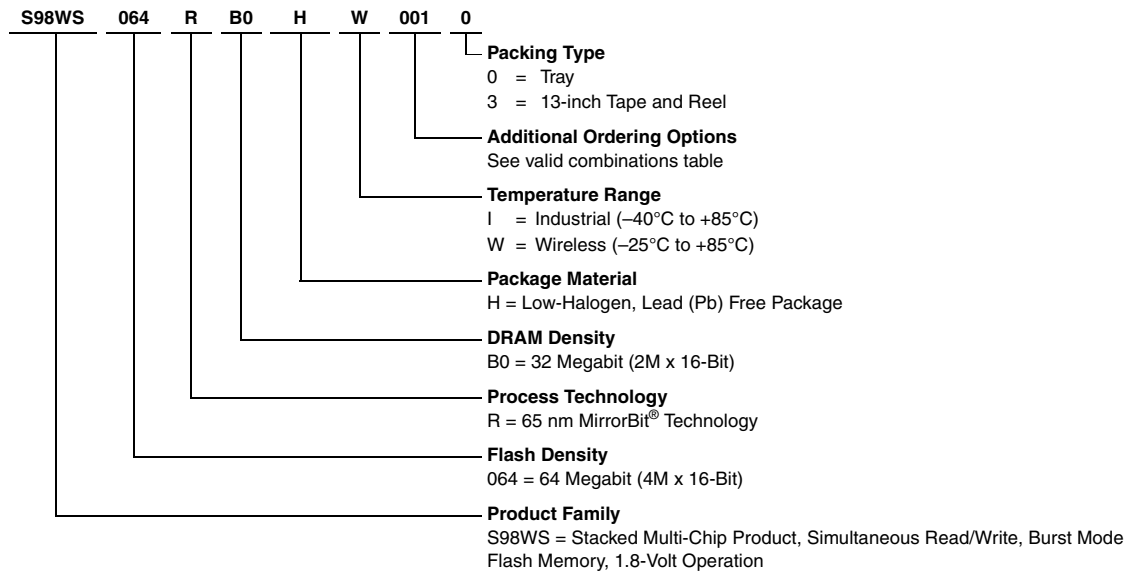
- **Single 1.8 volt read, program and erase (1.7 to 1.95 volt)**
- **Simultaneous Read/Write operation**
  - Data can be continuously read from one bank while executing erase/program functions in other bank
  - Zero latency between read and write operations
- **Package**
  - 88-ball Thin Fine pitch BGA
  - 10.0 x 8.0 x 1.2 mm
- **Speed**
  - Flash and CellularRAM: 108 MHz
- **Page Mode Read Access**
  - Flash: 8-word page with page access time of 20 ns
  - CellularRAM: 16-word page with page access time of 20 ns

For detailed specifications, please refer to the individual data sheets:

Document	Publication Identification Number (PID)
S29WS064R	S29WS064R_00
32 Mb Async/Page/Burst CellularRAM	SWM032D133S3R

# 1. Ordering Information

The order number is formed by a valid combination of the following:



## 1.1 Valid Combinations

The following configurations are planned to be supported for this device. Consult the local sales office to confirm availability of specific valid combinations and to check on newly released combinations.

**Table 1.1** Valid Combinations

Product Family	Flash Density	Process Technology	DRAM Density	Package Material / Temperature Range	Model Number	Packing Type
S98WS	064	R	B0	HI, HW	001, 002	0, 3

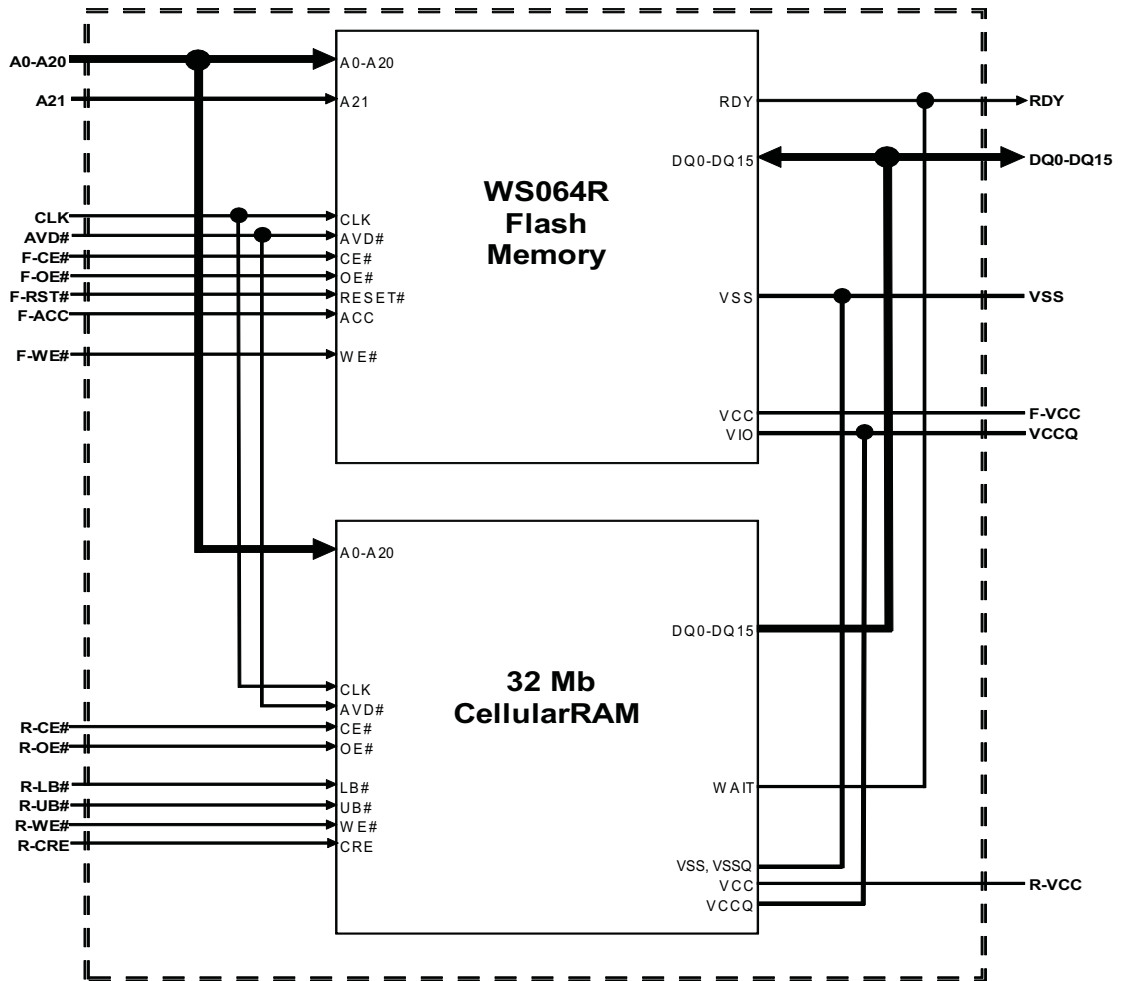
**Note:**

BGA package marking omits leading S and packing type designator from ordering part number.

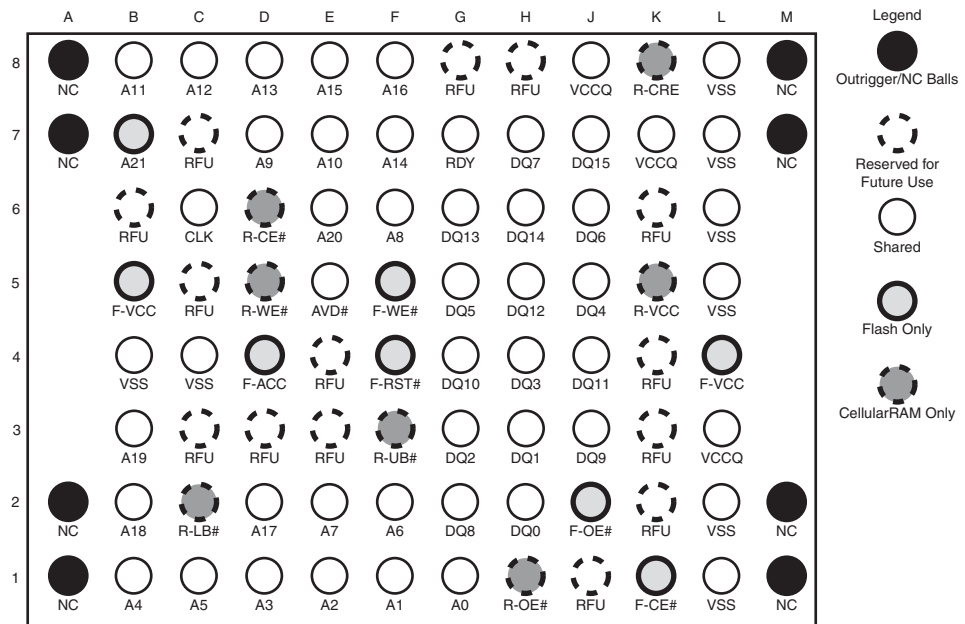
# 2. Product Selector Guide

Part#	S98WS064RB0HW001x/ S98WS064RB0HI001x	S98WS064RB0HW002x/ S98WS064RB0HI002x
Flash Burst Frequency	108 MHz	108 MHz
CellularRAM Frequency	108 MHz	108 MHz
DYB	Unlocked	Unlocked
Factory Secured Silicon Region	Locked	Locked
Customer Secured Silicon Region	Unlocked	Unlocked
Boot option	Top Boot	Bottom Boot

### 3. MCP Block Diagram



### 4. Connection Diagram

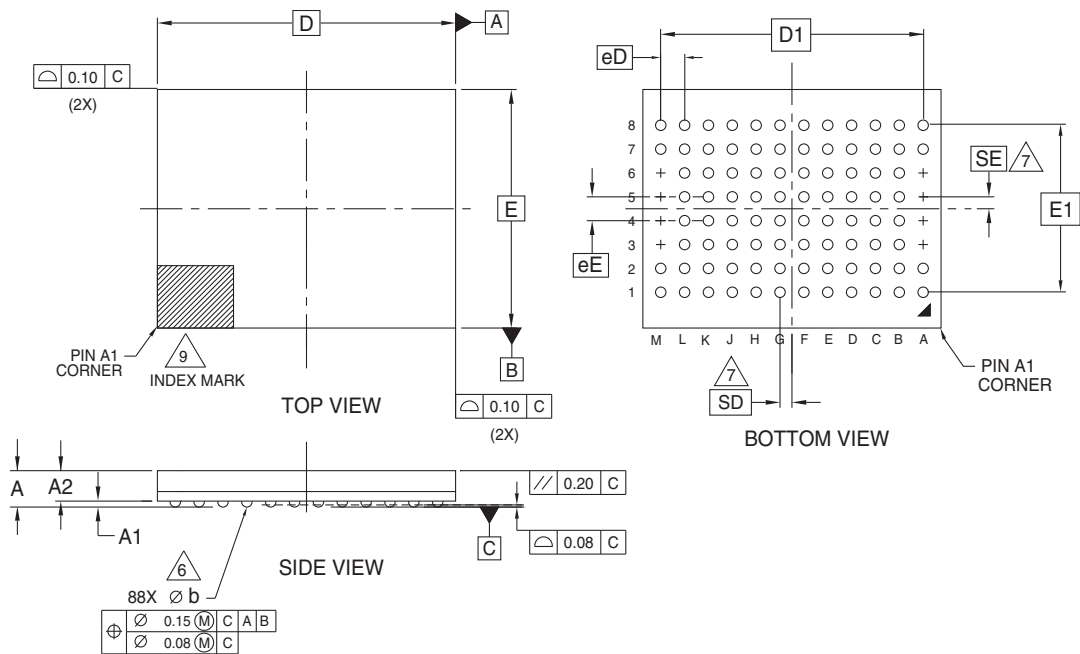


## 5. Input/Output Descriptions

Signal	Description	Flash	CellularRAM
A21	NOR Flash only Address inputs	X	
A20-A0	NOR Flash/CellularRAM Address inputs	X	X
DQ15-DQ0	Flash Data input/output, shared between NOR and CellularRAM	X	X
F-CE#	NOR Flash Chip-enable input #1. Asynchronous relative to CLK for Burst Mode	X	
F-OE#	NOR Output Enable input. Asynchronous relative to CLK for Burst mode	X	
F-WE#	NOR Write Enable input	X	
F-V <sub>CC</sub>	NOR Flash device power supply (1.7V - 1.95V)	X	
V <sub>CCQ</sub>	Input/Output Buffer power supply	X	X
V <sub>SS</sub>	Ground	X	X
RDY	Flash ready output. Indicates the status of the Burst read. V <sub>OL</sub> = data valid. The Flash RDY pin is shared with the WAIT pin of the CellularRAM.	X	X
CLK	NOR Flash Clock, shared with CLK of burst-mode CellularRAM. The first rising edge of CLK in conjunction with AVD# low latches the address input and activates burst mode operation. After the initial word is output, subsequent rising edges of CLK increment the internal address counter. CLK should remain low during asynchronous access.	X	X
AVD#	NOR Flash Address Valid input. Shared with AVD# of burst-mode CellularRAM. Indicates to device that the valid address is present on the address inputs. V <sub>IL</sub> = for asynchronous mode, indicates valid address; for burst mode, causes starting address to be latched on rising edge of CLK. V <sub>IH</sub> = device ignores address inputs.	X	X
F-RST#	NOR Flash hardware reset input. V <sub>IL</sub> = device resets and returns to reading array data	X	
F-ACC	NOR Flash accelerated input. At V <sub>IH</sub> , accelerates programming; automatically places device in unlock bypass mode. At V <sub>IL</sub> , disables all program and erase functions. Should be at V <sub>IH</sub> for all other conditions.	X	
R-CE#	Chip-enable input for CellularRAM		X
R-OE#	CellularRAM Output Enable input. Asynchronous relative to CLK for Burst mode		X
R-WE#	CellularRAM Write Enable input		X
R-CRE	Control Register Enable (CellularRAM). For CellularRAM only.		X
R-V <sub>CC</sub>	CellularRAM Power Supply		X
R-UB#	Upper Byte Control (CellularRAM)		X
R-LB#	Lower Byte Control (CellularRAM)		X
NC	Not Connected. No device internal signal is connected to the package connector nor is there any future plan to use the connector for a signal. The connection may safely be used for routing space for a signal on a Printed Circuit Board (PCB).		
DNU	Do Not Use. A device internal signal may be connected to the package connector. The connection may be used by Spansion for test or other purposes and is not intended for connection to any host system signal. Any DNU signal related function will be inactive when the signal is at V <sub>IL</sub> . The signal has an internal pull-down resistor and may be left unconnected in the host system or may be tied to V <sub>SS</sub> . Do not use these connections for PCB signal routing channels. Do not connect any host system signal to these connections.		
RFU	Reserved for Future Use. No device internal signal is currently connected to the package connector but there is potential future use for the connector for a signal. It is recommended to not use RFU connectors for PCB routing channels so that the PCB may take advantage of future enhanced features in compatible footprint devices.		

## 6. Physical Dimensions

### TSE088—88-Ball Thin Fine Pitch Ball Grid Array (FBGA) 10 x 8 mm Package



PACKAGE	TSE 088			
JEDEC	N/A			
D x E	10.00 mm x 8.00 mm PACKAGE			
SYMBOL	MIN	NOM	MAX	NOTE
A	---	---	1.20	PROFILE
A1	0.20	---	---	BALL HEIGHT
A2	0.82	---	0.90	BODY THICKNESS
D	10.00 BSC.			BODY SIZE
E	8.00 BSC.			BODY SIZE
D1	8.80 BSC.			MATRIX FOOTPRINT
E1	5.60 BSC.			MATRIX FOOTPRINT
MD	12			MATRIX SIZE D DIRECTION
ME	8			MATRIX SIZE E DIRECTION
n	88			BALL COUNT
Øb	0.33	---	0.43	BALL DIAMETER
eE	0.80 BSC.			BALL PITCH
eD	0.80 BSC.			BALL PITCH
SD / SE	0.40 BSC.			SOLDER BALL PLACEMENT
	A3,A4,A5,A6,M3,M4,M5,M6			DEPOPULATED SOLDER BALLS

NOTES:

- DIMENSIONING AND TOLERANCING METHODS PER ASME Y14.5M-1994.
- ALL DIMENSIONS ARE IN MILLIMETERS.
- BALL POSITION DESIGNATION PER JEP95, SECTION 4.3, SPP-010.
- $\boxed{e}$  REPRESENTS THE SOLDER BALL GRID PITCH.
- SYMBOL "MD" IS THE BALL MATRIX SIZE IN THE "D" DIRECTION.

SYMBOL "ME" IS THE BALL MATRIX SIZE IN THE "E" DIRECTION.

n IS THE NUMBER OF POPULATED SOLDER BALL POSITIONS FOR MATRIX SIZE MD X ME.

$\triangle 6$  DIMENSION "b" IS MEASURED AT THE MAXIMUM BALL DIAMETER IN A PLANE PARALLEL TO DATUM C.

$\triangle 7$  SD AND SE ARE MEASURED WITH RESPECT TO DATUMS A AND B AND DEFINE THE POSITION OF THE CENTER SOLDER BALL IN THE OUTER ROW.

WHEN THERE IS AN ODD NUMBER OF SOLDER BALLS IN THE OUTER ROW SD OR SE = 0.000.

WHEN THERE IS AN EVEN NUMBER OF SOLDER BALLS IN THE OUTER ROW, SD OR SE =  $\frac{eD}{2}$

- "+" INDICATES THE THEORETICAL CENTER OF DEPOPULATED BALLS.

$\triangle 9$  A1 CORNER TO BE IDENTIFIED BY CHAMFER, LASER OR INK MARK, METALLIZED MARK INDENTATION OR OTHER MEANS.

- OUTLINE AND DIMENSIONS PER CUSTOMER REQUIREMENT.

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## 7. Revision History

Section	Description
Revision 01 (August 20, 2010)	
	Initial release

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