GEC PLESSEY
SEMICONDUCTORS

SP8634 SP8635 SP8637

700/600/400MHz ÷ 10 (BCD OUTPUTS)

The SP8634/5 and 7 are ECL decade counters with TTL compatible BCD outputs. They require an AC coupled input of 600mV p-p and have an ECL 10K compatible inhibit input which inhibits the device when in the high state. Both ECL and TTL 'carry' outputs are provided and there is a TTL reset.

FEATURES

- BCD Outputs TTL Compatible
- Reset Input TTL Compatible
- AC Coupled Input (Internal Bias)
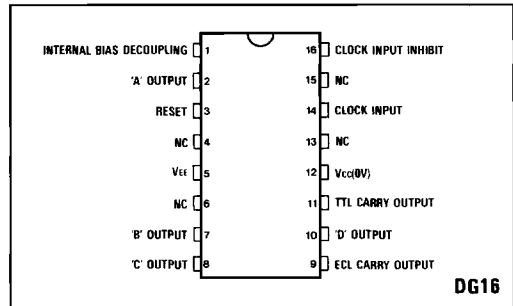- TTL and ECL Compatible Carry Outputs
- Clock Inhibit Input ECL Compatible

Fig.1 Pin connections - top view

QUICK REFERENCE DATA

- Supply Voltage: 5.2V
- Power Consumption: 400mW
- Temperature Range: 0°C to +70°C

ABSOLUTE MAXIMUM RATINGS

Supply voltage	−8V
BCD outputs voltage	V_{EE} +11V
Storage temperature range	−55°C to +150°C
Max. junction temperature	+175°C
Max. clock I/P voltage	2.5V p-p

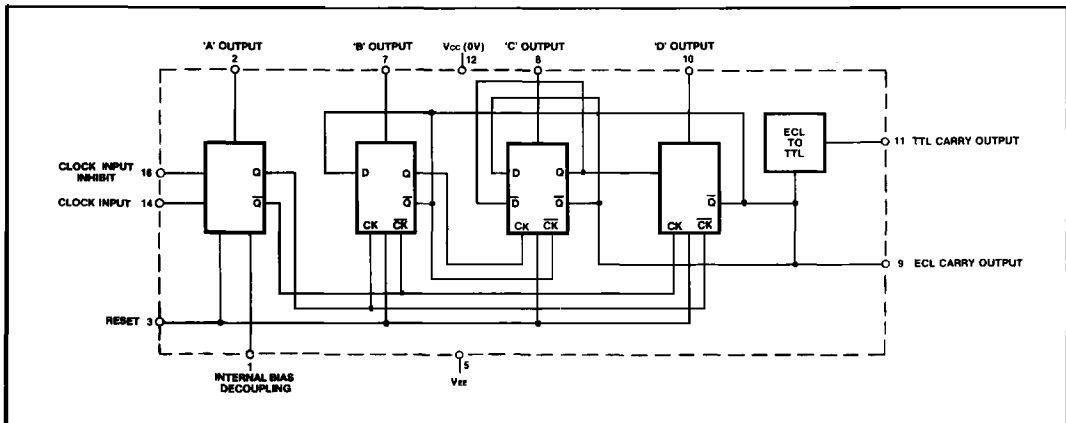## ORDERING INFORMATION

SP8634 B DG
**SP8635 B DG**
SP8637 B DG

Fig.2 Functional diagram

ELECTRICAL CHARACTERISTICS

Supply Voltage: $V_{CC} = 0V$ $V_{EE} = -5.2V \pm 0.25V$
Temperature: $T_{amb} = 0°C$ to $+70°C$

Characteristics	Symbol	Value		Units	Grade	Conditions	Notes
		Min.	Max.				
Maximum frequency sinewave input	f_{max}	700 600 400		MHz MHz MHz	SP8634B SP8635B SP8637B	Input = 400-800mV p-p	Note 5
Minimum frequency sinewave input	f_{min}		40	MHz	All	Input = 400-800mV p-p	Note 7
Power supply current	I_{EE}		90	mA	All	$V_{EE} = -5.2V$	Note 6
Clock inhibit high voltage	V_{INH}	-0.96		V	All	$V_{EE} = -5.2V$ (25°C)	
Clock inhibit low voltage	V_{INL}		-1.65	V	All	$V_{EE} = -5.2V$ (25°C)	
TTL output high voltage (pin 2,7,8,10)	V_{OH}	2.4		V	All	10kΩ from TTL output too +5V	Note 6
TTL output low voltage (pin 2,7,8,10)	V_{OL}		0.4	V	All	10kΩ from TTL output to +5V	Note 6
TTL output voltage (pin 11)	V_{OH}	2.4		V	All	5kΩ from TTL output to +5V	Note 6
TTL output low voltage (pin 11)	V_{OL}		0.4	V	All	5kΩ from TTL output to +5V	Note 6
ECL output high voltage (pin 9)	V_{OH}	-0.9	-0.7	V	All	$V_{EE} = -5.2V$ (25°C)	
ECL output low voltage (pin 9)	V_{OL}	-1.8	-1.5	V	All	$V_{EE} = -5.2V$ (25°C)	
Edge speed for correct operation at maximum frequency	t_E		2.5	ns	All	10% to 90%	Note 7
Reset on time for correct operation	t_{ON}	100		ns	All		Note 7
Reset input high voltage	V_{INH}	2.4		V	All		Note 6
Reset input low voltage	V_{INL}		0.5	V	All		Note 6

NOTES
1. Unless otherwise stated the electrical characteristics are guaranteed over full specified supply, frequency and temperature range.
2. The temperature coefficient of V_{OH} (ECL) = +1.3mV/°C and V_{OL} = +0.5mV/°C but these are not tested.
3. The temperature coefficient of inhibit threshold voltage = +0.24mV/°C but this is not tested.
4. The test configuration for dynamic testing is shown in Fig.5.
5. Tested at 0°C and +70°C only.
6. Tested at +25°C only.
7. Guaranteed but not tested.
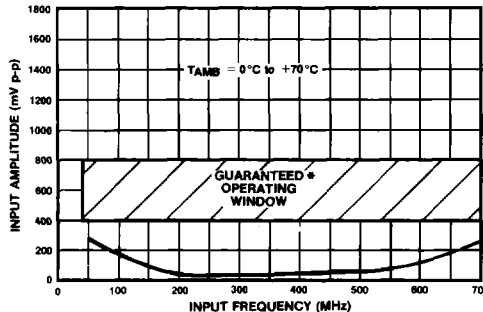
*Tested as specified in table of Electrical Characteristics

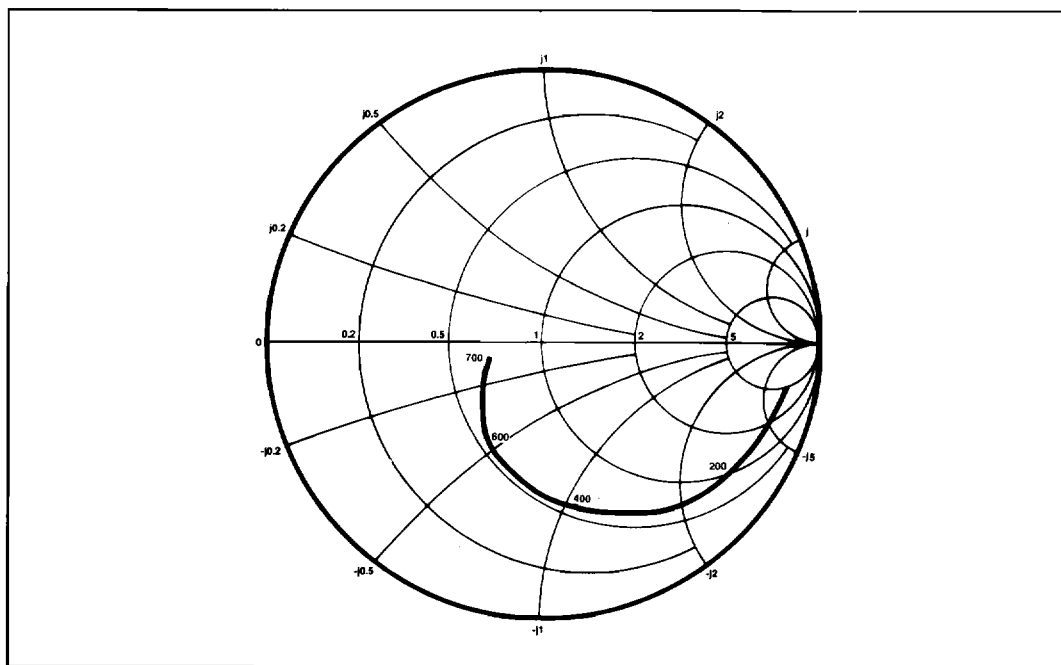Fig.3 Typical input characteristics SP8634

Fig.4 Typical input impedance. Test conditions: supply voltage 5.2V, ambient temperature 25°C. Frequencies in MHz, impedances normalised to 50 ohms.
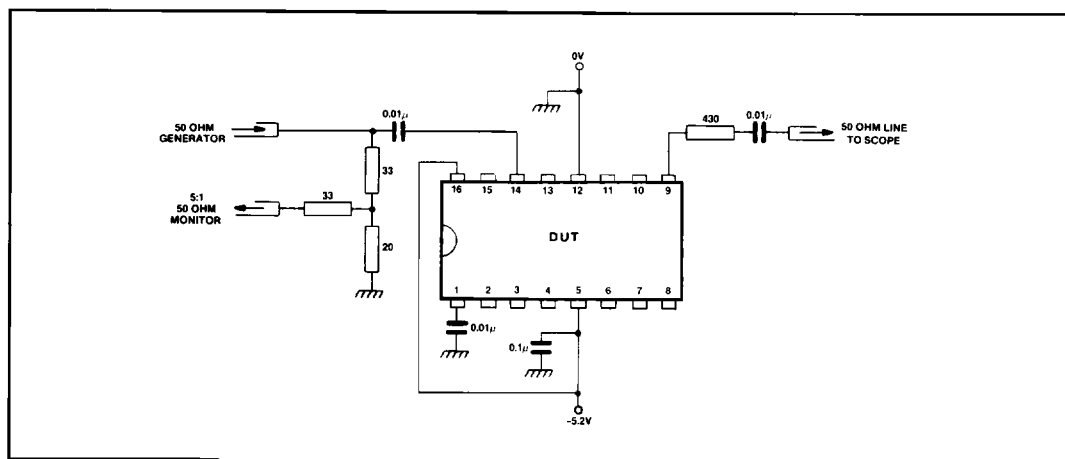

Fig.5 SP8634/5/7 high frequency test circuit

OPERATING NOTES

1. The clock input (pin 14) should be capacitively coupled to the signal source. The input signal path is completed by connecting a capacitor from the internal bias decoupling, pin 1, to ground.

2. In the absence of a signal the devices will self-oscillate. This can be prevented by connecting a 68k resistor between the clock input, pin 14, and the negative supply (pin 5).

3. The device will operate down to DC but the input slew rate must be better than 100V/μs.

4. The Carry O/P is ECL II compatible but can be interfaced ECL III/10K by the inclusion of two resistors. See Fig. 7.

5. The clock inhibit is compatible with ECL III/10K throughout the temperature range.

6. The output (pins 2, 7, 8, 10 and 11) are current sources and can be made TTL compatible by addition of 10k and 5k (pin 11) to +5V. See Fig.6. This gives a fan-out of 1. This can be increased by buffering the output with a PNP emitter follower. See Fig.8.

7. The device is clocked on the positive transition of the clock input on pin 14, provided that the clock inhibit input (pin 16) is in the low state. It is important to note that the positive transition of clock inhibit must occur while the clock is in the high state to avoid spurious counting.
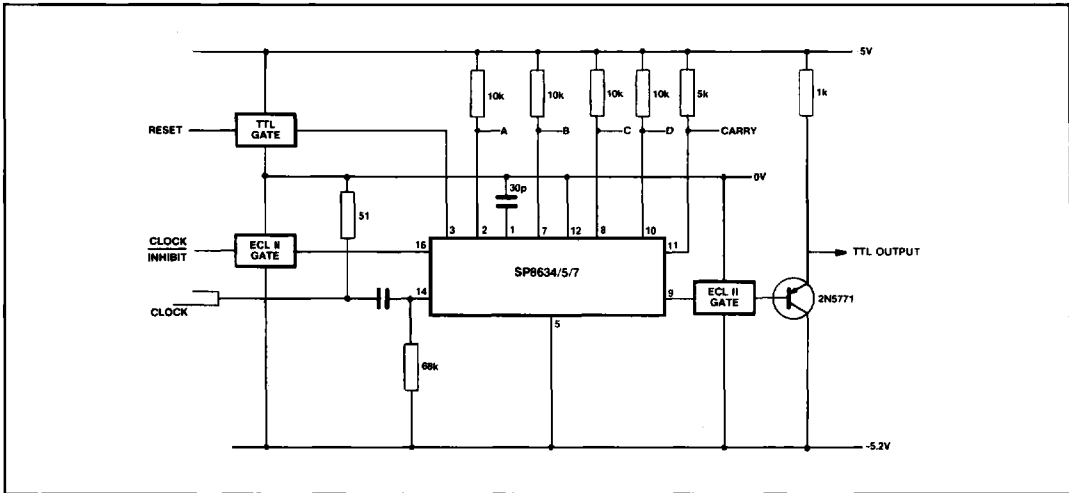
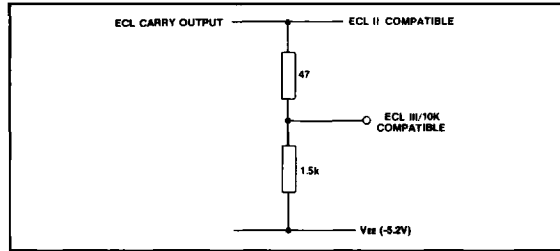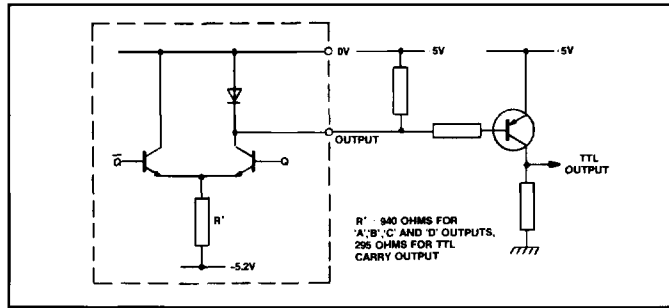Fig.6 Typical application configuration

Fig.7 ECL III/10K interfacing
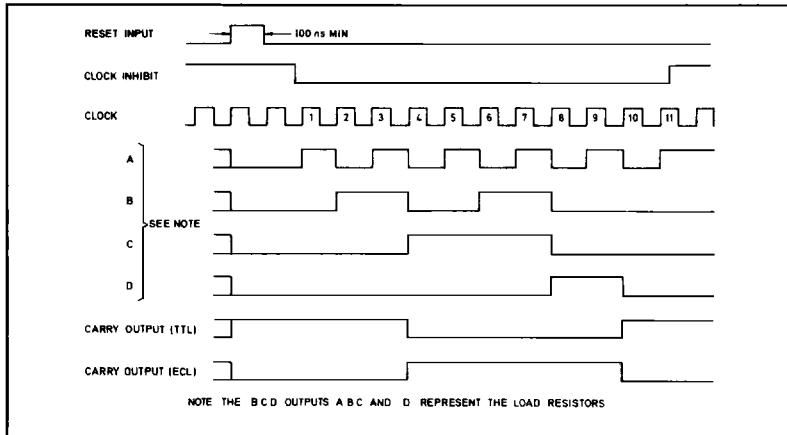

Fig.8 TTL output buffering for increased fan-out

Fig.9 Timing diagram