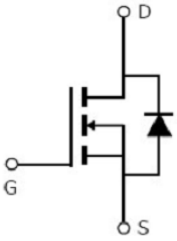
Main Product Characteristics:

V_{DSS}	170V(typ)
R_{DS}(on)	0.15Ω(typ)
I_D	8A

DPAK

Marking and pin Assignment



Schematic diagram

Features and Benefits:

- Advanced trench MOSFET process technology
- Special designed for PWM, load switching and general purpose applications
- Ultra low on-resistance with low gate charge
- Fast switching and reverse body recovery
- 175℃ operating temperature

Description:

It utilizes the latest trench processing techniques to achieve the high cell density and reduces the on-resistance with high repetitive avalanche rating. These features combine to make this design an extremely efficient and reliable device for use in power switching application and a wide variety of other applications

Absolute max Rating:

Symbol	Parameter	Max.	Units
I_D @ TC = 25°C	Continuous Drain Current, V_{GS} @ 10V①	8	A
I_D @ TC = 100°C	Continuous Drain Current, V_{GS} @ 10V①	5	
I_{DM}	Pulsed Drain Current②	32	
P_D @TC = 25°C	Power Dissipation③	33	W
	Linear Derating Factor	0.18	W/°C
V_{DS}	Drain-Source Voltage	150	V
V_{GS}	Gate-to-Source Voltage	± 20	V
T_J T_{STG}	Operating Junction and Storage Temperature Range	-55 to + 175	°C

Thermal Resistance

Symbol	Characterizes	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-case③	—	4.5	℃/W
$R_{\theta JA}$	Junction-to-Ambient (t ≤ 10s) ④	—	70	℃/W
	Junction-to-Ambient (PCB mounted, steady-state) ④	—	53	℃/W

Electrical Characterizes @T_A=25℃ unless otherwise specified

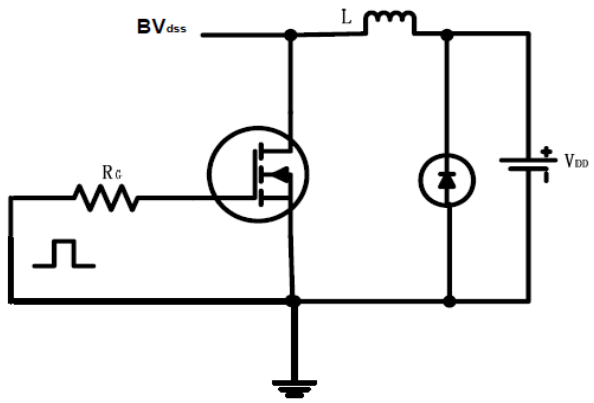
Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
$V_{(BR)DSS}$	Drain-to-Source breakdown voltage	150	170		V	V_{GS} = 0V, ID = 250μA
$R_{DS(on)}$	Static Drain-to-Source on-resistance	—	0.15	0.2	Ω	V_{GS}=10V,I_D = 3A
		—	0.32	—		T_J = 125℃
$V_{GS(th)}$	Gate threshold voltage	2	—	4	V	V_{DS} = V_{GS}, I_D = 250μA
		—	2.7	—		T_J = 125℃
I_{DSS}	Drain-to-Source leakage current	—	—	1	μA	V_{DS} = 150,Vgs=10V
		—	—	50		T_J = 125°C
I_{GSS}	Gate-to-Source forward leakage			100	A	V_{GS} =20V
	Gate-to-Source reverse leakage	-100	-			V_{GS} = -20V
Q_g	Total gate charge		37		nC	I_D = 6A
Q_{gs}	Gate-to-Source charge		7.5			V_{DD}=120V
Q_{gd}	Gate-to-Drain("Miller") charge		13.			V_{GS} = 10V
$t_{d(on)}$	Turn-on delay time		32		ns	V_{GS}=10V, VDD=24.6V,
t_r	Rise time		51.5			R_L=8.2Ω,
$t_{d(off)}$	Turn-Off delay time		157			R_{GEN}=2.55Ω
t_f	Fall time		67			ID=3.00A
C_{iss}	Input capacitance		1524		pF	V_{GS} = 0V
C_{oss}	Output capacitance		171			V_{DS} = 25V
C_{rss}	Reverse transfer capacitance		77			f = 800KHz

Source-Drain Ratings and Characteristics

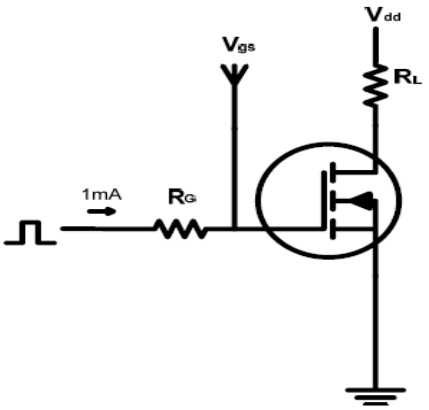
Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
I_S	Continuous Source Current (Body Diode)	—	—	8	A	MOSFET symb showing the integral reverse p-n junction diode.
I_{SM}	Pulsed Source Current (Body Diode)	—	—	32	A	
V_{sd}	Diode Forward Voltage		0.82	1.5	V	I_S=6.00A, V_{GS}=0V,T_J= 25°C
t_{rr}	Reverse Recovery Time		90		ns	T_J = 25°C, I_F =6.00A, di/dt = 25.0A/μs
Q_{rr}	Reverse Recovery Charge		105		nC	

Test circuits and Waveforms

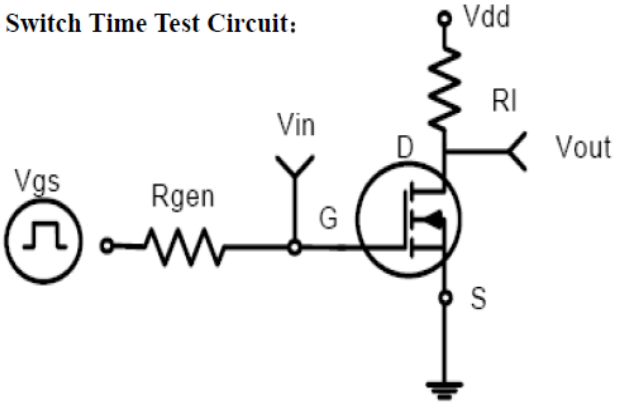
EAS test circuits:



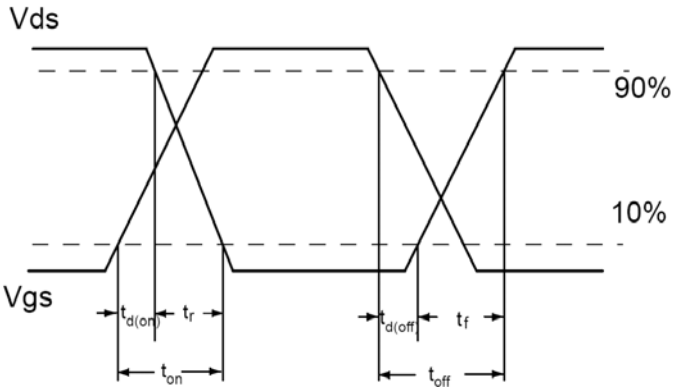
Gate charge test circuit:



Switch Time Test Circuit:



Switch Waveforms:



Notes:

①The maximum current rating is limited by bond-wires.
②Repetitive rating; pulse width limited by max. junction temperature.
③The power dissipation PD is based on max. junction temperature, using junction-to-case thermal resistance.
④The value of $R_{\theta JA}$ is measured with the device mounted on 1in 2 FR-4 board with 2oz. Copper, in a still air environment with TA =25°C
⑤These curves are based on the junction-to-case thermal impedence which is measured with the device mounted to a large heatsink, assuming a maximum junction temperature of $T_{J(MAX)}$=175°C.
⑥ The maximum current rating is limited by bond-wires.

Typical electrical and thermal characteristics

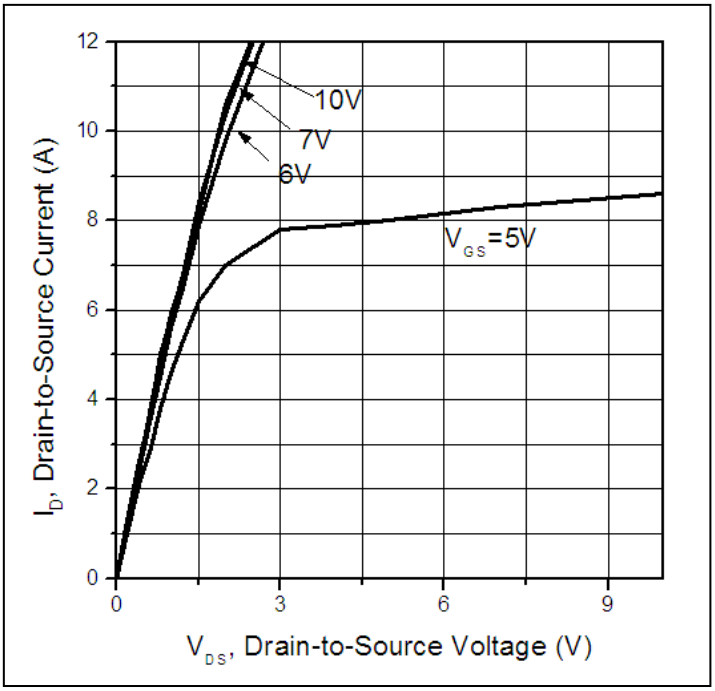


Figure 1: Typical Output Characteristics

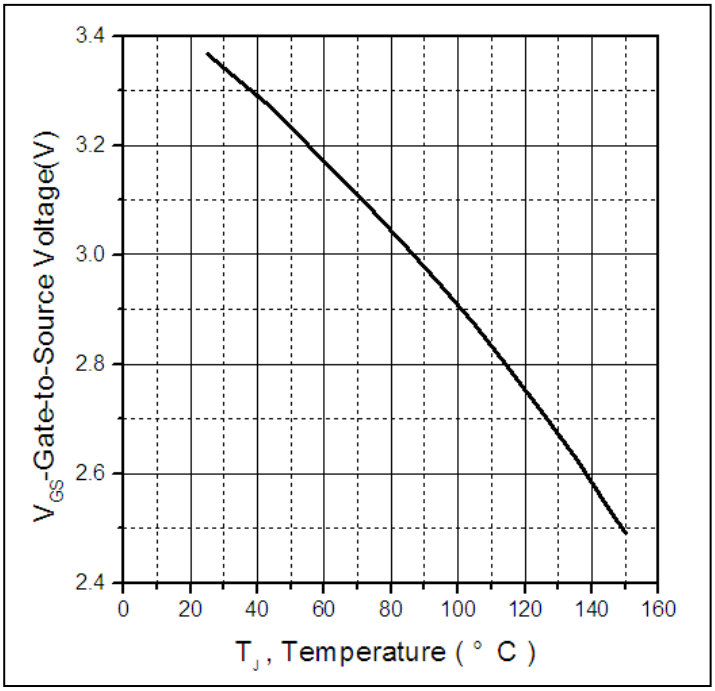


Figure 2. Gate to source cut-off voltage

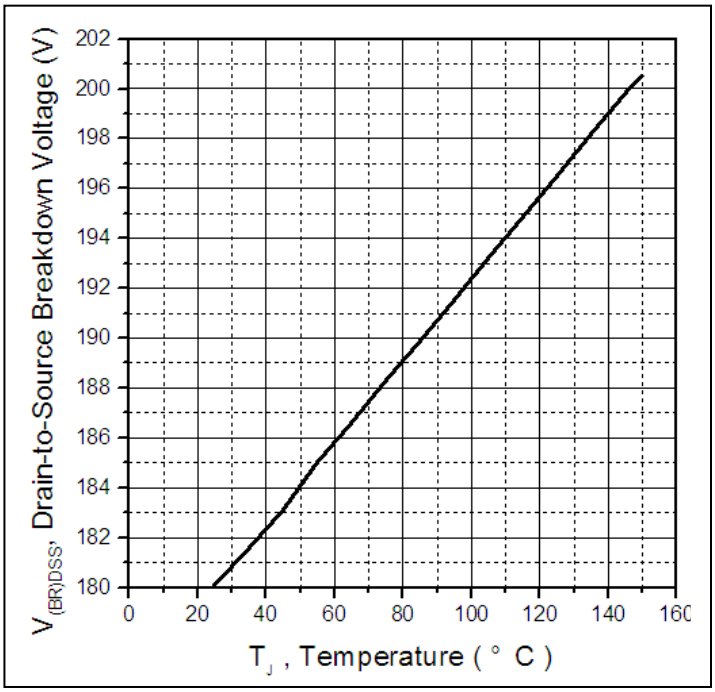


Figure 3. Drain-to-Source Breakdown Voltage vs. Temperature

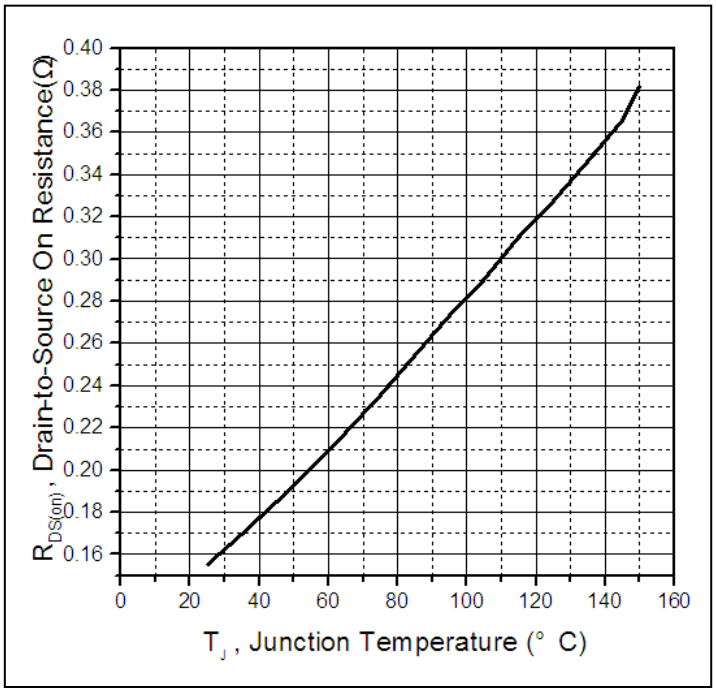


Figure 4: Normalized On-Resistance Vs. Case Temperature

Typical electrical and thermal characteristics

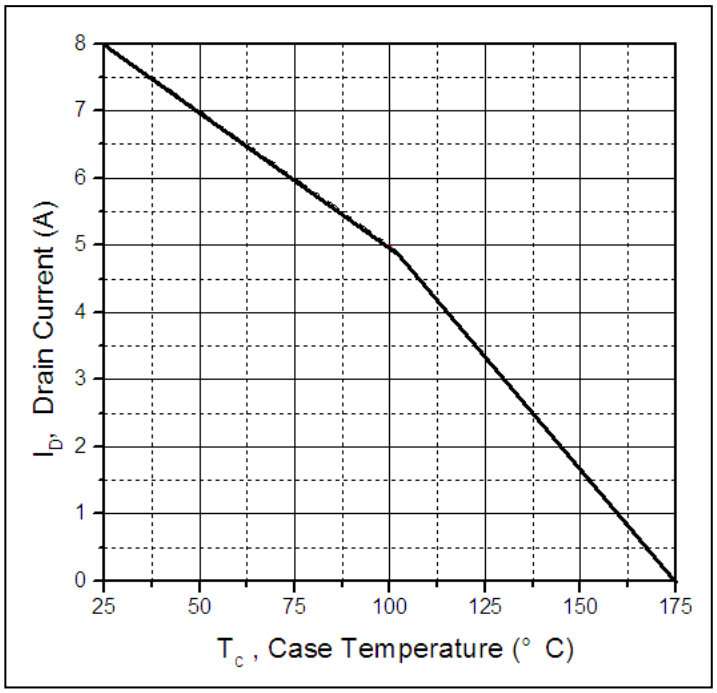


Figure 5. Maximum Drain Current Vs. Case Temperature

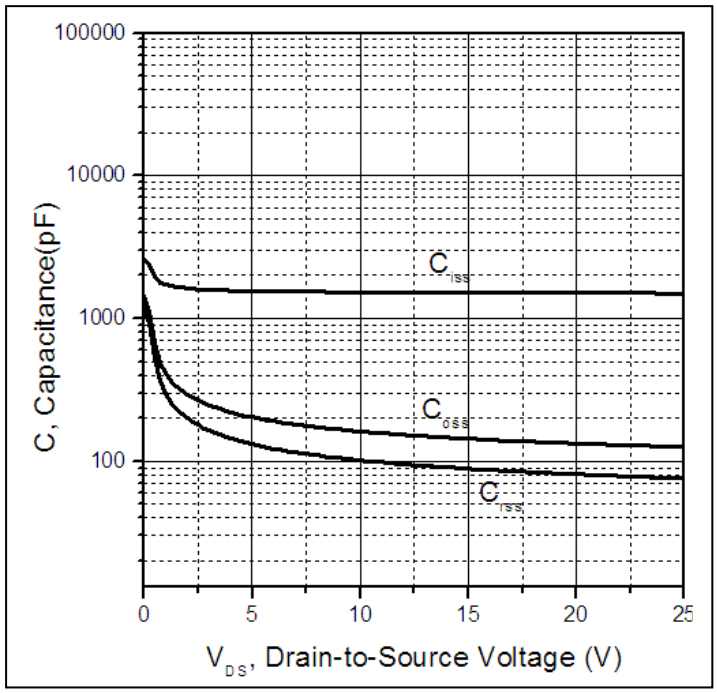


Figure 6.Typical Capacitance Vs. Drain-to-Source Voltage

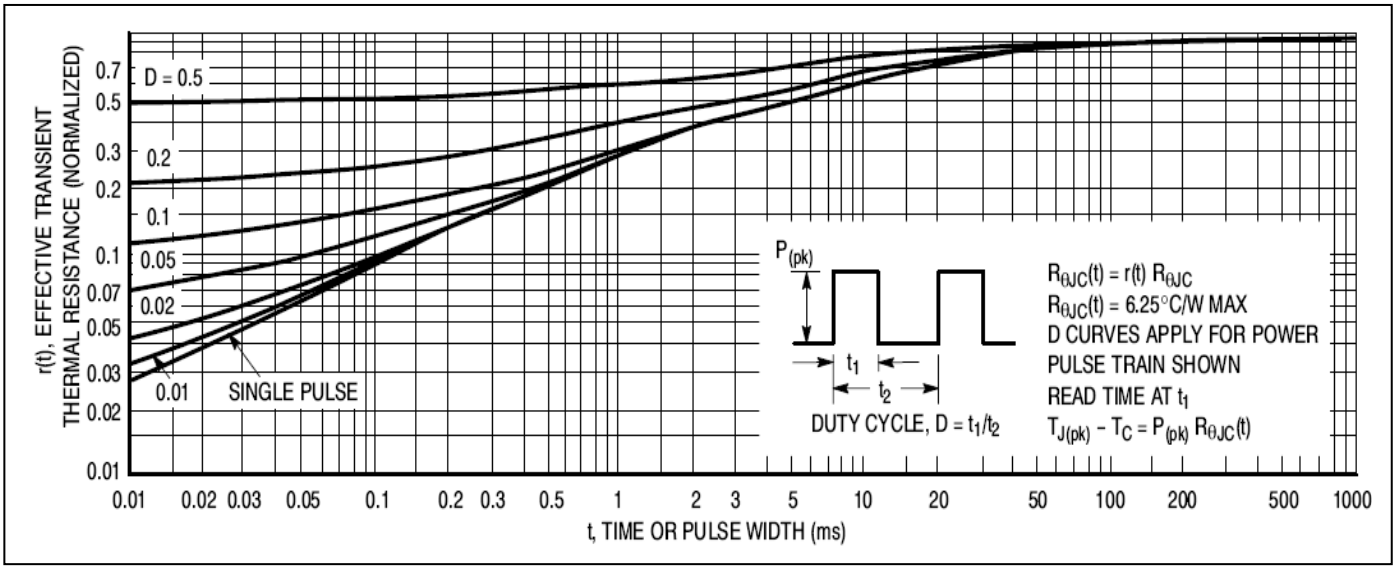
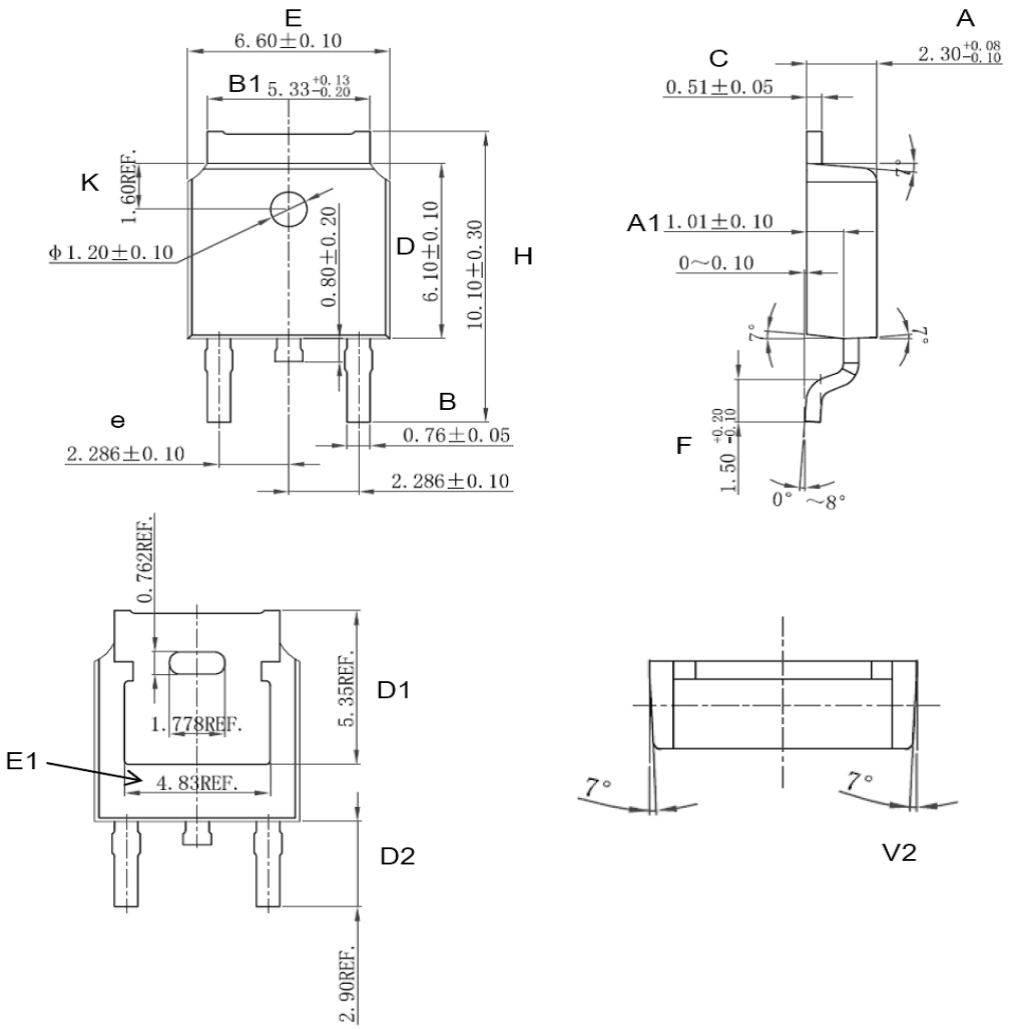


Figure7. Maximum Effective Transient Thermal Impedance, Junction-to-Case

Mechanical Data：

DPAK PACKAGE OUTLINE DIMENSION_CD



Symbol	Dimension In Millimeters			Dimension In Inches		
	Min	Nom	Max	Min	Nom	Max
A	2.200	2.300	2.380	0.087	0.091	0.094
A1	0.910	1.010	1.110	0.036	0.040	0.044
B	0.710	0.760	0.810	0.028	0.030	0.032
B1	5.130	5.330	5.460	0.202	0.210	0.215
C	0.460	0.510	0.560	0.018	0.020	0.022
D	6.000	6.100	6.200	0.236	0.240	0.244
D1	5.350 (REF)			0.211 (REF)		
D2	2.900 (REF)			0.114 (REF)		
E	6.500	6.600	6.700	0.256	0.260	0.264
E1	4.83 (REF)			0.190 (REF)		
e	2.186	2.286	2.386	0.086	0.090	0.094
H	9.800	10.100	10.400	0.386	0.398	0.409
F	1.400	1.500	1.700	0.055	0.059	0.067
K	1.600 (REF)			0.063 (REF)		
V2	8^0 (REF)			8^0 (REF)		

Ordering and Marking Information

Device Marking: SSF1502D

Package (Available)

DPAK

Operating Temperature Range

C : -55 to 175 ºC

Devices per Unit

Package Type	Units/Tube	Tubes/Inner Box	Units/Inner Box	Inner Boxes/Carton Box	Units/Carton Box
DPAK	80	50	4000	10	40000

Reliability Test Program

Test Item	Conditions	Duration	Sample Size
High Temperature Reverse Bias(HTRB)	T_j=125℃ to 175℃ @ 80% of Max V_{DSS}/V_{CES}/VR	168 hours 500 hours 1000 hours	3 lots x 77 devices
High Temperature Gate Bias(HTGB)	T_j=150℃ or 175℃ @ 100% of Max V_{GSS}	168 hours 500 hours 1000 hours	3 lots x 77 devices

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Customer Service

Worldwide Sales and Service:

Sales@silikron.com

Technical Support:

Technical@silikron.com

Suzhou Silikron Semiconductor Corp.

11A, 428 Xinglong Street, Suzhou Industrial Park, P.R.China

TEL: (86-512) 62560688

FAX: (86-512) 65160705

E-mail: Sales@silikron.com