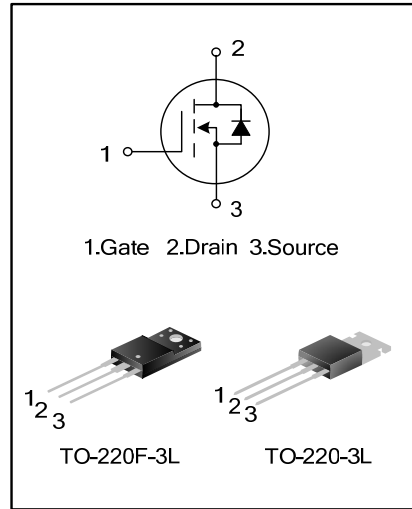


8A, 800V N-CHANNEL MOSFET

GENERAL DESCRIPTION

SVD8N80T/F is an N-channel enhancement mode power MOS field effect transistor which is produced using Silan proprietary S-Rin™ structure DMOS technology. The improved planar stripe cell and the improved guard ring terminal have been especially tailored to minimize on-state resistance, provide superior switching performance, and withstand high energy pulse in the avalanche and commutation mode.

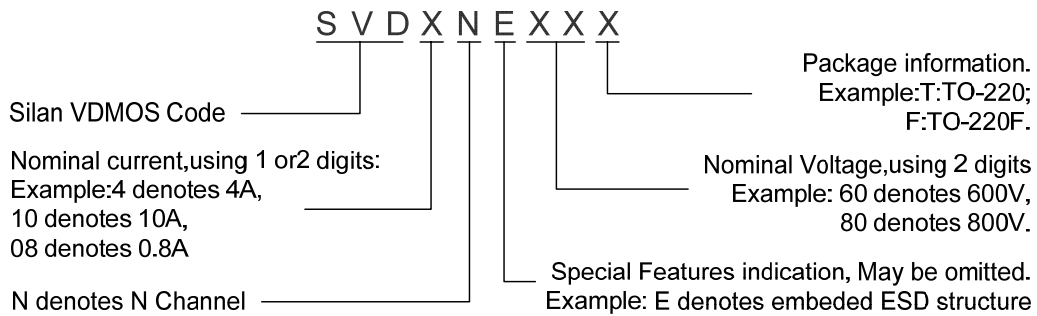
These devices are widely used in AC-DC power suppliers, DC-DC converters and H-bridge PWM motor drivers.



FEATURES

- * 8A,800V,RDS(on) (typ) =1.3Ω@VGS=10V
- * Low gate charge
- * Low Crss
- * Fast switching
- * Improved dv/dt capability

NOMENCLATURE



ORDERING SPECIFICATIONS

Part No.	Package	Marking	Material	Packing
SVD8N80T	TO-220-3L	SVD8N80T	Pb free	Tube
SVD8N80F	TO-220F-3L	SVD8N80F	Pb free	Tube

ABSOLUTE MAXIMUM RATINGS (T_c=25°C unless otherwise noted)

Parameter	Symbol	Rating		Unit
		SVD8N80T	SVD8N80F	
Drain-Source Voltage	V _{DS}	800		V
Gate-Source Voltage	V _{GS}	±30		V
Drain Current	I _D	8.0		A
Drain Current Pulsed	I _{DM}	35		A
Power Dissipation(T _C =25°C) -Derate above 25°C	P _D	180	59	W
		1.44	0.48	W/°C
Single Pulsed Avalanche Energy (Note 1)	E _{AS}	402		mJ
Operation Junction Temperature	T _J	-55~+150		°C
Storage Temperature	T _{stg}	-55~+150		°C

THERMAL CHARACTERISTICS

Parameter	Symbol	Rating		Unit
		SVD8N80T	SVD8N80F	
Thermal Resistance, Junction-to-Case	R _{θJC}	0.7	2.0	°C/W
Thermal Resistance, Junction-to-Ambient	R _{θJA}	62.5	120	°C/W

ELECTRICAL CHARACTERISTICS (T_c=25°C unless otherwise noted)

Parameter	Symbol	Test conditions	Min.	Typ.	Max.	Unit
Drain -Source Breakdown Voltage	B _V DSS	V _{GS} =0V, I _D =250μA	800	--	--	V
Drain-Source Leakage Current	I _{DSS}	V _{DS} =800V, V _{GS} =0V	--	--	10	μA
Gate-Source Leakage Current	I _{GSS}	V _{GS} =±30V, V _{DS} =0V	--	--	±100	nA
Gate Threshold Voltage	V _{GS(th)}	V _{GS} = V _{DS} , I _D =250μA	2.5	--	4.5	V
Static Drain- Source On State Resistance	R _{DS(on)}	V _{GS} =10V, I _D =4A	--	1.3	1.55	Ω
Input Capacitance	C _{iss}	V _{DS} =25V, V _{GS} =0V, f=1.0MHz	--	1354	2020	pF
Output Capacitance	C _{oss}		--	112	171	
Reverse Transfer Capacitance	C _{rss}		--	11	18	
Turn-on Delay Time	t _{d(on)}	V _{DD} =400V, I _D =8.0A, R _G =25Ω (Note 2,3)	--	39.6	87	ns
Turn-on Rise Time	t _r		--	76	240	
Turn-off Delay Time	t _{d(off)}		--	82.2	135	
Turn-off Fall Time	t _f		--	43.8	145	
Total Gate Charge	Q _g	V _{DS} =640V, I _D =8.0A, V _{GS} =10V (Note 2,3)	--	32.2	45	nC
Gate-Source Charge	Q _{gs}		--	7.66	--	
Gate-Drain Charge	Q _{gd}		--	15.27	--	

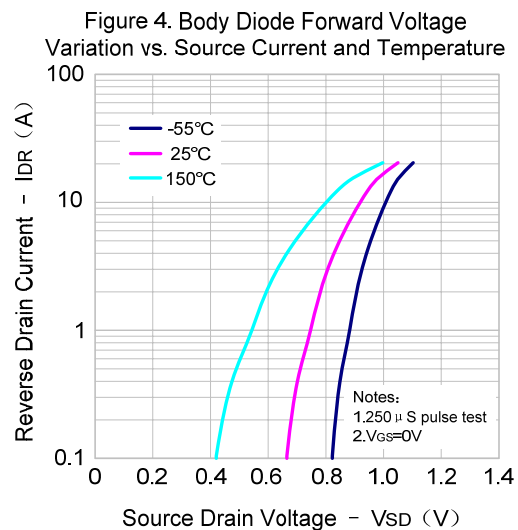
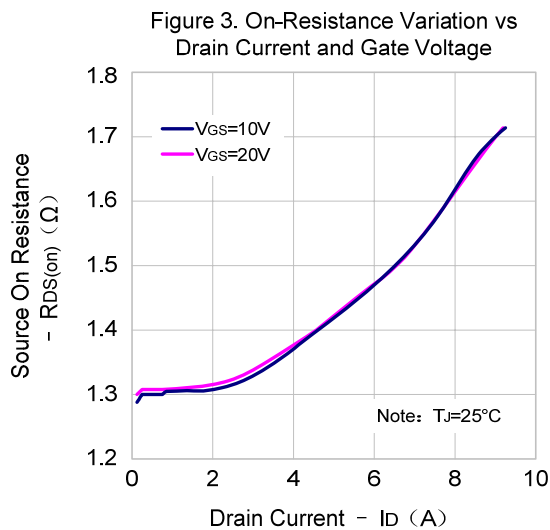
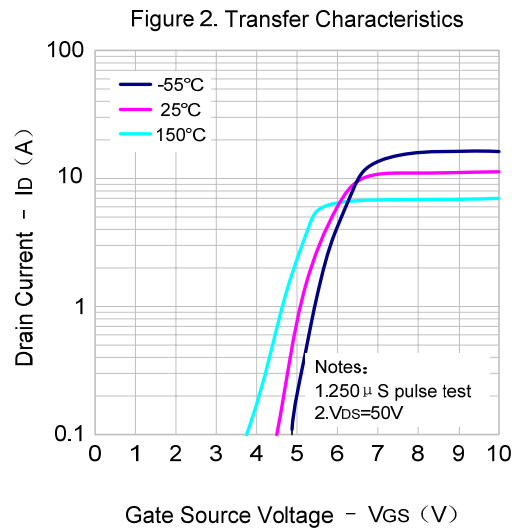
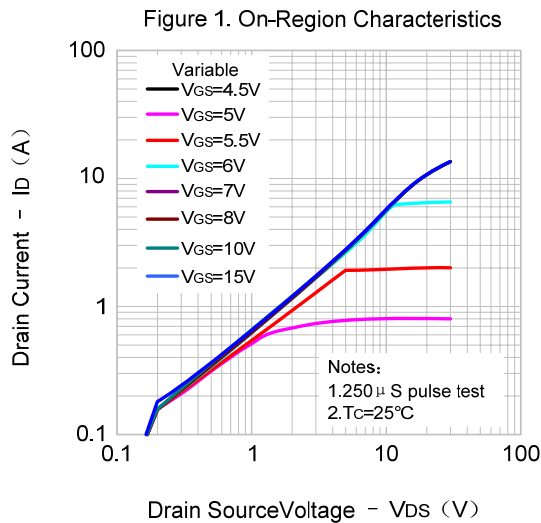
SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS

Parameter	Symbol	Test conditions	Min.	Typ.	Max.	Unit
Continuous Source Current	IS	Integral Reverse P-N Junction Diode in the MOSFET	--	--	8.0	A
Pulsed Source Current	ISM		--	--	32	
Diode Forward Voltage	VSD	IS=8.0A, VGS=0V	--	--	1.4	V
Reverse Recovery Time	Trr	IS=8.0A, VGS=0V, dIF/dt=100A/μS	--	680	--	ns
Reverse Recovery Charge	Qrr		--	8.1	--	μC

Notes:

1. L=30mH, IAS=4.74A, VDD=160V, RG=25Ω, starting T_J=25°C;
2. Pulse Test: Pulse width ≤300μs, Duty cycles≤2%;
3. Essentially independent of operating temperature.

TYPICAL CHARACTERISTICS



TYPICAL CHARACTERISTICS(continue)

Figure 5. Capacitance Characteristics

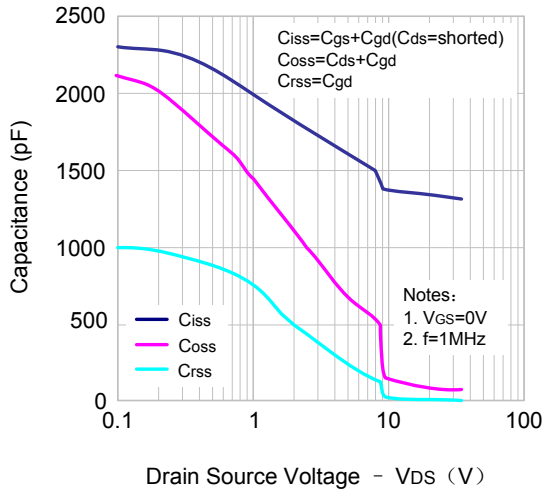


Figure 6. Gate Charge Characteristics

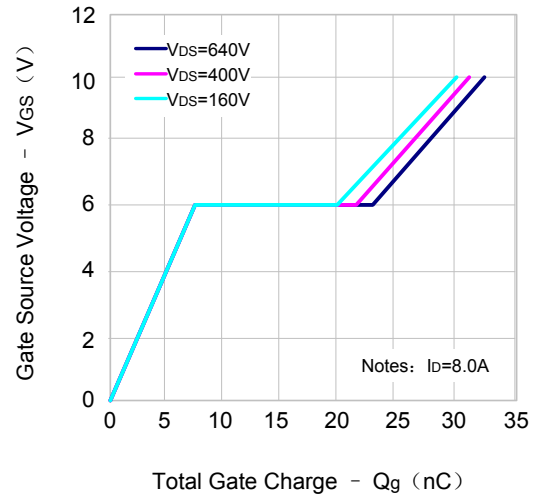


Figure 7. Breakdown Voltage Variation vs. Temperature

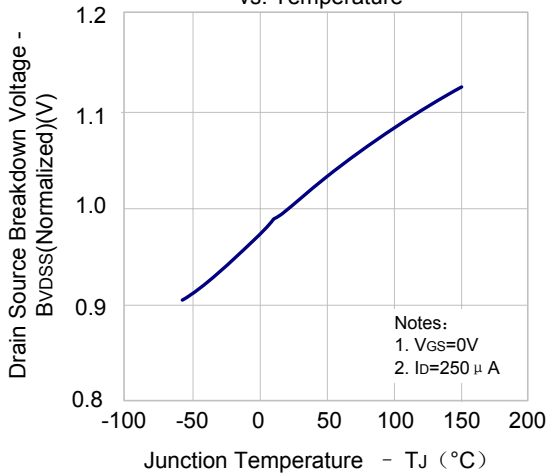
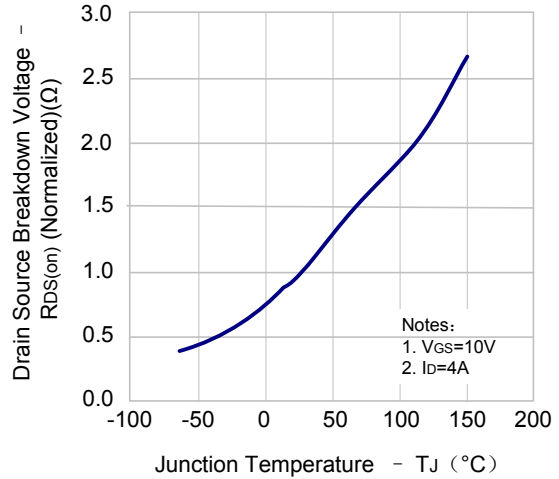
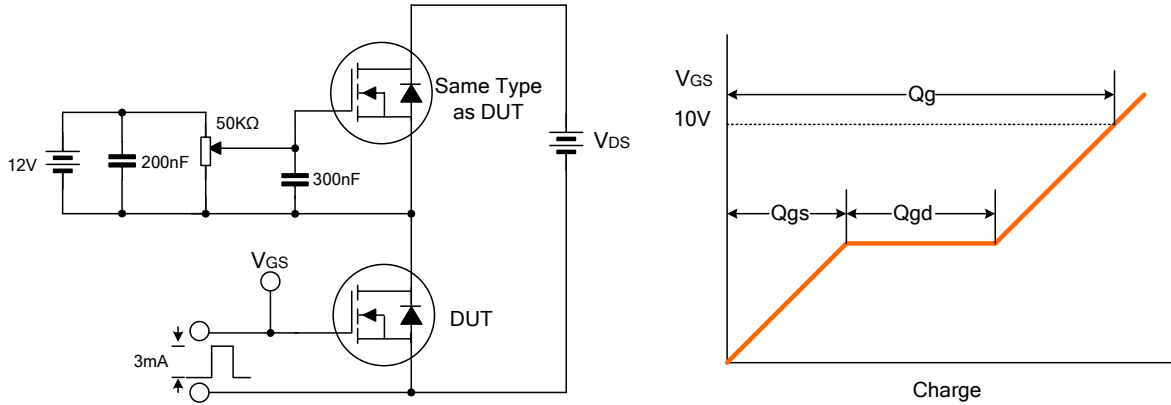


Figure 8. On-Resistance Variation

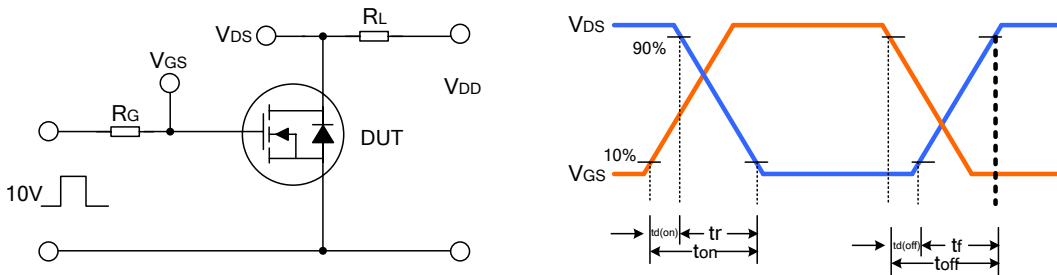


TYPICAL TEST CIRCUIT

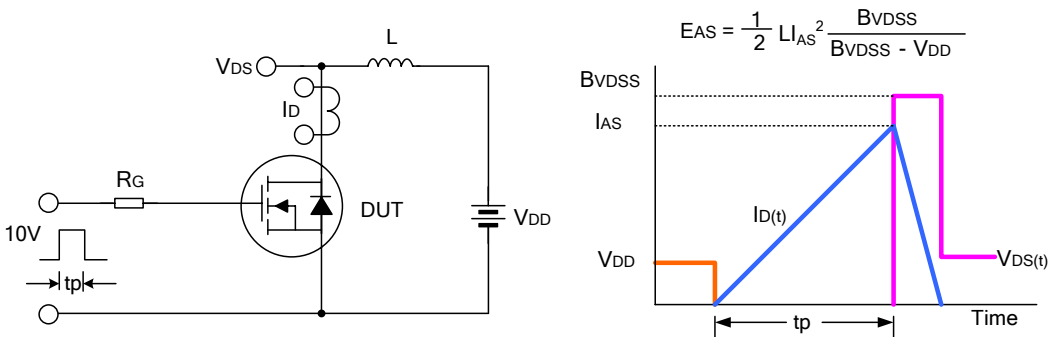
Gate Charge Test Circuit & Waveform



Resistive Switching Test Circuit & Waveform



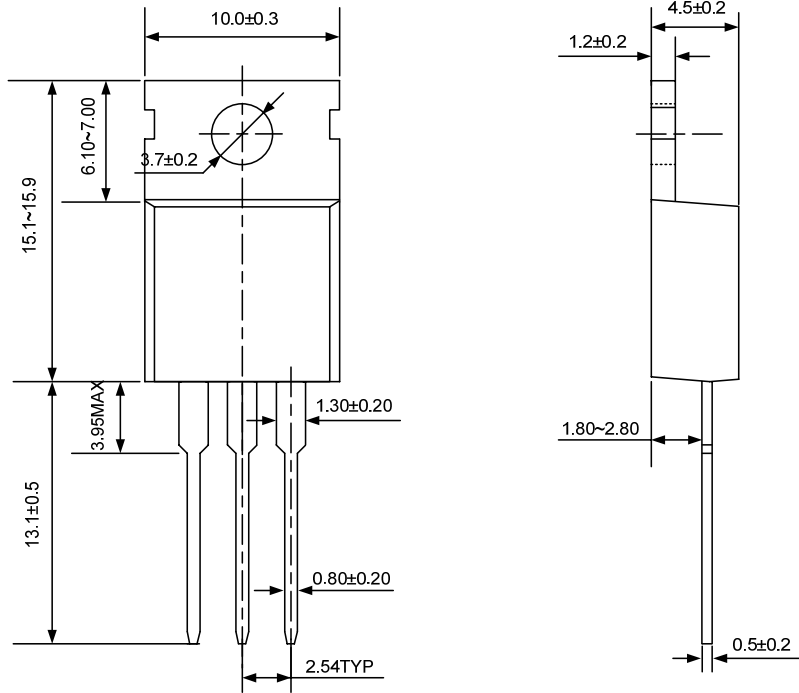
Unclamped Inductive Switching Test Circuit & Waveform



PACKAGE OUTLINE

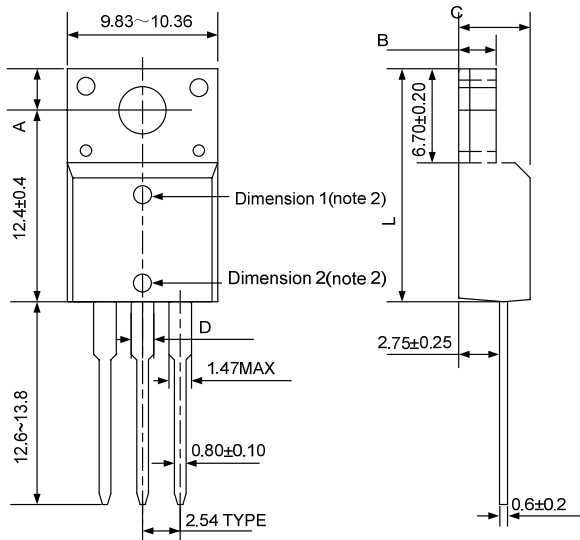
TO-220-3L

UNIT: mm



TO-220F-3L

UNIT: mm



Symbol(note1)	Dimension1	Dimension2
A	3.30 ± 0.15	2.70 ± 0.15
B	2.55 ± 0.20	3.0 ± 0.20
C	4.72 ± 0.2	4.50 ± 0.20
D	1.47 MAX	1.75 MAX
L	15.75 ± 0.30	15.00 ± 0.30

Note1: There may be two values for some products due to different plastic mould machine, so two dimensions of the same position are listed;
 Note2: When the product size is Dimension1, the thimble hole is on top of the surface; when the size is Dimension2, the center hole is on bottom of the surface.

Disclaimer:

- Silan reserves the right to make changes to the information herein for the improvement of the design and performance without further notice! Customers should obtain the latest relevant information before placing orders and should verify that such information is complete and current.
- All semiconductor products malfunction or fail with some probability under special conditions. When using Silan products in system design or complete machine manufacturing, it is the responsibility of the buyer to comply with the safety standards strictly and take essential measures to avoid situations in which a malfunction or failure of such Silan products could cause loss of body injury or damage to property.
- Silan will supply the best possible product for customers!

ATTACHMENT**Revision History**

Date	REV	Description	Page
2010.06.07	1.0	Original	
2010.10.20	1.1	Modify the template of Datasheet	