FAIRCHILD SEMICONDUCTOR®

November 2010

FDMC6296

Single N-Channel Logic-Level Power Trench® MOSFET

30 V, 11.5 A, 10.5 mΩ

Features

- Max $r_{DS(on)}$ = 10.5 mΩ at V_{GS} = 10 V, I_D = 11.5 A
- Max $r_{DS(on)}$ = 15 mΩ at V_{GS} = 4.5 V, I_D = 10 A
- Low Qg, Qgd and Rg for efficient switching performance
- RoHS Compliant

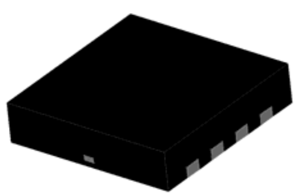
General Description

This single N-Channel MOSFET in the thermally efficient MicroFET Package has been specifically designed to perform well in Point of Load converters. Providing an optimized balance between $r_{DS(on)}$ and gate charge this device can be effectively used as a “high side” control swtich or “low side” synchronous rectifier.

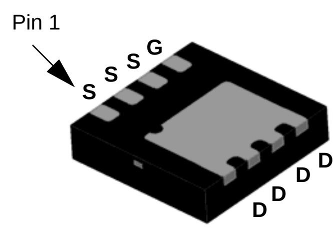
Application

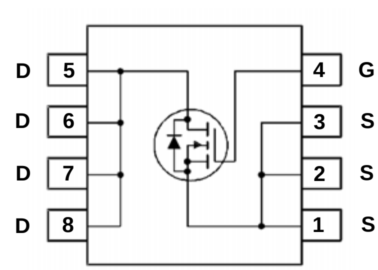
- Point of Load Converters
- 1/16 Brick Synchronous Rectifier

Top



Bottom





MLP 3.3X3.3

MOSFET Maximum Ratings T_A = 25 °C unless otherwise noted

Symbol	Parameter	Ratings	Units
V_{DS}	Drain to Source Voltage	30	V
V_{GS}	Gate to Source Voltage	±20	V
I_D	Drain Current -Continuous T_A = 25 °C (Note 1a)	11.5	A
	-Pulsed	40	
P_D	Power Dissipation T_C = 25 °C	2.1	W
	Power Dissipation T_A = 25 °C (Note 1a)	0.9	
T_J, T_{STG}	Operating and Storage Junction Temperature Range	-55 to +150	°C

Thermal Characteristics

$R_{\theta JC}$	Thermal Resistance, Junction to Case (Note 1)	3	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (Note 1a)	53	

Package Marking and Ordering Information

Device Marking	Device	Package	Reel Size	Tape Width	Quantity
FDMC6296	FDMC6296	MLP 3.3X3.3	13 ”	12 mm	3000 units

Electrical Characteristics T_J = 25 °C unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units

Off Characteristics

BV_{DSS}	Drain to Source Breakdown Voltage	I_D = 250 μA, V_{GS} = 0 V	30			V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	I_D = 250 μA, referenced to 25 °C		26		mV/°C
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = 24 V, V_{GS} = 0 V			1	μA
I_{GSS}	Gate to Source Leakage Current	V_{GS} = ±20 V, V_{DS} = 0 V			±100	nA

On Characteristics

$V_{GS(th)}$	Gate to Source Threshold Voltage	V_{GS} = V_{DS}, I_D = 250 μA	1	1.8	3	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate to Source Threshold Voltage Temperature Coefficient	I_D = 250 μA, referenced to 25 °C		-6		mV/°C
$r_{DS(on)}$	Static Drain to Source On Resistance	V_{GS} = 10 V, I_D = 11.5 A		8.7	10.5	mΩ
		V_{GS} = 4.5 V, I_D = 10 A		10.6	15	
		V_{GS} = 10 V, I_D = 11.5 A, T_J = 125 °C		13	17	
g_{FS}	Forward Transconductance	V_{DD} = 5 V, I_D = 11.5 A		49		S

Dynamic Characteristics

C_{iss}	Input Capacitance	V_{DS} = 15 V, V_{GS} = 0 V, f = 1 MHz		1610	2141	pF
C_{oss}	Output Capacitance			406	540	pF
C_{rss}	Reverse Transfer Capacitance			150	225	pF
R_g	Gate Resistance	V_{GS} = 0 V, f = 1 MHz		0.9		Ω

Switching Characteristics

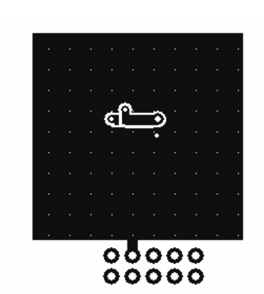
$t_{d(on)}$	Turn-On Delay Time	V_{DD} = 15 V, I_D = 1.0 A, V_{GS} = 10 V, R_{GEN} = 6 Ω		10	20	ns
t_r	Rise Time			3	10	ns
$t_{d(off)}$	Turn-Off Delay Time			27	43	ns
t_f	Fall Time			8	16	ns
$Q_{g(TOT)}$	Total Gate Charge at 5V	V_{GS} = 5 V, V_{DD} = 15 V, I_D = 11.5 A		14	19	nC
Q_{gs}	Total Gate Charge			4		nC
Q_{gd}	Gate to Drain “Miller” Charge			4		nC

Drain-Source Diode Characteristics

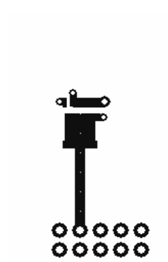
V_{SD}	Source to Drain Diode Forward Voltage	V_{GS} = 0 V, I_S = 2 A (Note 2)		0.7	1.2	V
t_{rr}	Reverse Recovery Time	I_F = 11.5 A, di/dt = 100 A/μs		30		ns
Q_{rr}	Reverse Recovery Charge			22		nC

Notes:

1. $R_{\theta JA}$ is determined with the device mounted on a 1in^2 pad 2 oz copper pad on a 1.5 x 1.5 in. board of FR-4 material. $R_{\theta JC}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design.



a. 53 °C/W when mounted on a 1 in^2 pad of 2 oz copper



b. 125 °C/W when mounted on a minimum pad of 2 oz copper

2. Pulse Test: Pulse Width < 300 μs, Duty cycle < 2.0%.

Typical Characteristics T_J = 25°C unless otherwise noted

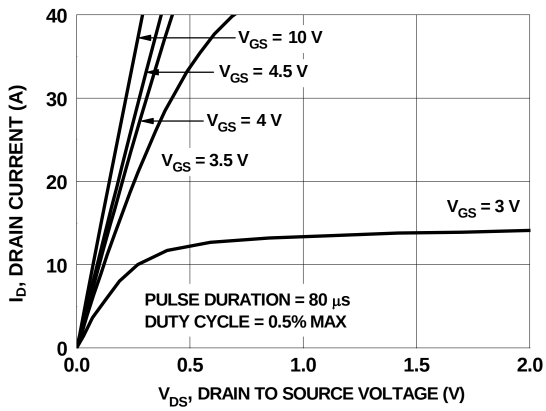


Figure 1. On Region Characteristics

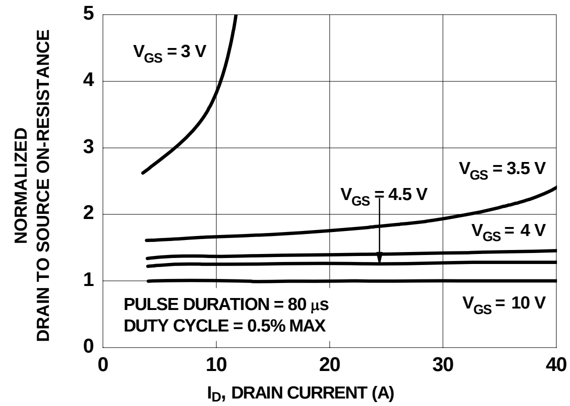


Figure 2. Normalized On-Resistance vs Drain Current and Gate Voltage

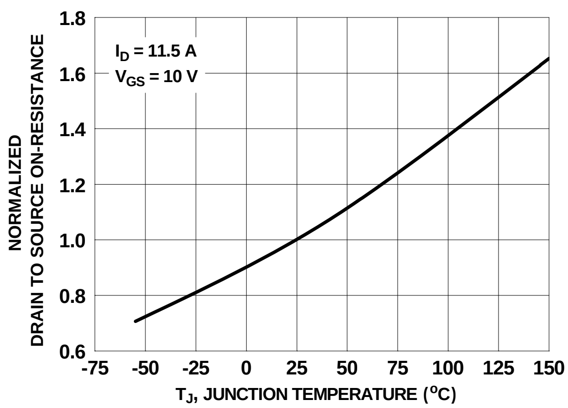


Figure 3. Normalized On Resistance vs Junction Temperature

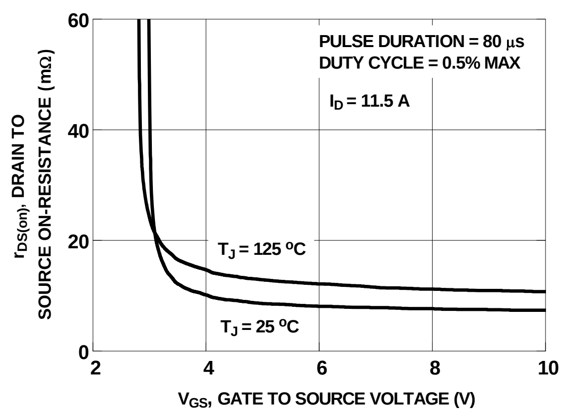


Figure 4. On-Resistance vs Gate to Source Voltage

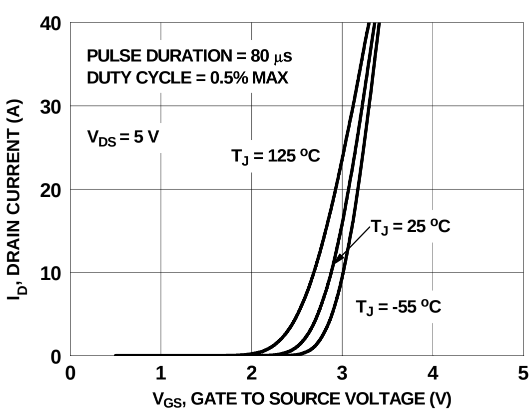


Figure 5. Transfer Characteristics

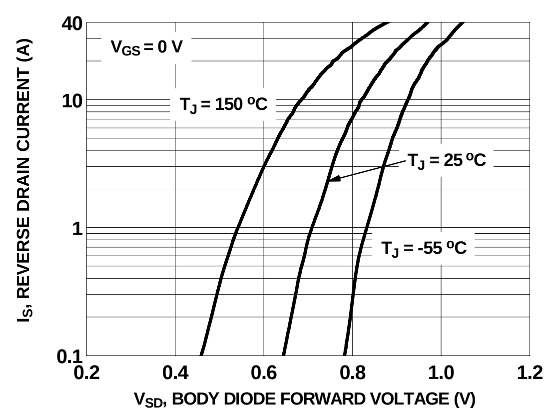


Figure 6. Source to Drain Diode Forward Voltage vs Source Current

Typical Characteristics T_J = 25°C unless otherwise noted

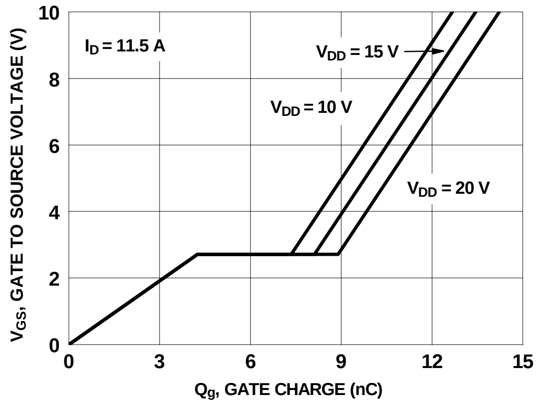


Figure 7. Gate Charge Characteristics

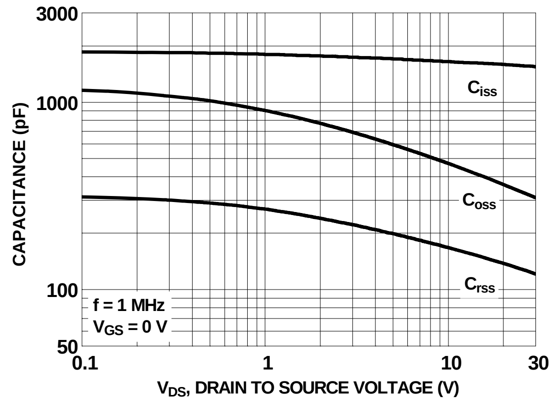


Figure 8. Capacitance vs Drain to Source Voltage

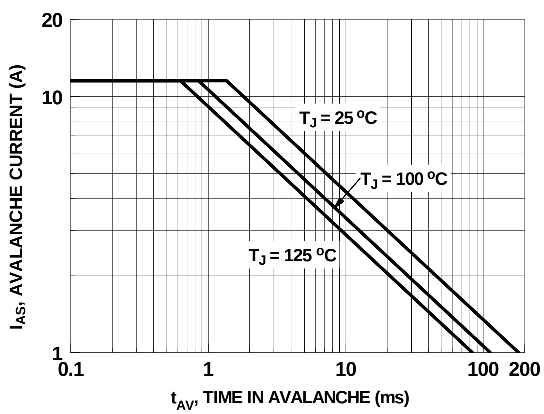


Figure 9. Unclamped Inductive Switching Capability

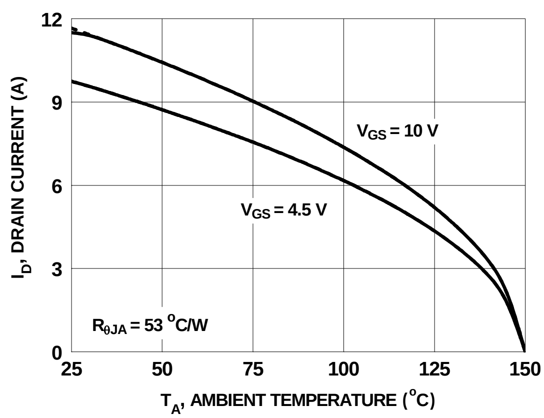


Figure 10. Maximum Continuous Drain Current vs Ambient Temperature

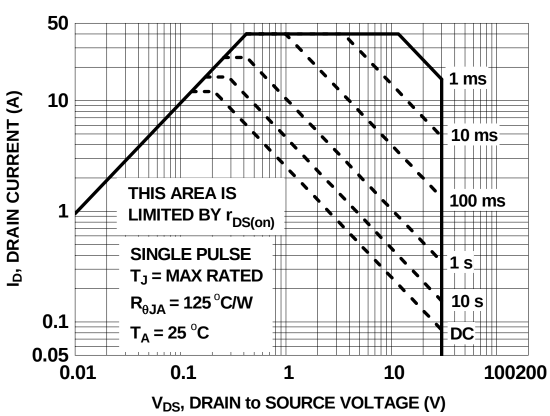


Figure 11. Forward Bias Safe Operating Area

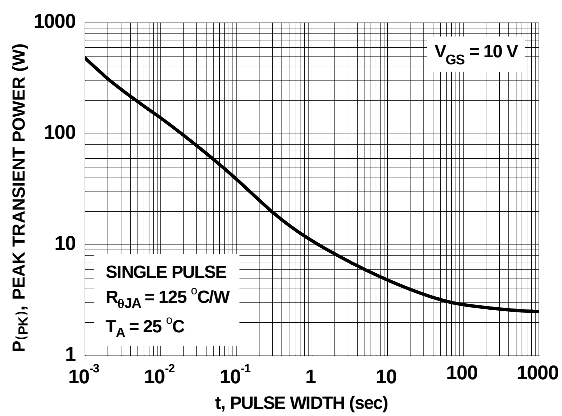


Figure 12. Single Pulse Maximum Power Dissipation

Typical Characteristics T_J = 25°C unless otherwise noted

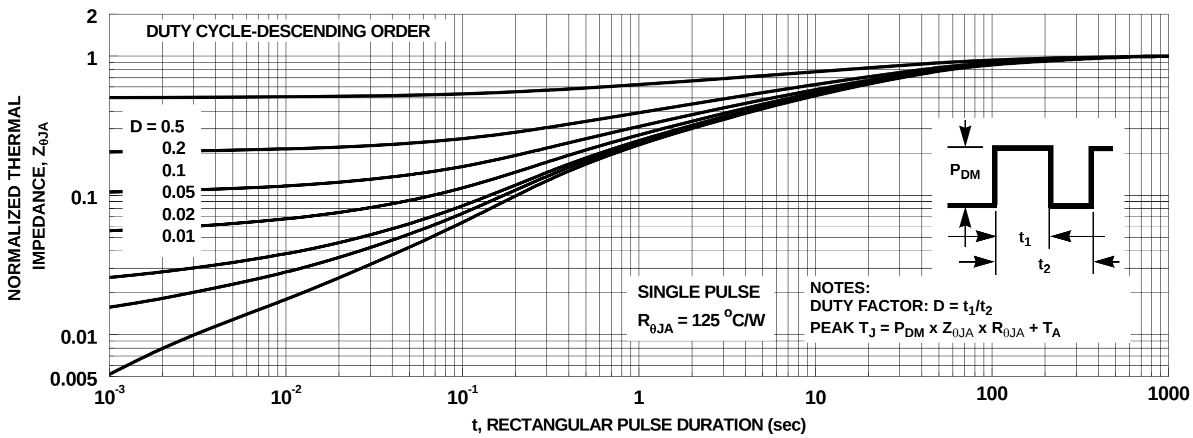
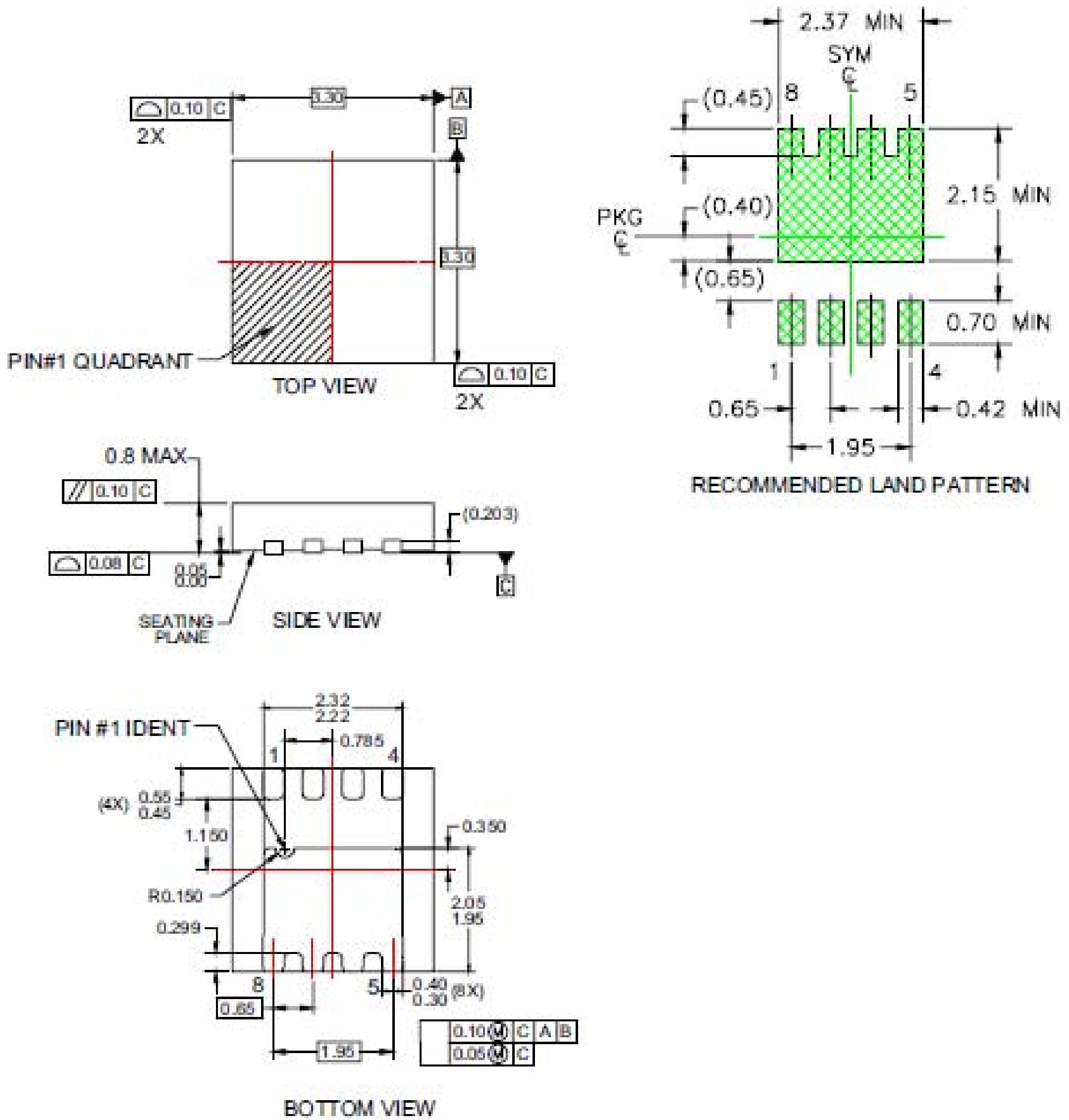


Figure 13. Junction-to-Ambient Transient Thermal Response Curve

Dimensional Outline and Pad Layout



NOTES:

A. DOES NOT CONFORM TO JEDEC REGISTRATION MO-229

B. DIMENSIONS ARE IN MILLIMETERS.

C. DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 1994

D. DRAWING FILE NAME : MLP08SREVA

E. LAND PATTERN RECOMMENDATION IS BASED ON FSC DESIGN ONLY

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Rev. I51