# FUJITSU

=== DATA SHEET ===

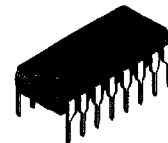# MB87001A
# CMOS PLL FREQUENCY SYNTHESIZER

## CMOS SERIAL INPUT PHASE-LOCKED-LOOP (PLL) FREQUENCY SYNTHESIZER

The Fujitsu MB87001A, fabricated in CMOS technology, is a serial input PLL frequency synthesizer.
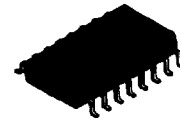
The MB87001A contains an inverter for connection to an external oscillator, a programmable reference divider, a divide factor of programmable reference divider control circuit, a phase detector, a charge pump, a 17-bit shift register, a 17-bit latch, a programmable divider (a binary 7-bit swallow counter, a binary 10-bit programmable counter), and a control generator for an external dual modulus prescaler.

When supplemented with a loop filter and VCO, the MB87001A contains the necessary circuitry to make up a Phase Locked Loop (PLL). Typically, a dual modulus prescaler such as the MB501L can be added, allowing input frequency operation up to 1.1 GHz.

**PLASTIC PACKAGE**
**DIP-16P-M04**

**PLASTIC PACKAGE**
**FPT-16P-M06**

- Single power supply voltage:
  $V_{DD} = 2.7V$ to 5.5V

- Wide temperature range:
  $T_A = -40$ to 85°C

- 13MHz typical input capability
  @5V (fin input)

- On-chip inverter for oscillator

- 8 divide factors for programmable reference divider is selected by $S_1$.

- $S_2$ and $S_3$ input (1/8, 1/16, 1/64, 1/128, 1/256, 1/512, 1/1024, 1/2048)

- Programmable 17-bit divider with input amplifier consisting of:
  Binary 7-bit swallow counter
  Binary 10-bit programmable counter

- 2 type of phase detector output
  On-chip charge pump output
  Output for external charge pump

- Easy interface to Fujitsu dual modulus prescaler

## PIN ASSIGNMENT

| | | | |
|---|---|---|---|
| $V_{DD}$ | 1 | 16 | $V_{SS}$ |
| Clock | 2 | 15 | $OSC_{IN}$ |
| Data | 3 | 14 | $OSC_{OUT}$ |
| LE | 4 | 13 | $S_3$ |
| fin | 5 | 12 | $S_2$ |
| M | 6 | 11 | $S_1$ |
| LD | 7 | 10 | $\phi P$ |
| $D_0$ | 8 | 9 | $\phi R$ |

TOP VIEW

## ABSOLUTE MAXIMUM RATINGS (see NOTE)          ($V_{SS} = 0V$)

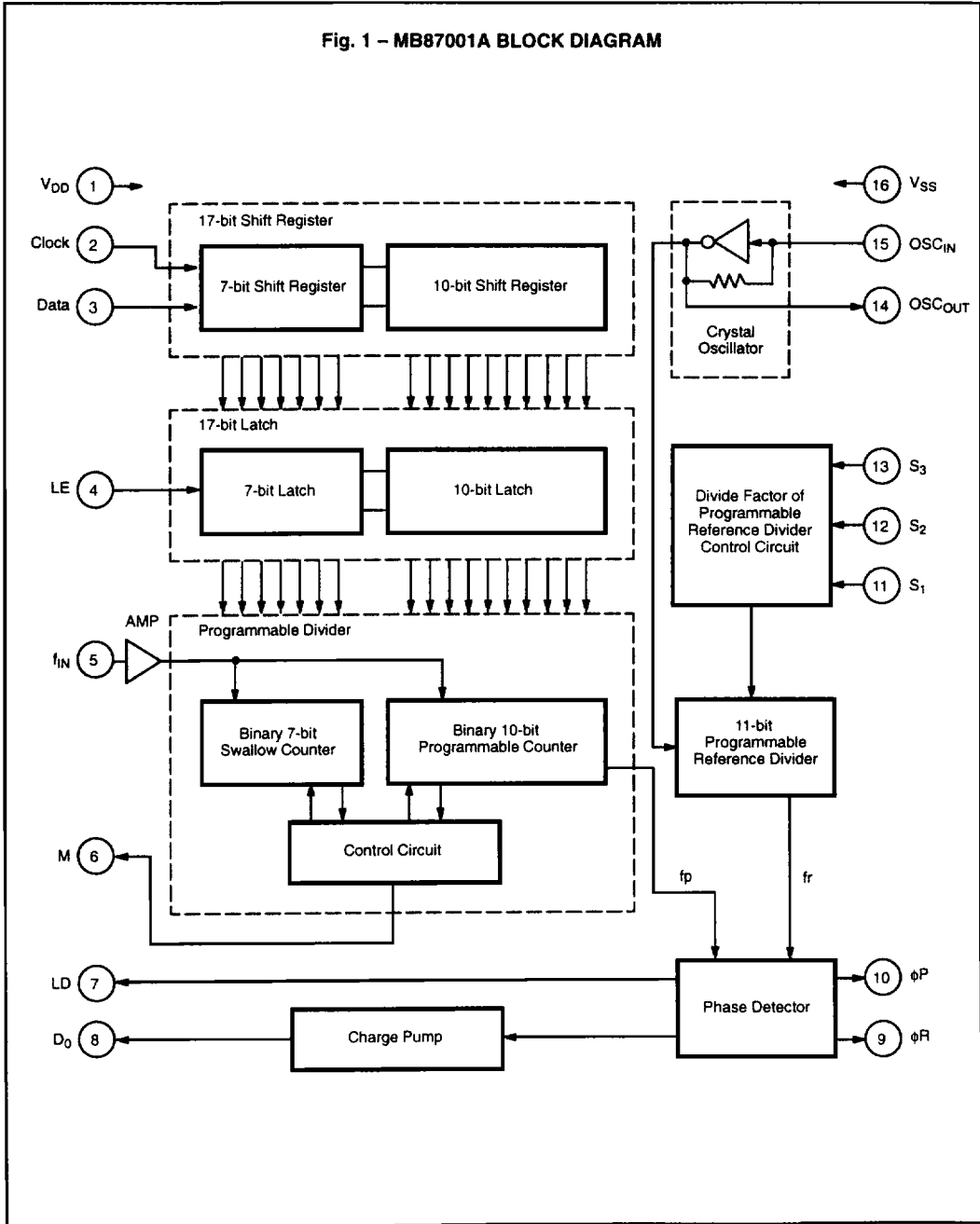| Rating | Symbol | Value | Unit |
|---|---|---|---|
| Power Supply Voltage | $V_{DD}$ | $V_{SS} -0.5$ to $V_{SS} +7.0$ | V |
| Input Voltage | $V_{IN}$ | $V_{SS} -0.5$ to $V_{DD} +0.5$ | V |
| Output Voltage | $V_{OUT}$ | $V_{SS} -0.5$ to $V_{DD} +0.5$ | V |
| Output Current | $I_{OUT}$ | $\pm10$ | mA |
| Open-drain Output | $V_{OOP}$ | $V_{SS}-0.5$ to $V_{DD} +3.0$ | V |
| Operating Temperature | $T_A$ | $-40$ to $+85$ | °C |
| Storage Temperature | $T_{STG}$ | $-65$ to $+150$ | °C |
| Power Dissipation | $P_D$ | 300 | mW |

**NOTE:** Permanent device damage may occur if the above **Absolute Maximum Ratings** are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
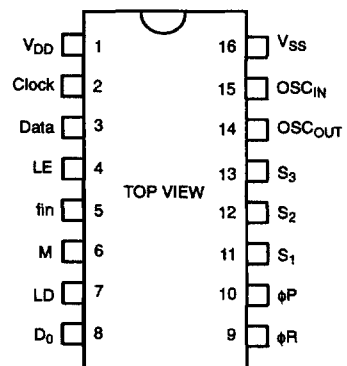
# Fig. 1 – MB87001A BLOCK DIAGRAM

$V_{DD}$ (1) →

(16) $V_{SS}$

**17-bit Shift Register**

Clock (2)

(15) $OSC_{IN}$

| 7-bit Shift Register | 10-bit Shift Register |

Data (3)

(14) $OSC_{OUT}$

Crystal Oscillator

**17-bit Latch**

LE (4)

| 7-bit Latch | 10-bit Latch |

(13) $S_3$

Divide Factor of Programmable Reference Divider Control Circuit

(12) $S_2$

(11) $S_1$

AMP

**Programmable Divider**

$f_{IN}$ (5)

| Binary 7-bit Swallow Counter | Binary 10-bit Programmable Counter |

11-bit Programmable Reference Divider

Control Circuit

M (6)

fp

fr

LD (7)

(10) $\phi P$

Phase Detector

$D_O$ (8)

Charge Pump

(9) $\phi R$

# PIN DESCRIPTION

| Pin No. | Pin Name | I/O | Description |
|---------|----------|-----|-------------|
| 1 | $V_{DD}$ | – | Power supply voltage input |
| 2 | Clock | I | Clock signal input for 17-bit shift register<br>Each rising edge of the clock shifts one bit of the data into the shift register |
| 3 | Data | I | Serial data input for 17-bit shift register<br>The data is used for setting the divide factor of the programmable divider |
| 4 | LE | I | Load enable input<br>When this pin is high level (high active), the data stored in the 17-bit shift register is transferred to the 17-bit latch. |
| 5 | $f_{IN}$ | I | Input for programmable divider from VCO or prescaler output<br>This input involves the bias circuit and amplifier. The connection with the external dual modulus prescaler should be an AC connection. |
| 6 | M | O | Control output for external dual modulus prescaler<br>The connection to the prescaler should be a DC connection. This output level is synchronized with the falling edge of the $f_{IN}$ input signal (pin #5).<br>Pulse Swallow Function:<br>MB501L  M = High: Preset modulus factor 64 or 128<br>           M = Low: Preset modulus factor 65 or 129 |
| 7 | LD | O | Output of phase detector<br>It is high level when fr and fp are equal, and then the loop is locked. Otherwise it outputs a negative pulse signal. |
| 8 | $D_O$ | O | Three-state charge pump output of the phase detector<br>The mode of $D_O$ is changed by the combination of the programmable reference divider output frequency (fr) and the programmable divider output frequency (fp) as listed below:<br>fr > fp:   Drive mode ($D_O$ = High level)<br>fr = fp:   High-impedance mode<br>fr < fp:   Sink mode ($D_O$ = Low level) |
| 9<br>10 | $\phi R$<br>$\phi P$ | O<br>O | Phase detector outputs for an external charge pump<br>The mode of $\phi R$ and $\phi P$ are changed by the combination of the programmable reference divider output frequency (fr) and the programmable divider output frequency (fp) as listed below:<br>        $\phi R$     $\phi P$<br>fr > fp:  Low    Low<br>fr = fp:  Low    High-Impedance<br>fr < fp:  High   High-Impedance<br>* $\phi P$ is a N-channel open drain output |
| 11<br>12<br>13 | $S_1$<br>$S_2$<br>$S_3$ | I<br>I<br>I | Control input for programmable reference divider<br>The combination of these inputs provides 8 kinds of divide factor for the programmable reference divider. |
| 14 | $OSC_{OUT}$ | O | Output pin for crystal oscillator<br>Output of the inverting amplifier<br>This pin should be open when an external oscillator is used. |
| 15 | $OSC_{IN}$ | I | Input pin for crystal oscillator.<br>Input to the inverting amplifier that forms part of the oscillator<br>This pin receives the oscillator signal as AC coupled when an external oscillator is used.<br>For large amplitude signals (standard CMOS levels) DC coupling may also be used. |
| 16 | $V_{SS}$ | – | Ground |

Table for pins 11–13:

| Divide Factor / Sn | $\frac{1}{8}$ | $\frac{1}{16}$ | $\frac{1}{64}$ | $\frac{1}{128}$ | $\frac{1}{256}$ | $\frac{1}{512}$ | $\frac{1}{1024}$ | $\frac{1}{2048}$ |
|---|---|---|---|---|---|---|---|---|
| $S_1$ | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 |
| $S_2$ | 0 | 0 | 1 | 1 | 0 | 0 | 1 | 1 |
| $S_3$ | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 |

# FUNCTIONAL DESCRIPTION

### DIVIDE FACTOR OF PROGRAMMABLE DIVIDER

Serial data of binary code is input to the Data pin. These data are loaded into the 17-bit shift register from the MSB. When the load enable signal (LE) is high, the data stored in the 17-bit shift register is transferred to the 17-bit latch.

The data ① to ⑦ set a divide factor of the binary 7-bit swallow counter and data ⑧ to ⑰ set a divide factor of the binary 10-bit programmable counter. In other words, serial data is equivalent to the divide factor of programmable divider.

## Fig. 2 – BLOCK DIAGRAM OF PROGRAMMABLE DIVIDER
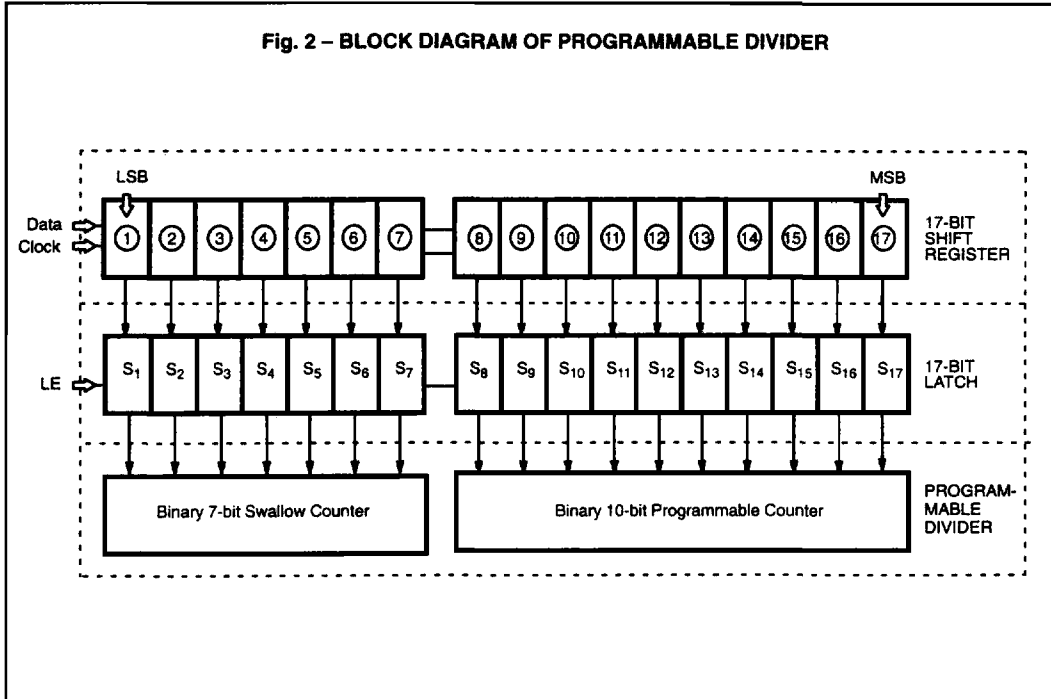
## Binary 7-bit Swallow Counter Data Input

| ⑦ | ⑥ | ⑤ | ④ | ③ | ② | ① | Divide Factor A |
|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 |
| 0 | 0 | 0 | 0 | 0 | 1 | 0 | 2 |
| 0 | 0 | 0 | 0 | 0 | 1 | 1 | 3 |
| 0 | 0 | 0 | 0 | 1 | 0 | 0 | 4 |
| . | . | . | . | . | . | . | . |
| 1 | 1 | 1 | 1 | 1 | 1 | 1 | 127 |

**Note:** Divide factor A: 0 to 127
Depending upon the divide factor set input (SW) of external prescaler, the input data should be as follows:
Example MB501L
SW = H (64/65): Bit 7 of shift register (7) should be zero

## Binary 10-bit Programmable Counter Data Input

| ⑰ | ⑯ | ⑮ | ⑭ | ⑬ | ⑫ | ⑪ | ⑩ | ⑨ | ⑧ | Divide Factor N |
|---|---|---|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 1 | 5 |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 6 |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 7 |
| . | . | . | . | . | . | . | . | . | . | . |
| 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1023 |

**Note:** Divide factor less than 5 is prohibited
Divide factor N: 5 to 1023

## PULSE SWALLOW FUNCTION

$$f_{VCO} = [(N \times M) + A] \times fr$$

$f_{VCO}$ : Output frequency of external voltage controlled oscillator (VCO)

N : Preset divide factor of binary 10-bit programmable counter (5 to 1023)

M : Preset modulus factor of external dual modulus prescaler (e.g. 64 in 64/65 mode, 128 in 128/129 mode of an MB501L prescaler)

A : Preset divide factor of binary 7-bit swallow counter (0 to 127)

fr : Output frequency of the programmable reference divider

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**TIMING CHART**

• $t_1 - t_5 \geq 1\mu s$,

Data | $S_{17} = MSB$ | $S_{16}$ | $S_{15}$ | $S_8$ | $S_7$ | $S_3$ | $S_2$ | $S_1 = LSB$

Clock

$t_1$ $t_2$ $t_3$

LE

$t_4$ $t_5$

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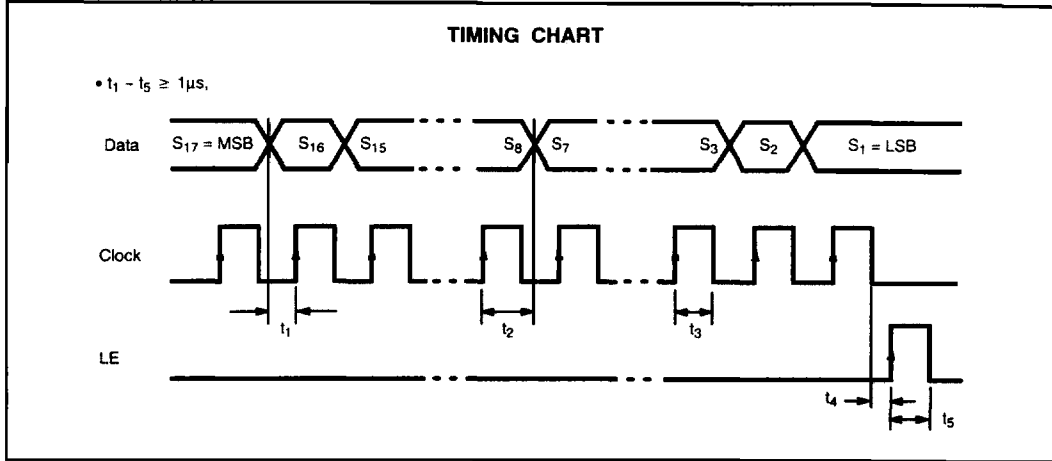
Clock : Clock signal input for the 17-bit shift register
Each rising edge of the clock shifts one bit of data into the shift register.

Data : Serial data input for the 17-bit shift register

LE : Load enable input
When LE is high (high active), the data stored in the 17-bit shift register is transferred to the 17-bit latch.
The 17-bit data is used for setting a divide factor of the programmable divider.

# RECOMMENDED OPERATING CONDITIONS

$(V_{SS} = 0V)$

| Parameter | Symbol | Value | | | Unit |
|---|---|---|---|---|---|
| | | Min | Typ | Max | |
| Power Supply Voltage | $V_{DD}$ | 2.7 | – | 5.5 | V |
| Input Voltage | $V_{IN}$ | $V_{SS}$ | – | $V_{DD}$ | V |
| Operating Temperature | $T_A$ | –40 | – | +85 | °C |

## HANDLING PRECAUTIONS

• This device should be transported and stored in anti-static containers.

• This is a static-sensitive device; take proper anti-ESD precautions. Ensure that personnel and equipment are properly grounded. Cover work-benches with grounded conductive mats.

• Always turn the power supply off before inserting or removing the device from its socket.

• Protect leads with a conductive sheet when handling or transporting PC boards with devices.

# ELECTRICAL CHARACTERISTICS

$(V_{DD} = 3.0V, V_{SS} = 0V, T_A = -40 \text{ to } +85°C)$

| Parameter | | Symbol | Condition | Value | | | Unit |
|---|---|---|---|---|---|---|---|
| | | | | Min | Typ | Max | |
| High-level Input Voltage | Except $f_{IN}$ and $OSC_{IN}$ | $V_{IH}$ | — | 2.1 | — | — | V |
| Low-level Input Voltage | | $V_{IL}$ | — | — | — | 0.9 | |
| Input Sensitivity | $f_{IN}$ | $Vf_{IN}$ | Amplitude in AC coupling, sine wave | 0.8 | — | — | $V_{P-P}$ |
| | $OCS_{IN}$ | $V_{OSC}$ | | 1.0 | — | — | |
| High-level Input Current | Except $f_{IN}$ and $OSC_{IN}$ | $I_{IH}$ | $V_{IN} = V_{DD}$ | — | 1.0 | — | μA |
| Low-level Input Current | | $I_{IL}$ | $V_{IN} = V_{SS}$ | — | −1.0 | — | |
| Input Current | $f_{IN}$ | $If_{IN}$ | $V_{IN} = V_{SS}$ to $V_{DD}$ | — | ±30 | — | μA |
| | $OCS_{IN}$ | $I_{OSC}$ | | — | ±30 | — | |
| High-level Output Voltage | Except $\phi P$ and $OSC_{OUT}$ | $V_{OH}$ | $I_{OH} = 0\mu A$ | 2.95 | — | — | V |
| Low-level Output Voltage | | $V_{OL}$ | $I_{OL} = 0\mu A$ | — | — | 0.05 | |
| Low-level Output Voltage | $\phi P$ | $V_{OLP}$ | $I_{OL} = 0.8mA$ | — | — | 0.8 | |
| High-level Output Voltage | $OSC_{OUT}$ | $V_{OHX}$ | $I_{OH} = 0\mu A$ | 2.50 | — | — | V |
| Low-level Output Voltage | | $V_{OLX}$ | $I_{OL} = 0\mu A$ | — | — | 0.50 | |
| High-level Output Current | Except $\phi P$ and $OSC_{OUT}$ | $I_{OH}$ | $V_{OH} = 2.0V$ | −0.5 | — | — | mA |
| Low-level Output Current | | $I_{OL}$ | $V_{OL} = 0.8V$ | 0.5 | — | — | |
| N-channel Open Drain Cut Off Current | $\phi P$ | $I_{OFF}$ | $V_O = V_{DD} +3.0V$ | — | 1.0 | — | μA |
| Power Supply Current[*1] | | $I_{DD}$ | — | — | 2.0 | — | mA |
| Max. Operating Frequency of Programmable Reference Divider | | fMAXd | — | 13 | 20 | — | MHz |
| Max. Operating Frequency of Programmable Divider | | fMAXp | — | 10 | 20 | — | MHz |

Note: *1: $f_{IN} = 5.0MHz$, 12.8MHz crystal is connected between $OSC_{IN}$ and $OSC_{OUT}$.
Inputs are connected to ground except for $f_{IN}$ and $OSC_{IN}$. Outputs are open.
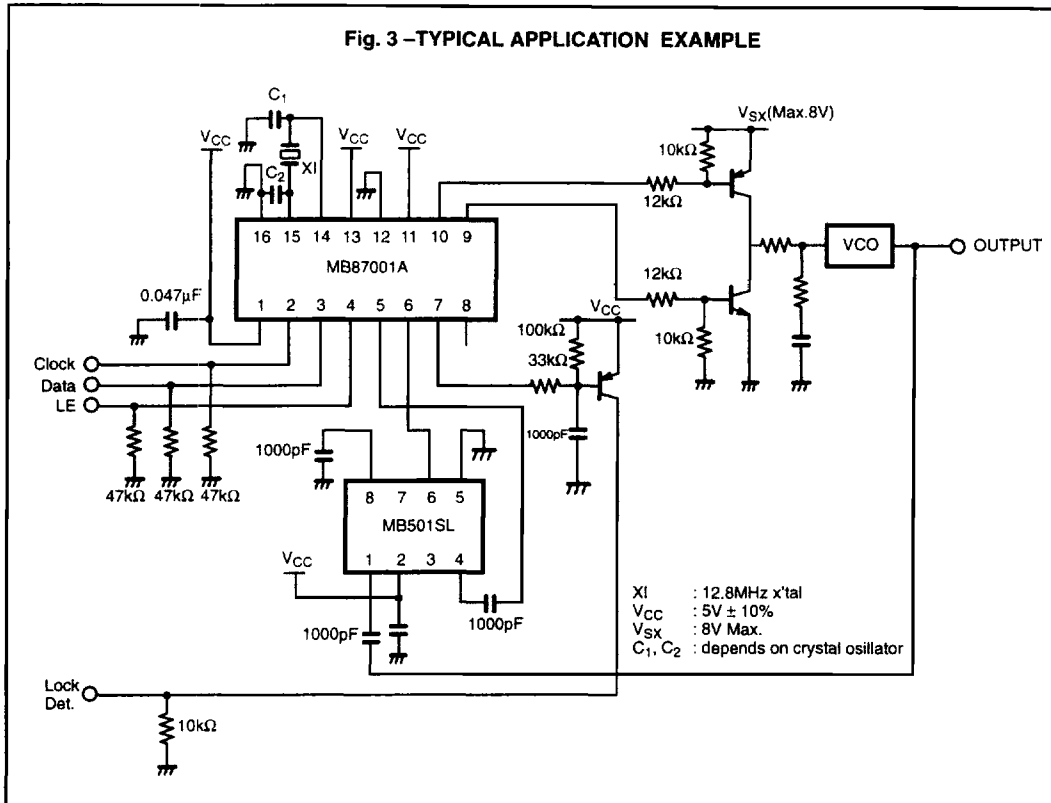
# ELECTRICAL CHARACTERISTICS

$(V_{DD} = 5.0V, V_{SS} = 0V, T_A = -40$ to $+85°C)$

| Parameter | | Symbol | Condition | Value | | | Unit |
|---|---|---|---|---|---|---|---|
| | | | | Min | Typ | Max | |
| High-level Input Voltage | Except $f_{IN}$ and $OSC_{IN}$ | $V_{IH}$ | — | 3.5 | — | — | V |
| Low-level Input Voltage | | $V_{IL}$ | — | — | — | 1.5 | |
| Input Sensitivity | $f_{IN}$ | $Vf_{IN}$ | Amplitude in AC coupling, sine wave | 1.0 | — | — | $V_{P-P}$ |
| | $OCS_{IN}$ | $V_{OSC}$ | | 1.5 | — | — | |
| High-level Input Current | Except $f_{IN}$ and $OSC_{IN}$ | $I_{IH}$ | $V_{IN} = V_{DD}$ | — | 1.0 | — | $\mu A$ |
| Low-level Input Current | | $I_{IL}$ | $V_{IN} = V_{SS}$ | — | -1.0 | — | |
| Input Current | $f_{IN}$ | $If_{IN}$ | $V_{IN} = V_{SS}$ to $V_{DD}$ | — | ±50 | — | $\mu A$ |
| | $OCS_{IN}$ | $I_{OSC}$ | | — | ±50 | — | |
| High-level Output Voltage | Except $\phi P$ and $OSC_{OUT}$ | $V_{OH}$ | $I_{OH} = 0\mu A$ | 4.95 | — | — | V |
| Low-level Output Voltage | | $V_{OL}$ | $I_{OL} = 0\mu A$ | — | — | 0.05 | |
| Low-level Output Voltage | $\phi P$ | $V_{OLP}$ | $I_{OL} = 0.8mA$ | — | — | 1.0 | |
| High-level Output Voltage | $OSC_{OUT}$ | $V_{OHX}$ | $I_{OH} = 0\mu A$ | 4.50 | — | — | V |
| Low-level Output Voltage | | $V_{OLX}$ | $I_{OL} = 0\mu A$ | — | — | 0.50 | |
| High-level Output Current | Except $\phi P$ and $OSC_{OUT}$ | $I_{OH}$ | $V_{OH} = 2.0V$ | -1.0 | — | — | mA |
| Low-level Output Current | | $I_{OL}$ | $V_{OL} = 0.8V$ | 1.0 | — | — | |
| N-channel Open Drain Cut Off Current | $\phi P$ | $I_{OFF}$ | $V_O = V_{DD} +3.0V$ | — | 1.0 | — | $\mu A$ |
| Power Supply Current[1] | | $I_{DD}$ | — | — | 2.0 | — | mA |
| Max. Operating Frequency of Programmable Reference Divider | | fMAXd | — | 15 | 25 | — | MHz |
| Max. Operating Frequency of Programmable Divider | | fMAXp | — | 13 | 25 | — | MHz |

**Note:** [1]: $f_{IN} = 5.0MHz$, 12.8MHz crystal is connected between $OSC_{IN}$ and $OSC_{OUT}$.
Inputs are connected to ground except for $f_{IN}$ and $OSC_{IN}$. Outputs are open.

## Fig. 3 – TYPICAL APPLICATION EXAMPLE



XI : 12.8MHz x'tal
$V_{CC}$ : 5V ± 10%
$V_{SX}$ : 8V Max.
$C_1, C_2$ : depends on crystal osillator
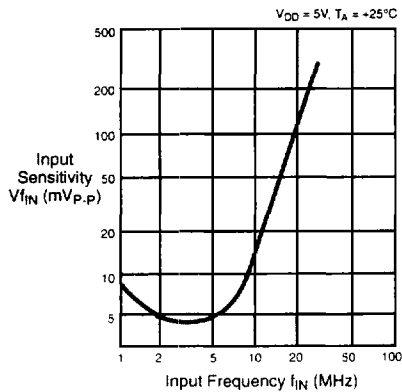
# TYPICAL CHARACTERISTICS CURVES

**Inupt Sensitivity vs. Input Frequency (fin Section)**



**Power Supply Current vs. Input Frequency**

# PACKAGE DIMENSIONS

## 16-LEAD PLASTIC DUAL IN-LINE PACKAGE
### (CASE No.: DIP-16P-M04)

INDEX-1

INDEX-2

.770 +.008 -.012 (19.55 +0.20 -0.30)

15°MAX

.244±.010
(6.20±0.25)

.300(7.62)
TYP

.039 +.012 -0
(0.99 +0.30 -0)

.060 +.012 -0
(1.52 +0.30 -0)

.010 ± .002
(0.25 ± 0.05)

.172(4.36)MAX

.118(3.00)MIN

.100(2.54)
TYP

.050(1.27)
MAX

.018 ± .003
(0.46 ± 0 08)

.020(0.51)MIN

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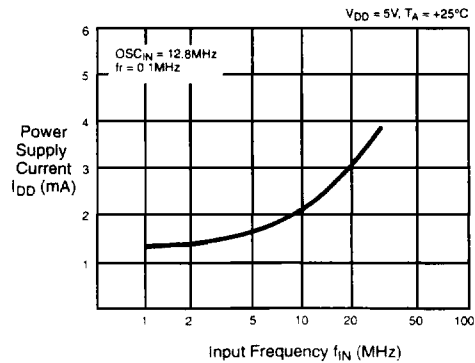
Dimensions in
inches (millimeters)
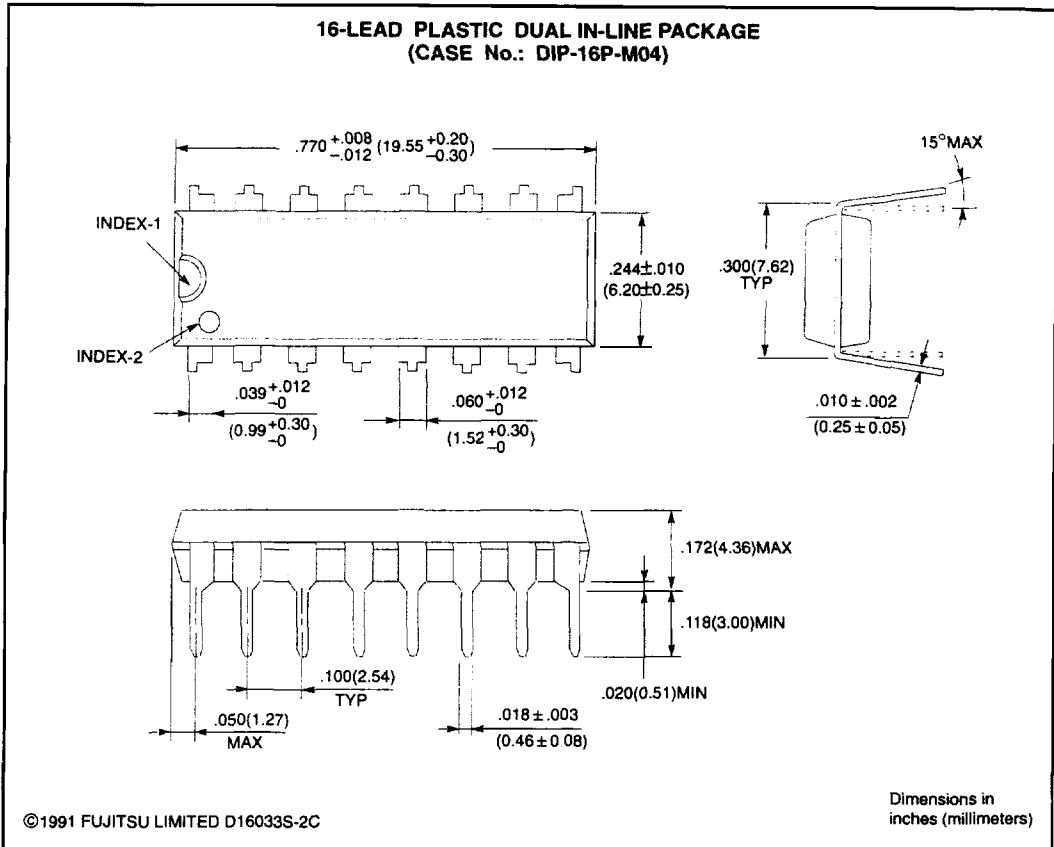
# PACKAGE DIMENSIONS (Continued)

## 16-LEAD PLASTIC FLAT PACKAGE
## (CASE No.: FPT-16P-M06)

.400 $^{+.010}_{-.008}$ (10.15 $^{+0.25}_{-0.20}$ )

INDEX

"B"

.307±.016
(7.80±0.40)

.209±.012
(5.30±0.30)

.050(1.27)
TYP

.018±.004
(0.45±0.10)

$\bigoplus$ Ø.005(0.13) Ⓜ

.089(2.25)MAX
(MOUNTING HEIGHT)

.002(0.05)MIN
(STAND OFF HEIGHT)

.268 $^{+.016}_{-.008}$ (6.80 $^{+0.40}_{-0.20}$ )

.020±.008
(0.50±0.20)

.006 $^{+.002}_{-.001}$ (0.15 $^{+0.05}_{-0.02}$ )

"A"

.004(0.10)

.350(8.89) REF

Details of "A" part

.016(0.40)

.008(0.20)

.007(0.18)
MAX

.027(0.68)
MAX

Details of "B" part

.006(0.15)

.008(0.20)

.007(0.18)
MAX

.027(0.68)
MAX

Dimensions in
inches (millimeters)