MT3332 GNSS Host-Based Solution Data Sheet

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Document Revision History

Revision	Date	Author	Description
0.01	2011/11/19	Loris Li	Initial version

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1 System Overview

1.1 General descriptions

MT3332 is a high-performance single-chip GPS solution which includes on-chip CMOS RF and digital baseband. It is able to achieve the industry's highest level of sensitivity, accuracy and Time-to-First-Fix (TTFF) with the lowest power consumption in a small-footprint lead-free package. Its small footprint and minimal BOM requirement provide significant reductions in the design, manufacturing and testing resource required for portable applications.

With built-in LNA to reach total NF to TBD dB, you can eliminate antenna requirement and do not need external LNA. With its on-chip image-rejection mixer, the spec of external SAW filter is alleviated. With an on-chip automatic center frequency calibration band pass filter, an external filter is not required. The on-chip power management design allows MT3332 to be easily integrated into your system without extra voltage regulator. With both linear and a highly efficient switching type regulator embedded, MT3332 allows direct battery connection and does not need any external LDO, which gives customers plenty of choices for the application circuit.

Up to 12 multi-tone active interference cancellers (ISSCC2011 award) offer you more flexibility in system design. The integrated PLL with Voltage Controlled Oscillator (VCO) provides excellent phase noise performance and fast locking time. A battery backed-up memory and a real-time clock are also provided to accelerate acquisition at the system restart-up.

MT3332 supports up to 210 PRN channels. With 99 search channels and 33 simultaneous tracking channels, MT3332 acquires and tracks satellites in the shortest time even at indoor signal levels. MT3332 supports various location and navigation applications, including autonomous GPS, GLONASS, GALILEO, BEIDOU(after ICD released), SBAS ranging (WAAS, EGNOS, GAGAN, and MSAS), QZSS, DGPS (RTCM) and AGPS.

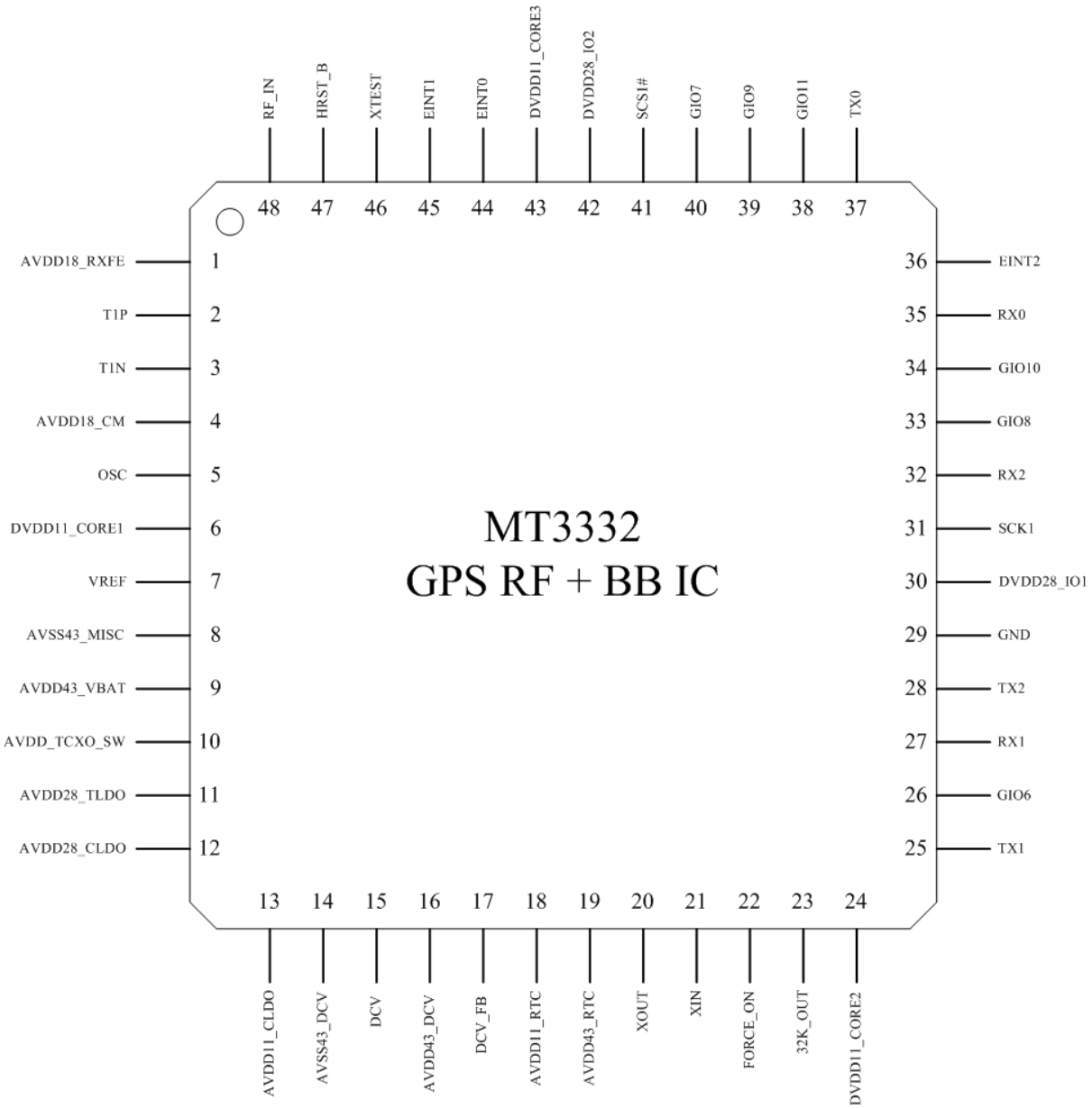
Through MT3332's excellent low-power consumption characteristic (acquisition TBD mW, track TBD mW), power sensitive devices, especially portable applications, you will not need to worry about the operating time anymore and can have more fun. Combined with many advanced features including AlwaysLocate™, EASY™, HotStill™, EPO™ and logger function, MT3332 provides always-on position with minimal average power consumption. The great features provide you supreme experiences for portable applications such as DSC, cellular phone, PMP, and gaming devices.

1.2 Features

- Specifications
  - 33 tracking / 99 acquisition-channel GPS/GLONASS/GALILEO/BEIDOU receiver
  - Supports up to 210 PRN channels
  - Supports multi-GNSS incl. QZSS, SBAS ranging
  - Supports WAAS/EGNOS/MSAS/GAGAN
  - 12 multi-tone active interference cancellers (ISSCC2011 award)
  - RTCM ready
  - Indoor and outdoor multi-path detection and compensation
  - Supports FCC E911 compliance and A-GPS
  - Max. fixed update rate up to 10 Hz
- Advanced software features
  - AlwaysLocate™ advanced location awareness technology
  - EPO™/HotStill™ orbit prediction
- Reference oscillator
  - TCXO
    - Frequency: 16.368 MHz, 12.6 ~ 40.0 MHz
    - Frequency variation: ±2.5 ppm
  - Crystal
    - Frequency: 26 MHz, 12.6 ~ 40.0 MHz
    - Frequency accuracy: ±10 ppm
- RF configuration
  - SoC, integrated in single chip with CMOS process
- Pulse-per-second (PPS) GPS time reference
  - Adjustable duty cycle
  - Typical accuracy: ±10 ns
- Power scheme
  - A 1.8 volts SMPS build-in SOC
  - Direct lithium battery connection (2.8 ~ 4.3 volts)
  - Self build 1.1 volts RTC LDO, 1.1 volts core LDO, and 2.8 volts TCXO LDO
- Build-in reset controller
  - Does not need of external reset control IC
- Internal real-time clock (RTC)
  - 32.768 KHz ± 20 ppm crystal
  - 1.1 volts RTC clock output
  - Supports external pin to wake up MT3332
- Serial interface
  - 3 UARTs
  - SPI
  - I2C
  - GPIO interface (up to 16 pins)
- Superior sensitivities
  - Acquisition: -148 dBm (cold) / -163 dBm (hot)
  - Tracking: -165 dBm
- Ultra-low power consumption (GPS only / GPS+GLONASS)
  - Acquisition: TBD/TBD mW
  - Tracking: TBD/TBD mW
  - AlwaysLocate™: TBD/TBD mW
- Package
  - QFN: 6mm x 6mm, 48 ball
- Slim hardware design
  - 9 passive external components
  - Single RF Front-End for Multi-GNSS frequency bands
- Compatibility
  - Pin-to-pin compatible to MT3336

2 Pin Assignment and Descriptions

2.1 Pin assignment (top view)



2.2 Pin descriptions

Pin#	Symbol	Type	Description
System interface (2 pins)			
47	HRST_B	2.8V LVTTL input default pull-up, SMT	System reset. Active low
46	XTEST	2.8V LVTTL input default pull-down, SMT	Test mode. *Must keep low in normal mode.*
Peripheral interface (8 pins)			
35	RX0/MM_I2CC/H_SPI_SI	2.8V, LVTTL I/O PPU, PPD, SMT 4mA, 8mA, 12mA, 16mA PDR	Serial input for UART 0 Default: pull-up Default: 8mA driving
37	TX0/MM_I2CD/H_SPI_SO	2.8V, LVTTL I/O PPU, PPD, SMT 4mA, 8mA, 12mA, 16mA PDR	Serial output for UART 0 Default: pull-up Default: 8mA driving
27	RX1/H_SPI_SCK/CTS0/MM_I2CC/CXO_TSENS/GIO0	2.8V, LVTTL I/O PPU, PPD, SMT 4mA, 8mA, 12mA, 16mA PDR	Serial input for UART 1 Default: pull-up Default: 8mA driving
25	TX1/TXIND/RTS0/MM_I2CD/CXO_CS/GIO1	2.8V, LVTTL I/O PPU, PPD, SMT 4mA, 8mA, 12mA, 16mA PDR	Serial output for UART 1 Default: pull-up Default: 8mA driving
32	RX2/SPI_SI/JDI/DBG_RX/BSI_CK/GIO2	2.8V, LVTTL I/O PPU, PPD, SMT 4mA, 8mA, 12mA, 16mA PDR	Serial input for UART 2 Default: pull-up Default: 8mA driving
28	TX2/SPI_SO/DBG_TX/GIO3	2.8V, LVTTL I/O PPU, PPD, SMT 4mA, 8mA, 12mA, 16mA PDR	Serial output for UART 2 Default: pull-up Default: 8mA driving Strap pin tcxo_sw_sel 1'b0: AVDD_TCXO_SW output 1.8V 1'b1: AVDD_TCXO_SW output 2.8V
31	SCK1/SPI_SCK/GIO4	2.8V, LVTTL I/O PPU, PPD, SMT 4mA, 8mA, 12mA, 16mA PDR	SPI clock output Default: pull-up Default: 8mA driving Strap pin clk_sel[0] **Clk_sel[1:0] Mode** 2'b00: XTAL mode 2'b01: External clock mode 2'b10: TCXO mode 2'b11: 16.368MHz TCXO mode

Pin#	Symbol	Type	Description
41	SCS1#/SPI_SCS#/BSI_DATA/SYNC_PULSE/GIO5	2.8V, LVTTL I/O PPU, PPD, SMT 4mA, 8mA, 12mA, 16mA PDR	SPI slave selection 1 Default: pull-up Default: 8mA driving Strap pin clk_sel[1]
Debugging interface (6 pins)			
26	BSI_CK/MM_I2CC/ECLK/GIO6	2.8V, LVTTL I/O PPU, PPD, SMT 4mA, 8mA, 12mA, 16mA PDR	GPIO6 Default: pull-down Default: 8mA driving
40	BSI_CS/MM_I2CD/DUTY_CYCLE/PPS/GIO7	2.8V, LVTTL I/O PPU, PPD, SMT 4mA, 8mA, 12mA, 16mA PDR	GPIO7 Default: pull-down Default: 8mA driving
33	FRAME_SYNC/DBG_RX/GIO8	2.8V, LVTTL I/O PPU, PPD, SMT 4mA, 8mA, 12mA, 16mA PDR	GPIO8. Default: pull-down Default: 8mA driving
39	PPS/DBG_TX/GIO9	2.8V, LVTTL I/O PPU, PPD, SMT 4mA, 8mA, 12mA, 16mA PDR	GPIO9 Default: pull-up Default: 8mA driving Strap pin host_sel[0] **Host_sel[1:0] Interface** 2'b00: I2C 2'b01: UART MEIF 2'b10: SPI 2'b11: UART
34	CXO_CS/GIO10	2.8V, LVTTL I/O PPU, PPD, SMT 4mA, 8mA, 12mA, 16mA PDR	GPIO10 Default: pull-up Default: 8mA driving Strap pin host_sel[1]
38	H_SPI_SCS#/CXO_TSENS/SYNC_PULSE/GIO11	2.8V, LVTTL I/O PPU, PPD, SMT 4mA, 8mA, 12mA, 16mA PDR	GPIO11 Default: pull-up Default: 8mA driving
External system interface (3 pins)			
44	EINT0/MM_I2CC/BSI_CS/GIO12	2.8V, LVTTL I/O PPU, PPD, SMT 4mA, 8mA, 12mA, 16mA PDR	External interrupt 0 Default: pull-down Default: 8mA driving
45	EINT1/MM_I2CD/PPS/BSI_DATA/GIO13	2.8V, LVTTL I/O PPU, PPD, SMT 4mA, 8mA, 12mA, 16mA PDR	External interrupt 1 Default: pull-down Default: 8mA driving
36	EINT2/DBG_RX/PPS/GIO14	2.8V, LVTTL I/O PPU, PPD, SMT 4mA, 8mA, 12mA, 16mA PDR	External interrupt 2 Default: pull-up Default: 8mA driving
RTC interface (6 pins)			

Pin#	Symbol	Type	Description
19	AVDD43_RTC	Analog power	RTC LDO input
18	AVDD11_RTC	Analog power	RTC LDO output
21	XIN	Analog input	RTC 32KHz XTAL input
20	XOUT	Analog output	RTC 32KHz XTAL output
23	32K_OUT/DR_IN	1.2V LVTTL I/O PPU, PPD, SMT 4mA, 8mA, 12mA, 16mA PDR	RTC domain GPIO pin, can be programmed to 32KHz clock output or DR wake-up signal input Default: 75K pull-down Default: 16mA driving
22	FORCE_ON	1.2V LVTTL I/O PPU,PPD, SMT	Force to power on this chip.
RF & analog			
1	AVDD18_RXFE	RF power	1.8V supply for RF core circuits
2	T1P	Analog signal	RF testing signal
3	T1N	Analog signal	RF testing signal
4	AVDD18_CM	RF power	1.8V supply for XTAL OSC, bandgap, Thermal sensor and level shifter
5	OSC	Analog signal	Input for crystal oscillator or TCXO
48	RF_IN	RF signal	LNA RF Input pin
6	DVDD11_CORE1	Digital power	Digital 1.1V core power input
24	DVDD11_CORE2	Digital power	Digital 1.1V core power input
43	DVDD11_CORE3	Digital power	Digital 1.1V core power input
30	DVDD28_IO1	Digital power	Digital 1.8/2.8V IO power input
42	DVDD28_IO2	Digital power	Digital 1.8/2.8V IO power input
29	GND	Digital ground	Digital ground
7	VREF	Analog	Bandgap output pin. Must add 1uF decoupling cap on EVB.
8	AVSS43_MISC	Analog ground	GND pin for buck controller, TCXO LDO and start-up block
9	AVDD43_VBAT	Analog power	TCXO LDO input pin. always be powered by external source. UVLO will detect this PIN to check power status.
10	AVDD_TCXO_SW	Analog power	TCXO power switch output pin
11	AVDD28_TLDO	Analog power	TCXO LDO output pin
12	AVDD28_CLDO	Analog power	Core LDO input pin. Always powered by external source or SMPS
13	AVDD11_CLDO	Analog power	Core LDO output pin
14	AVSS43_DCV	SMPS	SMPS GND pin
15	DCV	SMPS	SMPS output pin
16	AVDD43_DCV	SMPS	SMPS input pin.
17	DCV_FB	SMPS	SMPS feedback pin

Notes:
PPU = Programmable pull-up
PPD = Programmable pull-down
PSR = Programmable slew rate

PDR = Programmable driving

3 Block Diagrams

3.1 Architecture of single-chip receiver

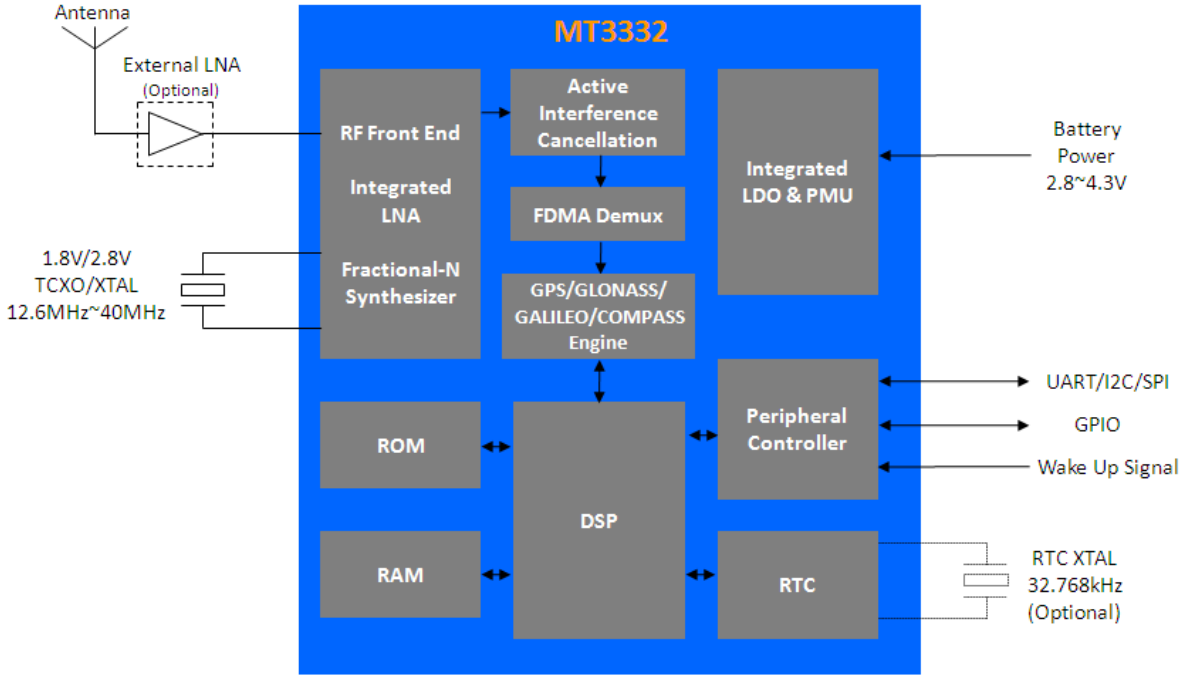


Figure 3-1: MT3332 system block diagram

3.2 Functional block diagram (RF part)

Figure 3-2: MT3332 RF functional block diagram

4 MT3332 RF Part

4.1 LNA/Mixer

Upon receiving RF input signal in through either GPS antenna to internal LNA or external antenna and LNA, the mixer down converts the amplified signal (GPS/Galileo=1575.42MHz, Beidou=1561.098-MHz, GLONASS=1601.71-MHz). The current chip provides 2 configurations to choose from, which are high-gain LNA and low-gain LNA. The high-gain LNA is used for low-cost solution without external LNA. The low-gain LNA offers high linearity to allow high external LNA gain, with much worsen noise figure performance. In the application with external LNA, the external LNA gain ranging from 0 to 20 dB is recommended. The down-conversion mixer is single-ended passive mixer with current mode interface between the mixer and multi-modes low pass filter.

4.2 VCO/Synthesizer

The entire frequency synthesizer includes crystal oscillator, VCO, divider, phase frequency detector (PFD), charge pump (CP) and loop filter which are all integrated on the MT3332 chip. Upon power-on, VCO is auto-calibrated to its required sub-band. The synthesizer adopts fractional-N sigma-delta PLL topology, which supports 12.6 to 40MHz reference clock frequencies.

4.3 LPF

The current-mode LPF supports multiple modes for different GNSS combinations. The LPF also provides 26dB gain-control range, with approximately 2dB per step.

4.4 ADC

The differential IF signal is being quantized by a high performance ADC. The sampling clock can be provided from divided clock from LO. The ADC can be programmed between high performance mode (GPS+GLONASS) for high bandwidth, and low performance mode (GPS-ONLY) for lower current consumption.

5 MT3332 Digital Part

5.1 Boot ROM

The embedded boot ROM provides a function of loading a set of user code through the host interface into SRAM. The host interface (UART/SPI/I2C) is decided by strap control.

5.2 Battery backed-up memory

MT3332 provides very low leakage (about TBD uA in the backup mode) battery backed-up memory, which contains all the necessary GPS information for quick start-up and a small amount of user configuration variables. There is a built-in 1.1 volts LDO for RTC domain and it can be bypassed while an external LDO is applied. The RTC LDO is a voltage regulator having very low quiescent current, and typical quiescent current < TBD uA. The small ceramic capacitor can be used as the output capacitor, and the stable operation region ranges from very light load (~=0) to about TBD mA.

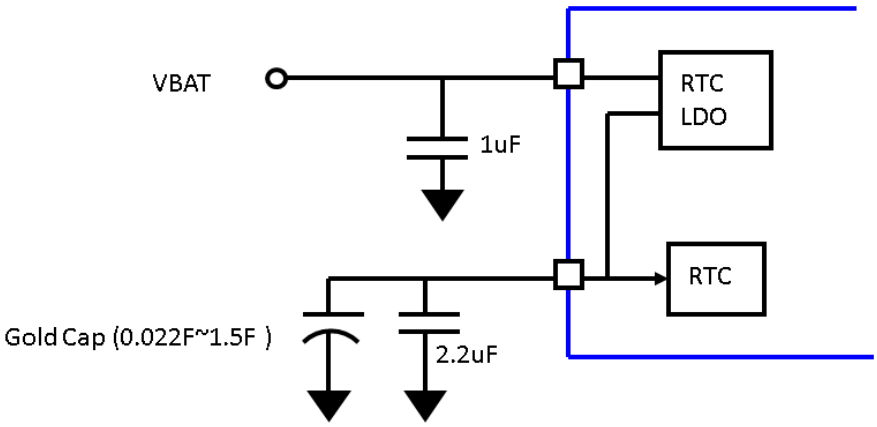


Figure 5-1: RTC with internal RTC LDO application circuit 1

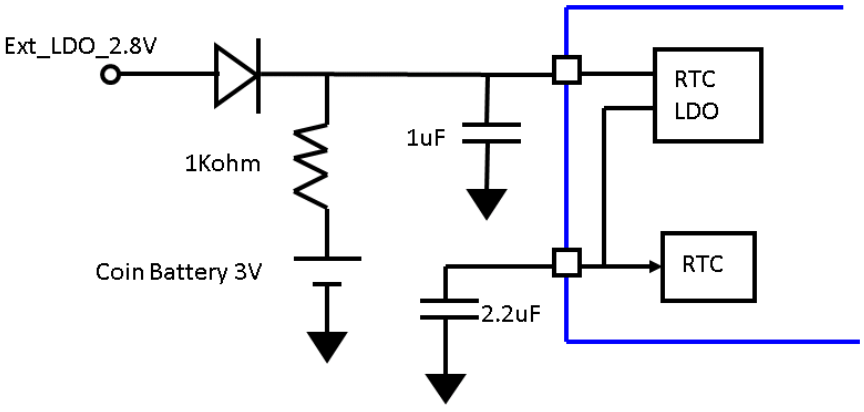


Figure 5-2: RTC with internal RTC LDO application circuit 2

5.3 SMPS

A built-in switching mode power supply provides 1.8 volts power supply for the digital 1.1 volts CLDO and RF input power. In the active mode, SMPS is operated in the PWM mode. In the power saving mode, SMPS is operated with reduced switching frequency in the PFM mode. The recommended L/C value is 1 uH / 4.7 uF.

5.4 Timer function

The timer function supports a time tick generation of 31.25 ms resolution. With the 24-bit counter, the period of timer is from 31.25 ms to 524,287 s.

5.5 GPIO in RTC domain

The “32K_OUT” pin in RTC domain can output 32.768 KHz clock which can be used to support low clock rate operation mode for some applications or peripherals that need an external clock source. This pin can also be programmed to be an input pin to receive the signal from an external accelerator sensor IC to be the wake-up signal of MT3332 when it is in the low-power mode.

5.6 Low power detection

A low power detection circuit is implemented. Whenever the independent power source (AVDD11_RTC) becomes low voltage, the low power detection circuit will detect this condition and use an indicator signal (output high in normal condition and low in low-power condition) to reflect this condition.

5.7 Clock module

The clock module generates all internal clocks required by processor, correlator, internal memory, bus interface and so on. The referenced input clock is generated from the RF block. For system flexibility and maximum power saving, it supports various power management modes.

5.8 Reset controller

The built-in reset controller generates reset signals for all digital blocks. It has power-on reset feature and hardware trapping function. The power-on reset level is 2.7 ± 0.1 volts. The software reset function for different circuit blocks are also included for flexible applications.

In Figure 5-4, the voltage drop time T_{drop_vbat} and T_{drop_cldo} depend on the capacitance connection of their power net. But $T_{drop\_vbat} > T_{drop\_cldo}$ should be guaranteed for the correct operation of reset behavior during power off sequence. It is strongly recommend using external LDOs without output discharged function or make sure $T_{drop\_vbat} > 100$ ms.

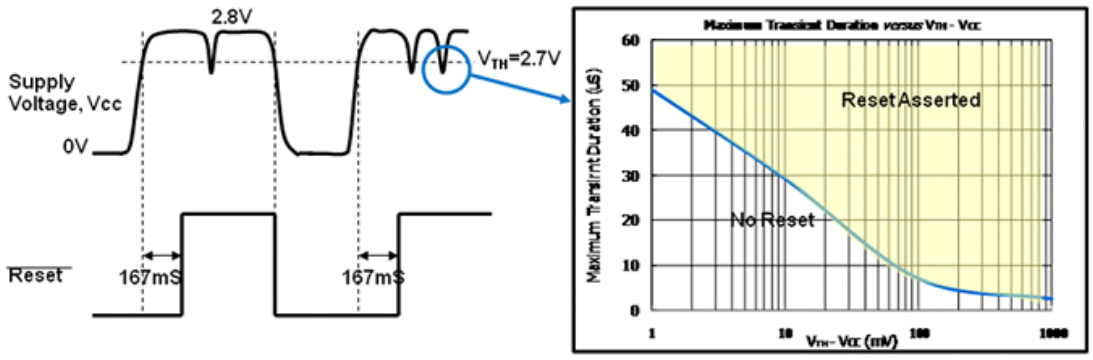


Figure 5-3: Power on reset diagram

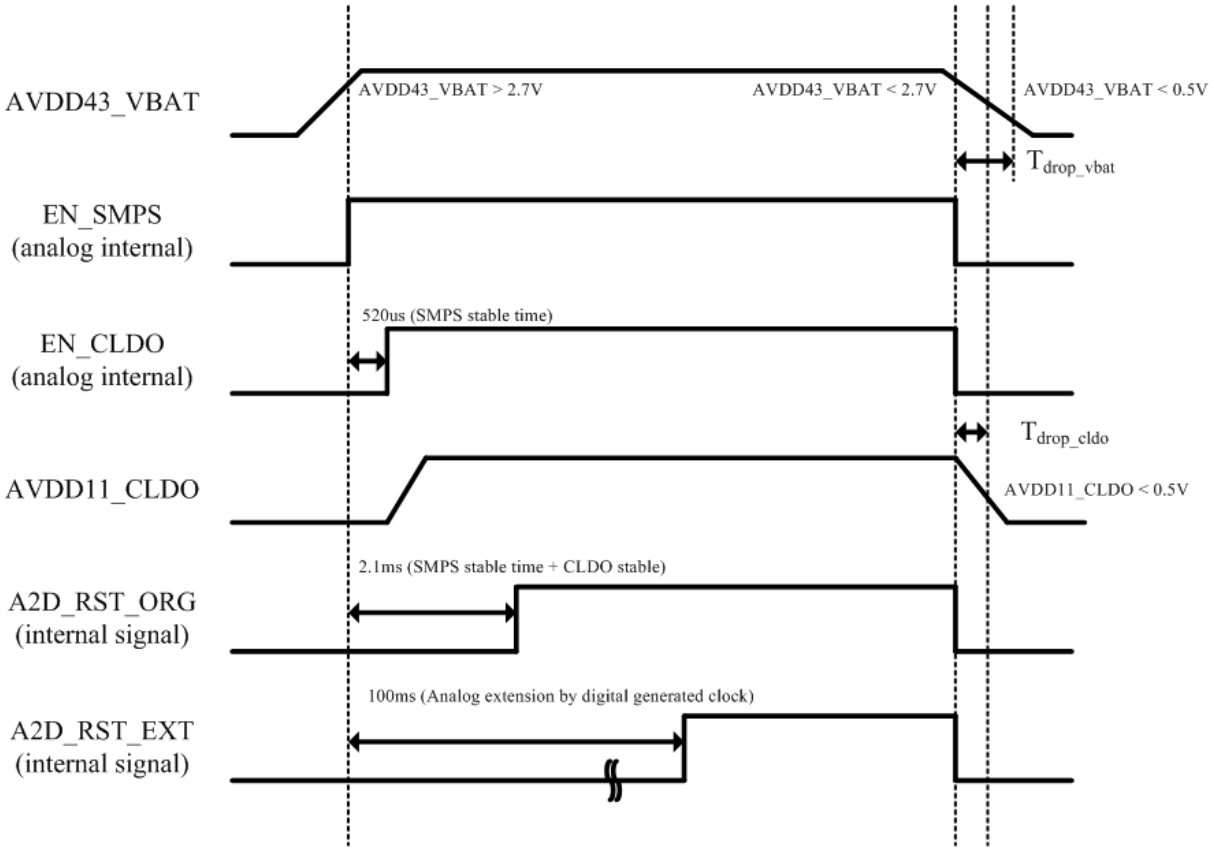


Figure 5-4: Power on/off reset behavior

5.9 Host interface

MT3332 supports 3 different host interfaces, which are UART, SPI, and I2C. The interface used as the host interface is determined by strap pins. Note that SPI and I2C support firmware update only for now.

5.9.1 UART

UART is the abbreviation of “Universal Asynchronous Receiver/Transmitter”. MT3332 has 3 full duplex serial ports. It is used for serial data communication. A UART converts bytes of data to and from asynchronous start-stop bit streams represented as binary electrical impulses.

There are several functions in MT3332 related to UART communication, such as UART data transmission/receive and aiding information input from host processor. In general, UART0 is as measurement data output and PMTK command input, UART1 as RTCM input. You can adjust the UART2 port as desired. The receiver (RX) and transmitter (TX) side of every port contains a 16-byte FIFO, but only UART0 has 256 bytes of URAM. The bit rates are selectable and range from 4.8 to 921.6 kbps. UART provides signal or message outputs.

5.9.2 SPI

The serial peripheral interface port manages the communication between digital BB and external devices. MT3332 supports both master and slave modes. Only 4 bytes of register in the master mode can be transferred. The slave has 4-byte-register mode or URAM mode. In the URAM mode, the transmitted and received data size is 256 bytes. The clock phase and clock polarity are selectable. MT3332 supports manual or automatic indicator for data transfer in the slave mode.

5.9.3 I2C

The I2C interface is mainly connected to external devices. MT3332 supports multi-master and slave modes. Both modes have 256-byte URAM mode and 8-byte FIFO mode for transmitting and receiving data. The multi-master mode supports 7-bit and 10-bit address modes up to 400 Kb/s fast mode and 3.4 Mb/s high-speed mode. In additions, MT3332 supports manual or automatic indicator for data transfer in the slave mode. Device addresses in the slave mode are programmable and support fast mode and high-speed mode data transmission and reception.

5.10 Interrupt control unit

The interrupt control unit manages all internal and external sources of interrupts, which include timer, watch-dog, all interfaces such as UART, I2C and SPI and external user interrupt pins. These interrupt sources can be wake-up events in the power saving mode.

5.11 GPIO unit

GPIO is the abbreviation of “General-Purpose Input/Output”. MT3332 supports a variety of peripherals through maximum 15 GPIO programmable ports. The unit manages all GPIO lines and supports a simple control interface. GPIO provides signal or message outputs.

5.12 PPS

The PPS (Pulse Per Second) signal is provided through designated output pin for many external applications. The pulse is not only limited to being active every second but also allowed to set up the required duration, frequency and active high/low by programming user-defined settings.

5.13 ECLK

ECLK is a clock input pin for introducing an external clock signal to MT3332 and obtaining the relation between the external clock and GPS local clock. With precise external clock input, the clock drift of the GPS local clock can be correctly estimated. Therefore, the Doppler search range is narrowed down accordingly. The technology is beneficial to speeding up the satellite acquisition process. Particularly in the cold start case, due to limited priori information about the satellite's location and local clock uncertainty, a receiver will execute a search in full frequency range. Consequently, a longer acquisition time is expected. However, the ECLK technology is able to reduce the frequency uncertainty so that the search process will be completed in a short time. Efficient acquisition and lower power consumption are attained by the ECLK technology.

5.14 SYNC

SYNC is a time stamp signal input pin for introducing an external timing to the GPS receiver and obtaining the relation between the external timing and the GPS receiver local timing. With precise external timing input and the established relation, the GPS time of week (TOW) can be correctly estimated in the GPS receiver. The technology is beneficial for time to first fix (TTFF), particularly in weak signal environments. In hot starts, with priori information about the GPS receiver's location and satellite ephemeris data, the GPS receiver uses the correct GPS TOW to accurately predict the signal code chip/phase. Therefore, the code search range can be narrowed down accordingly. Hence, fast TTFF is achieved by the SYNC technology.

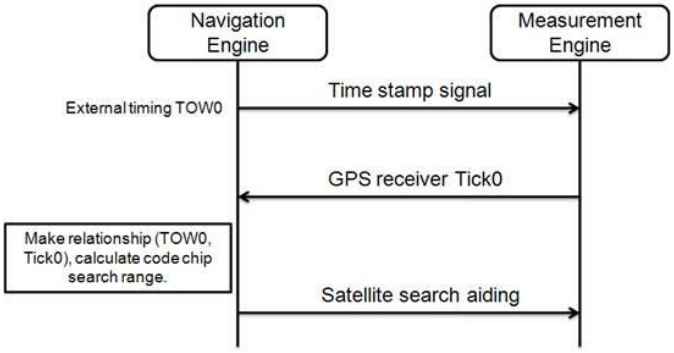


Figure 5-5: Flow diagram of SYNC function

5.15 Power scheme

- Internal SMPS is used as the source power of the internal RF/BB LDO. It is also used as 1.8 volts I/O power. The internal SMPS can switch to the LDO mode to supply power to each of the about block
- External LDO or VBAT can be used as the main power. The minimum/maximum input voltage of AVDD43_VBAT and AVDD43_DCV is 2.8/4.3 volts.
- The power-on reset voltage threshold of AVDD43_VBAT is 2.7 ± 0.1 volts. The maximum TLDO drop out voltage at half load (25 mA) is 0.25 volts. If one external LDO is used to provide power to

MT3332, the 3.3 volts external LDO will be recommended after taking TLDO drop-out into consideration.

- The power efficiency in SMPS mode will be better than that in the internal LDO mode.
- I/O supports 1.8 and 2.8 volts. The power comes from SMPS output for 1.8 volts application or TLDO output (AVDD28_TLDO) for 2.8 volts application.
- TCXO power is from AVDD_TCXO_SW with an internal MUX to select 2.8 volts from AVDD28_TLDO or 1.8 volts from AVDD28_CLDO by setting up power-on strap.
- RTC LDO input power comes from AVDD28_TLDO and uses coin battery as the backup battery. A schottky diode is usually used to avoid leakage from coin battery to TLDO.
- Here are 3 power schemes: low power (Figure 5-6), low cost (Figure 5-7) and external PMU (Figure 5-8).
- In Figure 5-8, if 2.8V TCXO is used, AVDD28_CLDO should be open for saving power.

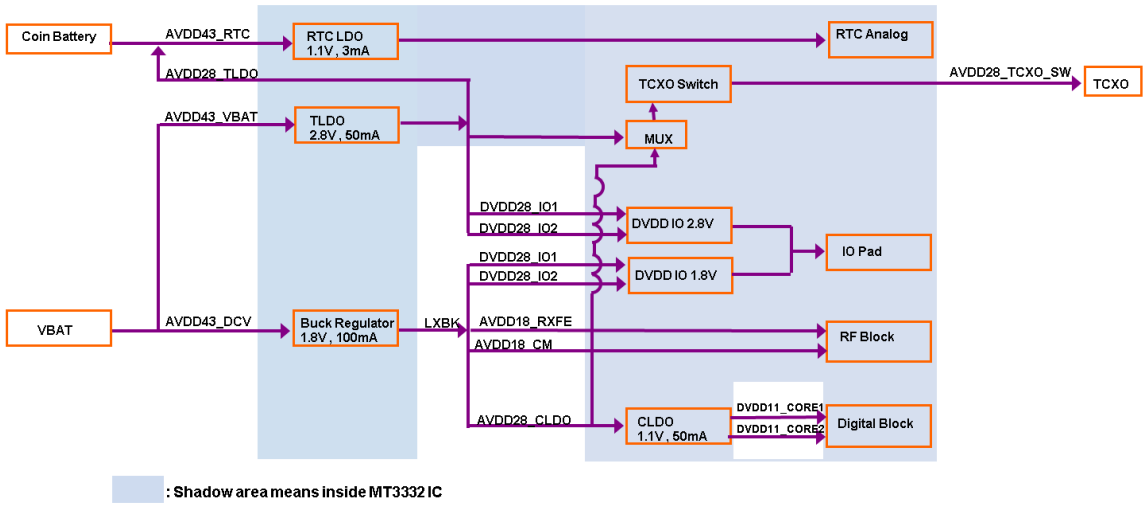


Figure 5-6: Power supply connection (low power)

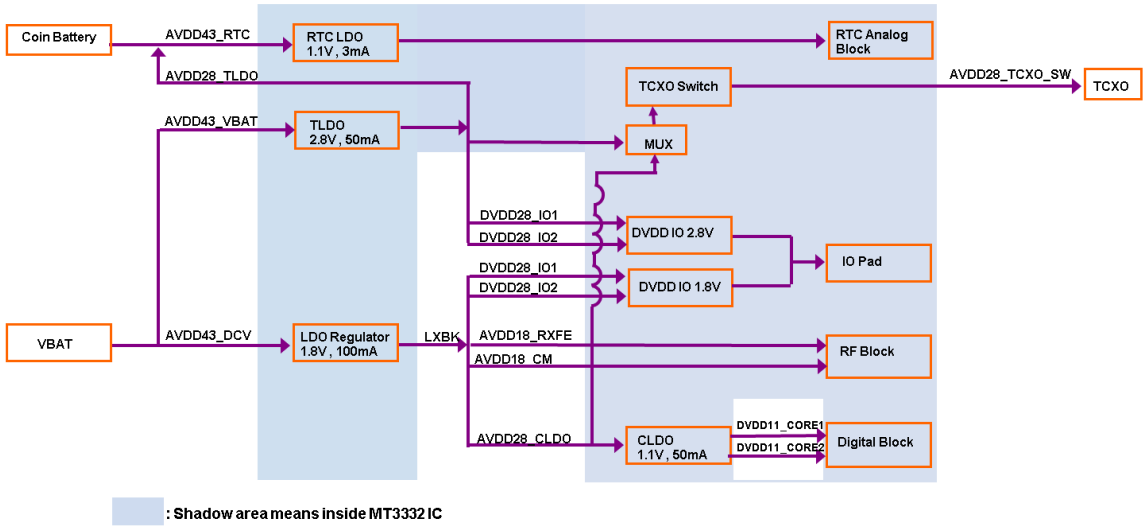


Figure 5-7: Power supply connection (low cost)

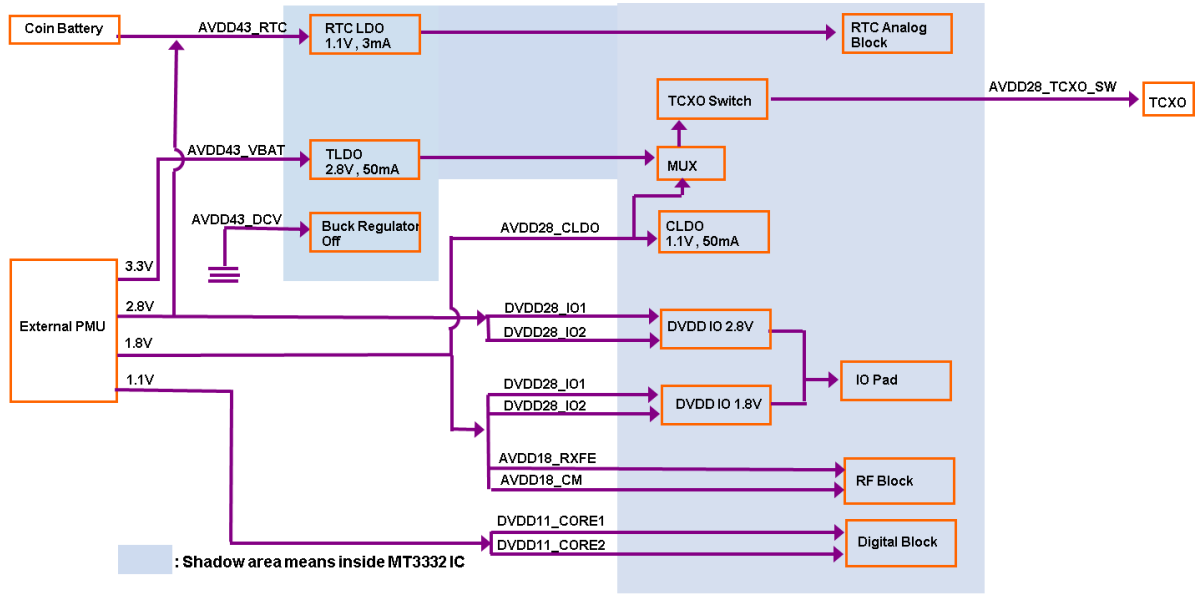


Figure 5-8: Power supply connection (external LDO)

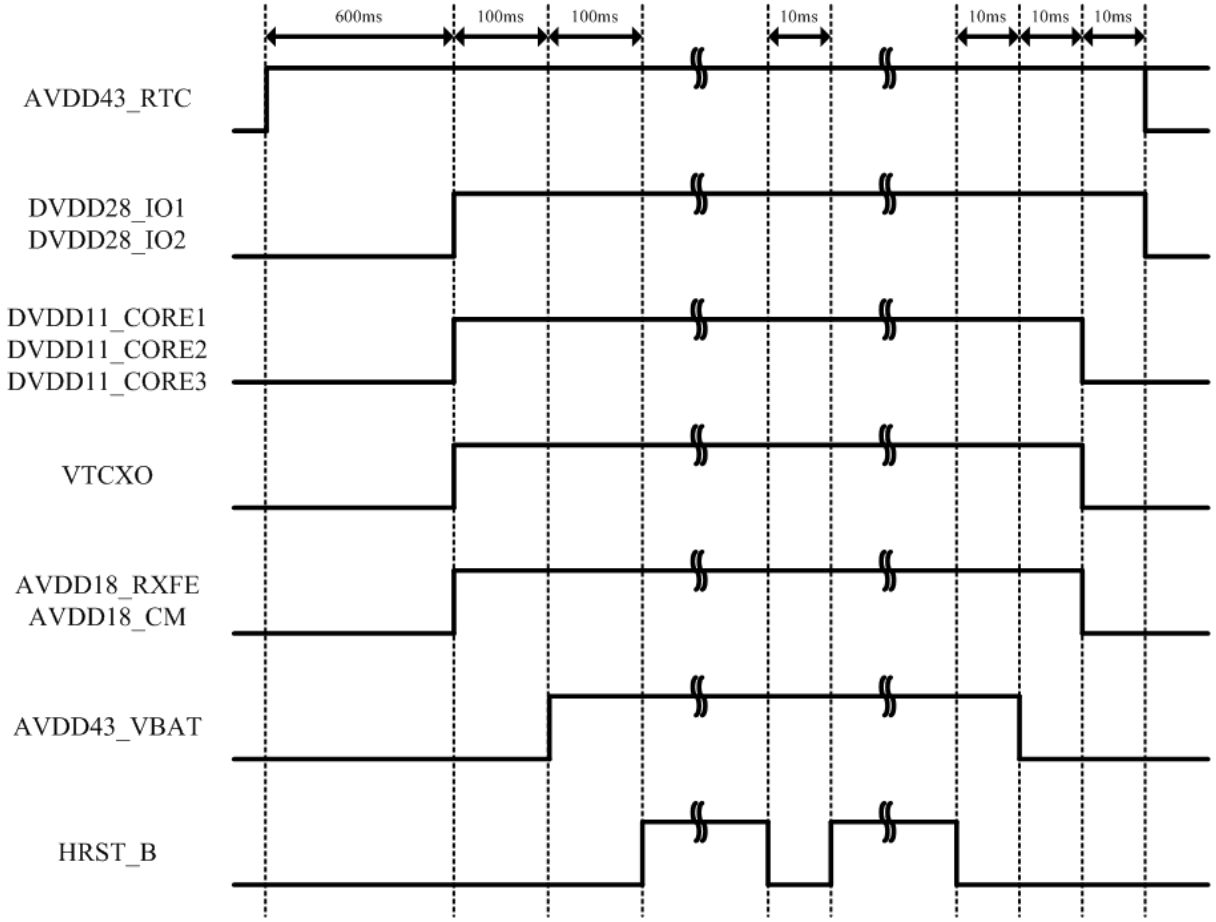


Figure 5-9: Power on/off sequence for external LDO mode

6 Electrical Characteristics

6.1 DC characteristics

6.1.1 Absolute maximum ratings

Symbol	Parameter	Rating	Unit
AVDD43_DCV	SMPS power supply	-0.3 ~ 4.3	V
AVDD43_VBAT	2.8 volts TLDO power supply	-0.3 ~ 4.3	V
AVDD28_CLDO	1.1 volts CLDO power supply	-0.3 ~ 3.6	V
DVDD28_IO1 DVDD28_IO2	IO 2.8/1.8 volts power supply	-0.3 ~ 3.6	V
DVDD11_CORE1 DVDD11_CORE2 DVDD11_CORE3	Baseband 1.1 volts power supply	-0.3 ~ 1.21	V
AVDD43_RTC	RTC 1.1 volts LDO power supply	-0.3 ~ 4.3	V
AVDD18_RXFE	1.8 volts supply for RF core circuits	-0.3 ~ 3.6	V
AVDD18_CM		-0.3 ~ 3.6	V
T_{STG}	Storage temperature	-50 ~ +125	°C
T_A	Operating temperature	-45 ~ +85	°C

6.1.2 Recommended operating conditions

Symbol	Parameter	Min.	Typ.	Max.	Unit
AVDD43_DCV	SMPS power supply	2.8	3.3	4.3	V
AVDD43_VBAT	2.8 volts TLDO power supply	2.8	3.3	4.3	V
DVDD11_CORE1 DVDD11_CORE2 DVDD11_CORE3	1.1 volts baseband core power	0.99	1.1	1.21	V
DVDD28_IO1 DVDD28_IO2	2.8 volts digital I/O power	2.52	2.8	3.08	V
	1.8 volts digital I/O power	1.62	1.8	1.98	V
AVDD18_RXFE	1.35 volts supply for RF core circuits in bypass mode	1.3	1.35	1.98	V
	1.8 volts supply for RF core circuits in LDO mode	1.62	1.8	3.08	V
AVDD18_CM	1.35 volts supply for common RF block in bypass mode	1.3	1.35	1.98	V
	1.8V volts supply for common RF block in LDO mode	1.62	1.8	3.08	V
T_A	Operating temperature	-40	25	85	˚C
T_j	Commercial junction operating temperature	0	25	115	˚C
	Industry junction operating temperature	-40	25	125	˚C

6.1.3 General DC characteristics

Symbol	Parameter	Condition	Min.	Max.	Unit
I_{IL}	Input low current	No pull-up or down	-1	1	uA
I_{IH}	Input high current	No pull-up or down	-1	1	uA
I_{OZ}	Tri-state leakage current		-10	10	uA

6.1.4 DC electrical characteristics for 2.8 volts operation

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
VDD	Supply voltage of core power		0.99	1.1	1.21	V
VDDIO	Supply voltage of IO power		2.52	2.8	3.08	V
V_{IL}	Input lower voltage	LVTTL	-0.3	-	0.25*VDDIO	V
V_{IH}	Input high voltage		0.75*VDDIO	-	VDDIO+0.3	V
V_{OL}	Output low voltage	VDDIO = min I_{OL} = -2 mA	-	-	0.15*VDDIO	V
V_{OH}	Output high voltage	VDDIO = min I_{OH} = -2 mA	0.85*VDDIO	-	-	V
R_{PU}	Input pull-up resistance	VDDIO = typ Vinput = 0 V	40	85	190	KΩ
R_{PD}	Input pull-down resistance	VDDIO = typ Vinput = 2.8 V	40	85	190	KΩ

6.1.5 DC electrical characteristics for 1.8 volts operation

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
VDD	Supply voltage of core power		0.99	1.1	1.21	V
VDDIO	Supply voltage of IO power		1.62	1.8	1.98	V
V_{IL}	Input lower voltage	LVTTL	-0.3	-	0.25*VDDIO	V
V_{IH}	Input high voltage		0.75*VDDIO	-	VDDIO+0.3	V
V_{OL}	Output low voltage	VDDIO = min I_{OL} = -2 mA	-	-	0.15*VDDIO	V
V_{OH}	Output high voltage	VDDIO = min I_{OH} = -2 mA	0.85*VDDIO	-	-	V
R_{PU}	Input pull-up resistance	VDDIO = typ Vinput = 0 V	70	150	320	KΩ
R_{PD}	Input pull-down resistance	VDDIO = typ Vinput = 1.8 V	70	150	320	KΩ

6.1.6 DC electrical characteristics for 1.1 volts operation (for FORCE_ON and 32K_OUT)

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
VDD	Supply voltage of core power		0.99	1.1	1.21	V
VDDIO	Supply voltage of IO power		0.99	1.1	1.21	V
V_{IL}	Input lower voltage	LVTTL	-0.3	-	0.25*VDDIO	V
V_{IH}	Input high voltage		0.75*VDDIO	-	VDDIO+0.3	V
V_{OL}	Output low voltage	VDDIO = min I_{OL} = -2 mA	-	-	0.15*VDDIO	V
V_{OH}	Output high voltage	VDDIO = min I_{OH} = -2 mA	0.85*VDDIO	-	-	V
R_{PU}	Input pull-up resistance	VDDIO = typ Vinput = 0 V	130		560	KΩ
R_{PD}	Input pull-down resistance	VDDIO = typ Vinput = 1.1 V	130		560	KΩ

6.2 Analog related characteristics

6.2.1 SMPS DC characteristics

Symbol	Parameter	Min.	Typ.	Max.	Unit	Note
AVDD43_DCV	SMPS input supply voltage	2.8	3.3	4.3	V	
DCV	SMPS output	1.74	1.84	1.94	V	
I_{max}	SMPS current limit	120	-	500	mA	
I_{cc}	For normal operation current	-	20	100	mA	
ΔV_PWM	Ripple of PWM mode	-	-	40	mV	With L=1uH, C=4.7uF
ΔV_PFM	Ripple of PFM mode	-	-	90	mV	With L=1uH, C=4.7uF
I_q	Quiescent current	-	50	65	uA	

6.2.2 TCXO LDO DC characteristics

Symbol	Parameter	Min.	Typ.	Max.	Unit	Note
AVDD43_VBAT	TCXO LDO input supply voltage	2.8	3.3	4.3	V	Will change to bypass mode under 3.1 volts
AVDD28_TLDO	TCXO LDO output	2.71	2.8	2.89	V	
I_{max}	TCXO LDO current limit	60	-	250	mA	
I_{cc}	For normal operation current	-	1	50	mA	Not include external devices
	PSRR-30 KHz	35	-	-	dB	Co = 1 uF, ESR = 0.05, Iload = 25 mA
	Load regulation	-84	10	84	mV	

Symbol	Parameter	Min.	Typ.	Max.	Unit	Note
I_q	Quiescent current	-	50	65	uA	

6.2.3 TCXO SWITCH DC characteristics

Symbol	Parameter	Min.	Typ.	Max.	Unit	Note
AVDD_TCXO_SW	TCXO switch output voltage @ TCXO switch input = AVDD28_TLDO	2.66	-	-	V	
AVDD_TCXO_SW	TCXO switch output voltage @ TCXO switch input = AVDD28_CLDO	1.71	-	-	V	
I_{max}	TCXO SWITCH current limit	-	-	30	mA	

6.2.4 1.1 volts core LDO DC characteristics

Symbol	Parameter	Min.	Typ.	Max.	Unit	Note
AVDD28_CLDO	1.2 volts LDO input supply voltage	1.62	1.8	3.08	V	
AVDD11_CLDO	1.1 volts LDO output	1.05	1.12	1.2	V	
I_{max}	1.1 volts LDO current limit	60	-	250	mA	
I_{cc}	For normal core operation current	-	15	50	mA	
	Load regulation	-	-	-	mV	
I_q	Quiescent current	-	10	20	uA	

6.2.5 1.1 volts RTC LDO DC characteristics

Symbol	Parameter	Min.	Typ.	Max.	Unit	Note
AVDD43_RTC	RTC LDO input supply voltage	2	4	4.3	V	
AVDD11_RTC	RTC LDO output	0.99	1.1	1.21	V	
I_{max}	RTC LDO current limit	-	-	-	mA	
I_{cc}	For normal RTC operation current	-	-	3	mA	
I_q	Quiescent current	-	-	3.5	uA	
I_{leak}	Leakage current	2.2	10	-	uA	Including LDO and RTC domain circuit

6.2.6 32 KHz crystal oscillator (XOSC32)

Symbol	Parameter	Min.	Typ.	Max.	Unit	Note
AVDD11_RTC	Analog power supply	0.99	-	1.21	V	
Dcyc	Duty cycle	-	50	-	%	

6.3 RF related characteristics

6.3.1 DC electrical characteristics for RF part

Symbol	Parameter	Min.	Typ.	Max.	Unit
I_{cc} (GPS-ONLLY)	Total supply current:	-	TBD	TBD	mA
I_{cc}(GPS+GALILEO)	Total supply current:	-	TBD	-	mA
I_{cc}(GPS+BEIDOUu)	Total supply current:	-	TBD	-	mA
I_{cc}(GPS+GLONASS)	Total supply current:	-	-	TBD	mA

6.3.2 RX chain (GPS-ONLY)

Parameter	Condition	Min.	Typ.	Max.	Unit
RF input frequency		-	1575.4	-	MHz
LO frequency	LO frequency is 4.092MHz lower than RF	-	1571.3	-	MHz
LO leakage	Measured at balun matching network input at LNA high gain	-	-70	-	dBm
Input return loss	Single-ended input and external matched to 50Ω source using balun matching network for all gain	-10	-	-	dB
Gain (Av) (integrated average over Fc+-4M)	High current mode with max PGA gain	80	78	76	dB
	Low current mode with max PGA gain	-	-	58	dB
PGA Gain range		-	24	-	dB
PGA Gain step		-	2	-	dB
Gain compression	Blocker -25dBm CW at 1710MHz, relative to uncompressed gain, max PGA gain	-	1	2	dB
NF	High current mode with max PGA gain	-	TBD	-	dB
	Low current mode with max PGA gain	-	4.8	-	dB
ΔNF at Gain=62dB	relative to NF at max Gain	-	0.5	1	dB
ΔNF at Gain=52dB	relative to NF at max Gain	-	2	3	dB
NF under compression	Blocker -25dBm CW at 1710MHz, max gain	-	7	10	dB
Input IP3, inband	max gain, 5M/10M offset@-60dBm	-35	-30	-	dBm
Input IP3, outband	max gain, ~2000M/2400M@-40dBm	-15	-10	-	dBm
Input IP2, outband	max gain, ~800M/2400M@-40dBm	+30	+35	-	dBm
Input P1 dB, inband	PGA gain=0dB, offset 500 k	-58	-55	-	
Frequency response, relative to 4.092MHz, (GPS/Galileo)	At offset +-3MHz	-	-12/-6	-	
	At offset +-10MHz	-	-40/-34	-	
	At offset +-20MHz	-	-60/-54	-	
	At offset +-100MHz	-	-100/-94	-	
Gain ripple, GPS	4.092+-1MHz	-	1.0	1.5	dB

Gain ripple, Galileo	4.092+-2MHz	-	2.0	3.0	dB
Delay ripple, GPS	4.092+-1MHz	-	60	110	ns
Delay ripple, Galileo	4.092+-2MHz	-	40	70	ns
Image rejection	All mode	-	35	-	dB
DC offset		-	±50	±100	mV
ADC clock		-	16.368	-	MHz
ADC input FS		-	1.0	-	Vppd
ADC	ENOB	7.5	8.3	-	bits
	SNR over Fclk/2	45	50	-	dB
RX Current	High current mode	-	TBD	-	mA
	Low current mode	-	TBD	-	mA

6.3.3 RX chain (GPS+BEIDOU mode)

Parameter	Condition	Min.	Typ.	Max.	Unit
RF input frequency		-	1561	-	MHz
LO frequency	LO frequency is 4.092 MHz lower than RF	-	1568.2	-	MHz
LO leakage	Measured at balun matching network input at LNA high gain	-	-70	-	dBm
Input return loss	Differential input and external matched to 50Ω source using balun matching network for all gain	-10	-	-	dB
Gain (Av) (integrated average over Fc+-4M)	High current mode with max PGA gain	80	76	70	dB
	Low current mode with max PGA gain	-	-	52	dB
PGA Gain range		-	24	-	dB
PGA Gain step		-	2	-	dB
Gain compression	Blocker -25dBm CW at 1710MHz, relative to uncompressed gain, max PGA gain	-	1	2	dB
NF (integrated average over Fc+-2M)	High current mode with max PGA gain	-	1.7	-	dB
	Low current mode with max PGA gain	-	4.8	-	dB
ΔNF at Gain=56dB	relative to NF at max Gain	-	0.5	1	dB
ΔNF at Gain=46dB	relative to NF at max Gain	-	2	3	dB
NF under compression	Blocker -25dBm CW at 1710MHz, max gain	-	7	10	dB
Input IP3, inband	max gain, +10M/+20M offset @ -70dBm	-50	-45	-	dBm
Input IP3, outband	max gain, ~2000M/2400M@ -40dBm	-15	-10	-	dBm
Input IP2, outband	max gain, ~800M/2400M @ -40dBm	+30	+35	-	dBm
Input P1 dB, inband	PGA gain=0dB, offset 500 k	-58	-55	-	dBm
Frequency response (relative to 7.16M)	At 0~5MHz	-	3	4	dB
	At 33MHz	-	-43	-40	dB
	At 53MHz	-	-60	-57	dB

	At 120MHz	-	-83	-80	dB
	At 180MHz	-	-100	-97	dB
LPF 3 dB bandwidth	(recom. 4th order Butterworth BW=9M)	-	TBD	-	MHz
Gain ripple	7.2+-1MHz	-	0.5	1.0	dB
	7.2+-2MHz	-	1.0	2.0	dB
Delay ripple	7.2+-2MHz	-	40	70	ns
Image rejection	All gain mode	-	35	-	dB
DC offset		-	±50	±100	mV
ADC clock		-	66	-	MHz
ADC input FS		-	1.0	-	Vppd
ADC	ENOB	7.5	8.3	-	
	SNR over Fclk/2	45	50	-	dB
RX Current	High current mode	-	TBD	-	mA
	Low current mode	-	TBD	-	mA

6.3.4 RX chain (GPS+GLONASS mode)

Parameter	Condition	Min.	Typ.	Max.	Unit
RF input frequency		-	1575.4	-	MHz
LO frequency		-	1588.6	--	MHz
LO leakage	Measured at balun matching network input at LNA high gain	-	-70	-	dBm
Input return loss	Differential input and external matched to 50Ω source using balun matching network for all gain	-10	-	-	dB
Gain (Av) (integrated average over Fc+-4M)	High current mode with max PGA gain	80	76	70	dB
	Low current mode with max PGA gain	-	-	52	dB
PGA Gain range		-	24	-	dB
PGA Gain step		-	2	-	dB
Gain compression	Blocker -25dBm CW at 1710MHz, relative to uncompressed gain, max PGA gain	-	1	2	dB
NF (integrated average over Fc+-4M)	High current mode with max PGA gain	-	1.7	-	dB
	Low current mode with max PGA gain	-	4.8	-	dB
ΔNF at Gain=56dB	relative to NF at max Gain	-	0.5	1	dB
ΔNF at Gain=46dB	relative to NF at max Gain	-	2	3	dB
NF under compression	Blocker -25dBm CW at 1710MHz, max gain	-	7	10	dB
Input IP3, inband	max gain, +10M/+20M offset@-70dBm	-50	-45	-	dBm
Input IP3, outband	max gain, ~2000M/2400M@-40dBm	-15	-10	-	dBm
Input IP2, outband	max gain, ~800M/2400M@-40dBm	+30	+35	-	dBm
Input P1 dB, inband	PGA gain=0dB, offset 500 k	-58	-55	-	dBm
Frequency response	At 0~23MHz	-	3	4	dB
	At 33MHz	-	-25	-22	dB

(relative to 13.14M)	At 53MHz	-	-43	-40	dB
	At 120MHz	-	-66	-63	dB
	At 180MHz	-	-85	-82	dB
LPF 3 dB bandwidth	(recom. 4th order Butterworth BW=15M)	-	TBD	-	MHz
Gain ripple	13+-1MHz	-	0.5	1.0	dB
	13+-4MHz	-	2.0	3.0	dB
Delay ripple	13+-4MHz	-	10	14	ns
Image rejection	All gain mode	-	35	-	dB
DC offset		-	±50	±100	mV
ADC clock		-	66.192	-	MHz
ADC input FS		-	1.0	-	Vppd
ADC	ENOB	7.5	8.3	-	Bits
	SNR over Fclk/2	45	50	-	dB
RX Current	High current mode	-	TBD	-	mA
	Low current mode	-	TBD	-	mA

6.3.5 Crystal oscillator (XO)

Symbol	Parameter	Min.	Typ.	Max.	Unit
F_{tcxo}	TCXO oscillation frequency	12.6	16.368	40	MHz
V_{tcxo}	TCXO output swing	0.8	1.2	-	Vpp

7 Interface Characteristics

7.1 RS-232 interface timing

Baudrate required (bps)	Programmed baudrate (bps)	Baudrate error (%)	Baudrate error (%) [3]
4,800	4,800.000	0.0000	0.002
9,600	9,600.000	0.0000	0.002
14,400	14,408.451	0.0587	0.0567
19,200	19,164.319	0.0587	0.0567
38,400	38,422.535	0.0587	0.0567
57,600	57,633.803	0.0587	0.0567
115,200	115,267.606	0.0587	0.0567
230,400	230,535.211	0.0587	0.0567
460,800	454,666.667	-1.3310	-1.3330
921,600	909,333.333	-1.3310	-1.3330

Notes:
1. UART baud-rate settings with UART_CLK frequency = 16.368 MHz (UART_CLK uses the reference clock of the system).
2. The baudrate error is optimized. Each baudrate needs to adjust counter to obtain the optimized error.
3. Suppose TCXO frequency is exactly at 16.368 MHz. If TCXO has 20 PPM, the error will raise slightly.

Figure 7-1: Timing diagram of RS-232 interface

7.2 SPI interface timing

Description	Symbol	Min.	Max.	Unit	Note
SCS# setup time	T1	0.5T	-	ns	1
SCS# hold time	T2	0.5T	-	ns	1
SO setup time	T3	0.5T – 3t	0.5T - 2t	ns	1, 2
SO hold time	T4	0.5T + 2t	0.5T + 3t	ns	1, 2
SIN setup time	T5	3t	-	ns	1, 2
SIN hold time	T6	10	-	ns	1

Notes:

1. The condition of SPI clock cycle (T) is (SPI_IPLLSPI_IPLL/12) MHz ~ (rf_clk/1,020) MHz.
2. t indicates the period of SPI controller clock, which is SPISPI_IPLL clock or rf_clk.

Figure 7-2: Timing diagram of SPI interface

7.3 I2C interface timing

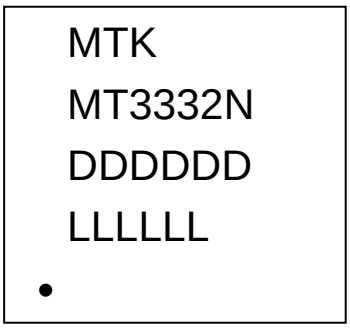
Symbol	Period
T1	(MM_CNT_PHASE_VAL0+1)/TCXO_CLK
T2	(MM_CNT_PHASE_VAL1+1)/TCXO_CLK
T3	(MM_CNT_PHASE_VAL2+1)/TCXO_CLK
T4	(MM_CNT_PHASE_VAL3+1)/TCXO_CLK

Note: The condition of I2C clock cycle (I2C_CLK) is (TCXO_CLK/4) MHz ~ (TCXO_CLK/(MM_CNT+4)) MHz. The MM_CNT is sum of MM_CNT_PHASE_VAL0, MM_CNT_PHASE_VAL1, MM_CNT_PHASE_VAL2 and MM_CNT_PHASE_VAL3 in full speed mode.

Figure 7-3: Timing diagram of HOST I2C interface

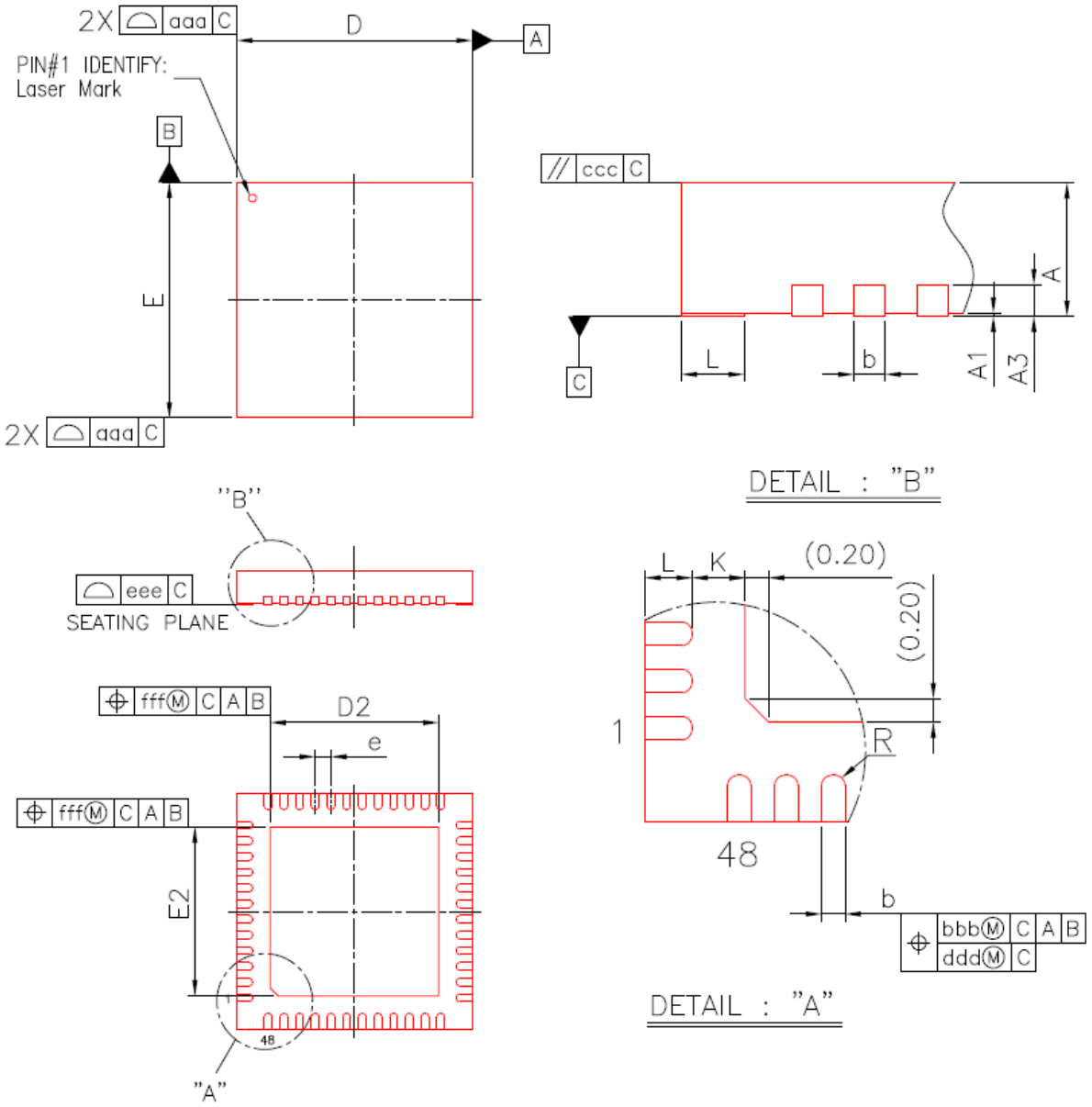
8 Package Description

8.1 Top mark



N : QFN package
DDDDDD : Date code
LLLLLL : Lot number

8.2 Package dimensions



Exposed Pad Size							Internal Pad Size					
L/F	Dimension in mm			Dimension in inch			Dimension in mm			Dimension in inch		
	MIN	NOM	MAX	MIN	NOM	MAX	MIN	NOM	MAX	MIN	NOM	MAX
D2/E2	4.15	4.30	4.45	0.163	0.169	0.175	4.45	4.60	4.75	0.175	0.181	0.187

Symbol	Dimension in mm			Dimension in inch		
	MIN	NOM	MAX	MIN	NOM	MAX
A	0.80	0.85	0.90	0.031	0.033	0.035
A1	0.00	0.02	0.05	0.000	0.001	0.002
A3		0.20 REF			0.008 REF	
b	0.15	0.20	0.25	0.006	0.008	0.010
D/E	5.90	6.00	6.10	0.232	0.236	0.240
e		0.40 BSC			0.016 BSC	
L	0.30	0.40	0.50	0.012	0.016	0.020
K	0.20	---	---	0.008	---	---
R	0.075	---	---	0.003	---	---
aaa		0.10			0.004	
bbb		0.07			0.003	
ccc		0.10			0.004	
ddd		0.05			0.002	
eee		0.08			0.003	
fff		0.10			0.004	

NOTE:

1. CONTROLLING DIMENSION : MILLIMETER
2. REFERENCE DOCUMENT: JEDEC MO-220.

ESD CAUTION

MT3332 is ESD (electrostatic discharge) sensitive device and may be damaged with ESD or spike voltage. Although MT3332 is with built-in ESD protection circuitry, please handle with care to avoid permanent malfunction or performance degradation.

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