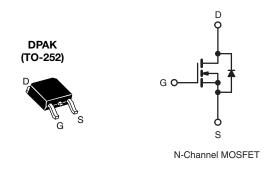
Vishay Siliconix

COMPLIANT

HALOGEN FREE

E Series Power MOSFET

PRODUCT SUMMARY					
V _{DS} (V) at T _J max.	650				
R _{DS(on)} max. at 25 °C (Ω)	V _{GS} = 10 V	0.6			
Q _g max. (nC)	40				
Q _{gs} (nC)	5				
Q _{gd} (nC)	9				
Configuration	Single				



FEATURES

- Low Figure-of-Merit (FOM) Ron x Qg
- Low Input Capacitance (Ciss)
- · Reduced Switching and Conduction Losses
- Ultra Low Gate Charge (Qa)
- Avalanche Energy Rated (UIS)
- Material categorization: For definitions of compliance please see www.vishay.com/doc?99912

APPLICATIONS

- Server and Telecom Power Supplies
- Switch Mode Power Supplies (SMPS)
- Power Factor Correction Power Supplies (PFC)
- Lighting
 - High-Intensity Discharge (HID)
 - Fluorescent Ballast Lighting
- Industrial
 - Welding
 - Induction Heating
 - Motor Drives
 - Battery Chargers
 - Renewable Energy
 - Solar (PV Inverters)

ORDERING INFORMATION				
Package	DPAK (TO-252)			
	SiHD7N60E-GE3			
Lood (Dh) free and Helegan free	SiHD7N60ET1-GE3			
Lead (Pb)-free and Halogen-free	SiHD7N60ET5-GE3			
	SiHD7N60ET4-GE3			

ABSOLUTE MAXIMUM RATINGS (T _C = 25 °C, unless otherwise noted)						
PARAMETER			SYMBOL	LIMIT	UNIT	
Drain-Source Voltage			V_{DS}	600		
Drain-Source Voltage	T _C = - 25 °	T _C = - 25 °C, I _D = 250 μA		575	J	
Gate-Source Voltage			.,	± 20	V	
Gate-Source Voltage AC (f > 1 Hz)			V_{GS}	30		
Continuous Drain Current (T _J = 150 °C)	V _{GS} at 10 V	$T_C = 25 ^{\circ}\text{C}$ $T_C = 100 ^{\circ}\text{C}$	I _D	7	А	
	V _{GS} at 10 V	T _C = 100 °C		5		
Pulsed Drain Current ^a			I _{DM}	18		
Linear Derating Factor				0.63	W/°C	
Single Pulse Avalanche Energyb			E _{AS}	43	mJ	
Maximum Power Dissipation			P_{D}	78	W	
Operating Junction and Storage Temperature Range			T _J , T _{stg}	- 55 to + 150	°C	
Drain-Source Voltage Slope	rce Voltage Slope T _J = 125 °C		dV/dt	37	V/ns	
Reverse Diode dV/dtd			uv/at	3	V/IIS	
Soldering Recommendations (Peak Temperatur	re) ^c fo	for 10 s		300	°C	

Notes

- a. Repetitive rating; pulse width limited by maximum junction temperature.
- b. $V_{DD} = 50 \text{ V}$, starting $T_J = 25 \,^{\circ}\text{C}$, $L = 13.8 \,\text{mH}$, $R_q = 25 \,\Omega$, $I_{AS} = 2.5 \,\text{A}$.
- c. 1.6 mm from case.
- d. $I_{SD} \le I_D$, $dI/dt = 100 \text{ A/}\mu\text{s}$, starting $T_J = 25 \,^{\circ}\text{C}$.



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THERMAL RESISTANCE RATINGS						
PARAMETER	SYMBOL	TYP.	MAX.	UNIT		
Maximum Junction-to-Ambient	R _{thJA}	-	62	°C/W		
Maximum Junction-to-Case (Drain)	R_{thJC}	-	1.6			

PARAMETER	SYMBOL	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
Static						•	•
Drain-Source Breakdown Voltage	V _{DS}	V _{GS} = 0 V, I _D = 250 μA		609	-	-	V
V _{DS} Temperature Coefficient	$\Delta V_{DS}/T_{J}$	Referenc	e to 25 °C, I _D = 1 mA	-	0.68	-	V/°C
Gate-Source Threshold Voltage (N)	V _{GS(th)}	V _{DS} =	V _{GS} , I _D = 250 μA	2	-	4	V
Gate-Source Leakage	I _{GSS}	,	$V_{GS} = \pm 20 \text{ V}$		-	± 100	nA
	I _{DSS}	V _{DS} =	V _{DS} = 600 V, V _{GS} = 0 V		-	1	
Zero Gate Voltage Drain Current		V _{DS} = 480 V	V _{DS} = 480 V, V _{GS} = 0 V, T _J = 125 °C		-	10	μA
Drain-Source On-State Resistance	R _{DS(on)}	V _{GS} = 10 V	I _D = 3.5 A	-	0.5	0.6	Ω
Forward Transconductance	9 _{fs}	V _{DS} =	= 50 V, I _D = 3.5 A	-	1.9	-	S
Dynamic				l.	l		
Input Capacitance	C _{iss}		V _{GS} = 0 V,	-	680	-	-
Output Capacitance	C _{oss}	┦ ,	$V_{\rm DS} = 100 \rm V,$	-	39	-	
Reverse Transfer Capacitance	C _{rss}		f = 1 MHz	-	5	-	
Effective Output Capacitance, Energy Related ^a	C _{o(er)}	V 0VV 400VV 0V		-	34	-	pF
Effective Output Capacitance, Time Related ^b	C _{o(tr)}	V _{DS} = 0 \	$V_{DS} = 0 \text{ V to } 480 \text{ V}, V_{GS} = 0 \text{ V}$		100	-	
Total Gate Charge	Qg			-	20	40	
Gate-Source Charge	Q _{gs}	V _{GS} = 10 V	$V_{GS} = 10 \text{ V}$ $I_D = 3.5 \text{ A}, V_{DS} = 480 \text{ V}$		5	-	nC
Gate-Drain Charge	Q _{gd}	1		-	9	-	
Turn-On Delay Time	t _{d(on)}		V _{DD} = 480 V, I _D = 3.5 A,		13	26	ns
Rise Time	t _r				13	26	
Turn-Off Delay Time	t _{d(off)}	$V_{GS} = 10 \text{ V}, R_g = 9.1 \Omega$			24	48	
Fall Time	t _f				14	28	
Gate Input Resistance	R_g	f = 1 MHz, open drain		-	1.1	-	Ω
Drain-Source Body Diode Characteristics							
Continuous Source-Drain Diode Current	I _S	MOSFET symbol showing the integral reverse p - n junction diode		-	-	7	١.
Pulsed Diode Forward Current	I _{SM}			-	-	18	A
Diode Forward Voltage	V _{SD}	T _J = 25 °C, I _S = 3.5 A, V _{GS} = 0 V		-	-	1.2	V
Reverse Recovery Time	t _{rr}	T _J = 25 °C, I _F = I _{S = 3.5} A, dI/dt = 100 A/ μ s. V_R = 20 V		-	230	-	ns
Reverse Recovery Charge	Q _{rr}			-	1.9	-	μC
Reverse Recovery Current	I _{RRM}			_	14	_	A

Notes

- a. $C_{oss(er)}$ is a fixed capacitance that gives the same energy as C_{oss} while V_{DS} is rising from 0 % to 80 % V_{DSS} .
- b. $C_{oss(tr)}$ is a fixed capacitance that gives the same charging time as C_{oss} while V_{DS} is rising from 0 % to 80 % V_{DSS} .



TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

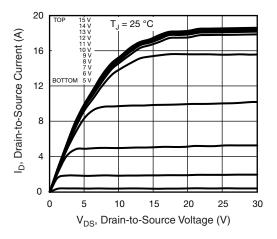


Fig. 1 - Typical Output Characteristics

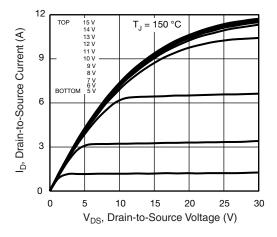


Fig. 2 - Typical Output Characteristics

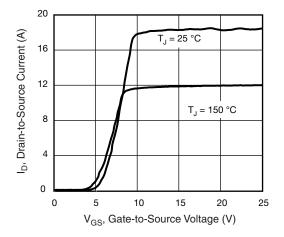


Fig. 3 - Typical Transfer Characteristics

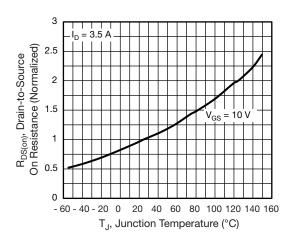


Fig. 4 - Normalized On-Resistance vs. Temperature

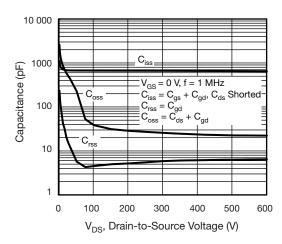


Fig. 5 - Typical Capacitance vs. Drain-to-Source Voltage

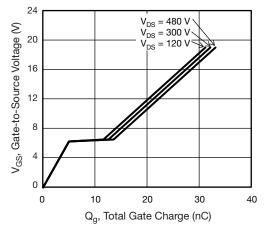


Fig. 6 - Typical Gate Charge vs. Gate-to-Source Voltage



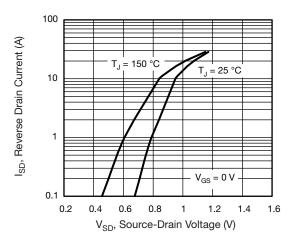


Fig. 7 - Typical Source-Drain Diode Forward Voltage

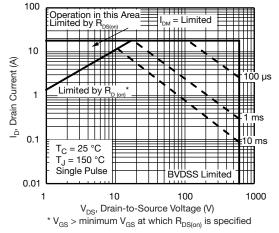


Fig. 8 - Maximum Safe Operating Area

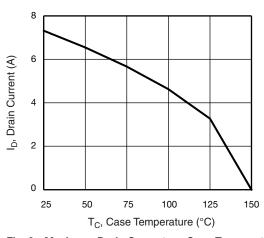


Fig. 9 - Maximum Drain Current vs. Case Temperature

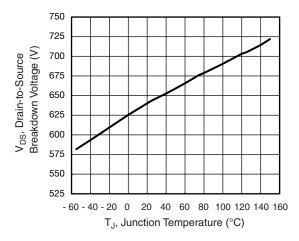


Fig. 10 - Temperature vs. Drain-to-Source Voltage

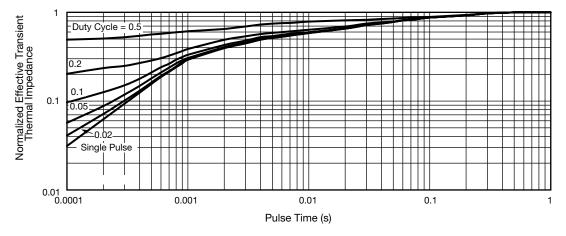


Fig. 11 - Normalized Thermal Transient Impedance, Junction-to-Case

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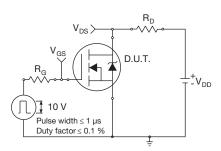


Fig. 12 - Switching Time Test Circuit

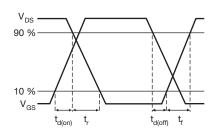


Fig. 13 - Switching Time Waveforms

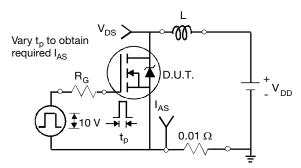


Fig. 14 - Unclamped Inductive Test Circuit

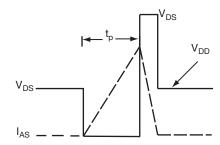


Fig. 15 - Unclamped Inductive Waveforms

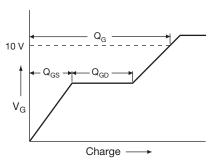


Fig. 16 - Basic Gate Charge Waveform

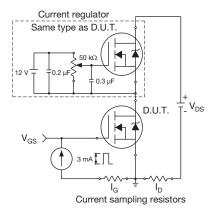
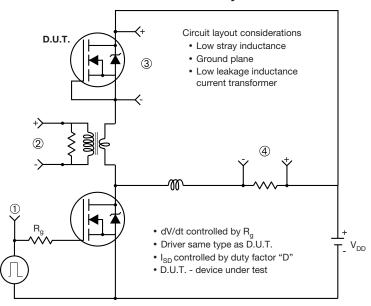


Fig. 17 - Gate Charge Test Circuit



Peak Diode Recovery dV/dt Test Circuit



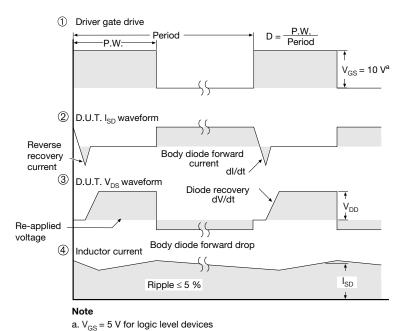
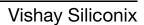


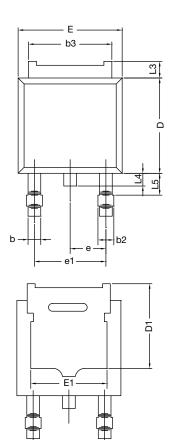
Fig. 18 - For N-Channel

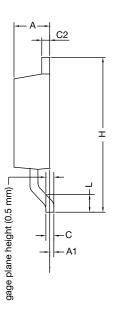
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TO-252AA Case Outline



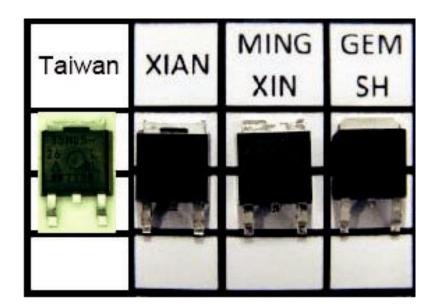


	MILLIN	METERS	INC	HES		
DIM.	MIN.	MAX.	MIN.	MAX.		
Α	2.18	2.38	0.086	0.094		
A1	-	0.127	-	0.005		
b	0.64	0.88	0.025	0.035		
b2	0.76	1.14	0.030	0.045		
b3	4.95	5.46	0.195	0.215		
С	0.46	0.61	0.018	0.024		
C2	0.46	0.89	0.018	0.035		
D	5.97	6.22	0.235	0.245		
D1	4.10	-	0.161	-		
Е	6.35	6.73	0.250	0.265		
E1	4.32	-	0.170	-		
Н	9.40	10.41	0.370	0.410		
е	2.28	BSC	0.090 BSC			
e1	4.56	BSC	0.180 BSC			
L	1.40	1.78	0.055	0.070		
L3	0.89	1.27	0.035	0.050		
L4	=	1.02	-	0.040		
L5	1.01	1.52	0.040	0.060		
ECN: T13-0359-Rev. O, 03-Jun-13						

DWG: 5347

Notes

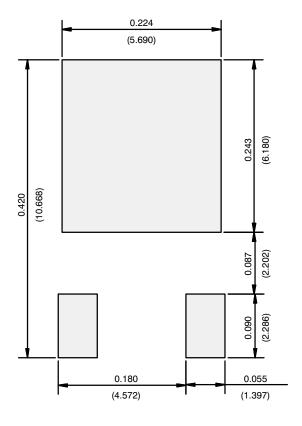
- Dimension L3 is for reference only.
- Xi'an, Mingxin, and GEM SH actual photo.



Revision: 03-Jun-13 Document Number: 71197



RECOMMENDED MINIMUM PADS FOR DPAK (TO-252)



Recommended Minimum Pads Dimensions in Inches/(mm)

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APPLICATION NOTE



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Revision: 02-Oct-12 Document Number: 91000