

Dual P-Channel Logical Level MOSFET

These miniature surface mount MOSFETs utilize a high cell density trench process to provide low  $r_{DS(on)}$  and to ensure minimal power loss and heat dissipation. Typical applications are DC-DC converters and power management in portable and battery-powered products such as computers, printers, PCMCIA cards, cellular and cordless telephones.

PRODUCT SUMMARY		
$V_{DS}$ (V)	$r_{DS(on)}$ (OHM)	$I_D$ (A)
-20	0.028 @ $V_{GS} = -4.5V$	6
	0.045 @ $V_{GS} = -2.5V$	4.8
	0.078 @ $V_{GS} = -1.8V$	3.6

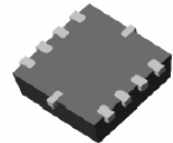
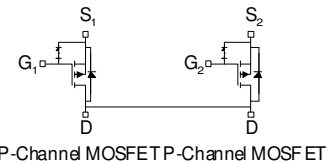
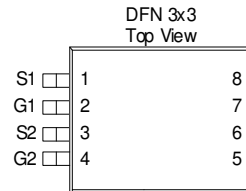
- Low  $r_{DS(on)}$  provides higher efficiency and extends battery life
- Low thermal impedance copper leadframe DFN 3x3 saves board space
- Fast switching speed
- High performance trench technology



RoHS COMPLIANT HALOGEN FREE



ESD Protected  
2000V



ABSOLUTE MAXIMUM RATINGS ( $T_A = 25^\circ C$ UNLESS OTHERWISE NOTED)			
Parameter	Symbol	Maximum	Units
Drain-Source Voltage	$V_{DS}$	-20	V
Gate-Source Voltage	$V_{GS}$	$\pm 8$	
Continuous Drain Current <sup>a</sup>	$I_D$	$T_A=25^\circ C$	6
		$T_A=70^\circ C$	4.9
Pulsed Drain Current <sup>b</sup>	$I_{DM}$	$\pm 40$	A
Continuous Source Current (Diode Conduction) <sup>a</sup>	$I_S$	1.5	A
Power Dissipation <sup>a</sup>	$P_D$	$T_A=25^\circ C$	1.5
		$T_A=70^\circ C$	1.0
Operating Junction and Storage Temperature Range	$T_J, T_{stg}$	-55 to 150	$^\circ C$

THERMAL RESISTANCE RATINGS				
Parameter	Symbol	Typ	Max	
Maximum Junction-to-Ambient <sup>a</sup>	$R_{thJA}$	$t \leq 10$ sec	72	83
		Steady State	100	120
				$^\circ C/W$

Notes

- a. Surface Mounted on 1" x 1" FR4 Board.
- b. Pulse width limited by maximum junction temperature

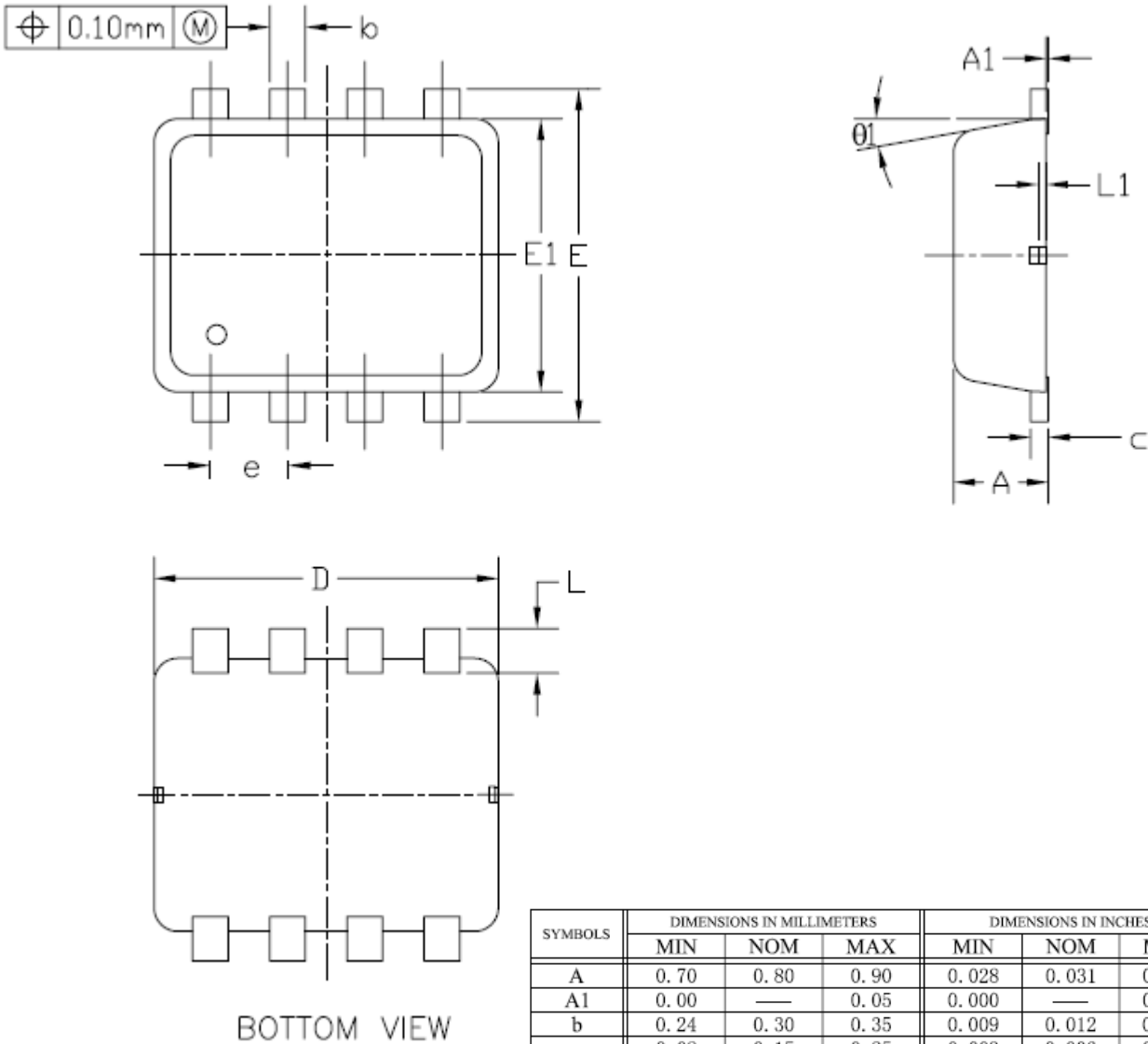
SPECIFICATIONS (T <sub>A</sub> = 25°C UNLESS OTHERWISE NOTED)						
Parameter	Symbol	Test Conditions				Unit
			Min	Typ	Max	
<b>Static</b>						
Gate-Threshold Voltage	V <sub>GS(th)</sub>	V <sub>GS</sub> = V <sub>DS</sub> , I <sub>D</sub> = 250 uA	-0.3			V
Gate-Body Leakage	I <sub>GSS</sub>	V <sub>DS</sub> = 0 V, V <sub>GS</sub> = ± 8 V			±10	μA
Zero Gate Voltage Drain Current	I <sub>DSS</sub>	V <sub>DS</sub> = 16 V, V <sub>GS</sub> = 0 V			-1	μA
		V <sub>DS</sub> = 16 V, V <sub>GS</sub> = 0 V, T <sub>J</sub> = 55°C			-10	μA
On-State Drain Current <sup>A</sup>	I <sub>D(on)</sub>	V <sub>DS</sub> = 5 V, V <sub>GS</sub> = 4.5 V	5			A
Drain-Source On-Resistance <sup>A</sup>	r <sub>DS(on)</sub>	V <sub>GS</sub> = 4.5 V, I <sub>D</sub> = 1 A			0.028	Ω
		V <sub>GS</sub> = 2.5 V, I <sub>D</sub> = 1 A			0.045	
		V <sub>GS</sub> = 1.8 V, I <sub>D</sub> = 1 A			0.078	
Forward Transconductance <sup>A</sup>	g <sub>fs</sub>	V <sub>DS</sub> = 10 V, I <sub>D</sub> = 1 A		25		S
Diode Forward Voltage <sup>A</sup>	V <sub>SD</sub>	I <sub>S</sub> = 1 A, V <sub>GS</sub> = 0 V		0.8		V
<b>Dynamic<sup>b</sup></b>						
Total Gate Charge	Q <sub>g</sub>	V <sub>DS</sub> =10V, V <sub>GS</sub> =4.5V, I <sub>D</sub> =1A		11		nC
Gate-Source Charge	Q <sub>gs</sub>			1.5		
Gate-Drain Charge	Q <sub>gd</sub>			2.9		
Turn-On Delay Time	t <sub>d(on)</sub>	V <sub>DD</sub> =10V, V <sub>GS</sub> =4.5V, I <sub>D</sub> =1A , R <sub>GEN</sub> =10Ω		10		nS
Rise Time	t <sub>r</sub>			70		
Turn-Off Delay Time	t <sub>d(off)</sub>			100		
Fall-Time	t <sub>f</sub>			80		

Notes

- a. Pulse test: PW ≤ 300us duty cycle ≤ 2%.
- b. Guaranteed by design, not subject to production testing.

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# Package Information



SYMBOLS	DIMENSIONS IN MILLIMETERS			DIMENSIONS IN INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A	0.70	0.80	0.90	0.028	0.031	0.035
A1	0.00	—	0.05	0.000	—	0.002
b	0.24	0.30	0.35	0.009	0.012	0.014
c	0.08	0.15	0.25	0.003	0.006	0.010
D	2.90 BSC			0.114 BSC		
E	2.80 BSC			0.110 BSC		
E1	2.30 BSC			0.091 BSC		
e	0.65 BSC			0.026 BSC		
L	0.20	0.38	0.45	0.008	0.015	0.018
L1	0.05	—	—	0.002	—	—
$\theta 1$	0°	10°	12°	0°	10°	12°