F10179 • F10579

CARRY LOOKAHEAD GENERATOR

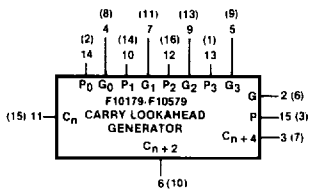
F10K VOLTAGE COMPENSATED ECL

DESCRIPTION — The F10179 and F10579 are high-speed carry generators intended for use with the F10181 4-bit ALU. Typical addition times for two 32-bit words is 30 ns when using F10181 in the ripple carry mode. When the F10179 carry lookahead generator is used, the typical add time drops to 18 ns.

PIN NAMES

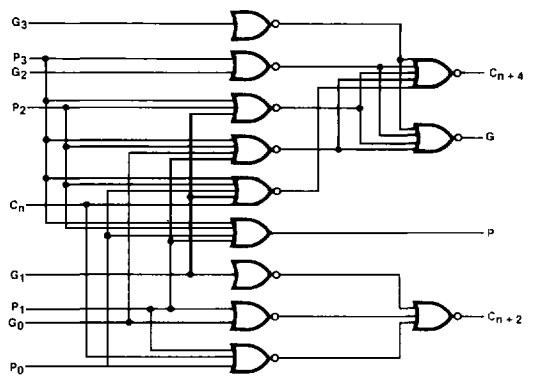
C_n	Carry In
C_{n+2}, $+4$	Carry Out
P	Propagate
G	Generate

LOGIC SYMBOL



V_{CC1} = 1(5)
V_{CC2} = 16 (4)
V_{EE} = 8 (12)
( ) Flatpak

LOGIC DIAGRAM



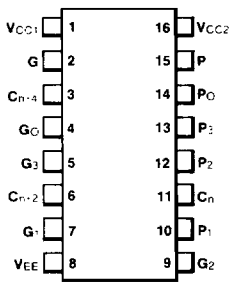
$P = P_0 + P_1 + P_2 + P_3$

$G = (G_0 + P_1 + P_2 + P_3)(G_1 + P_2 + P_3)(G_2 + P_3)G_3$

$C_{n+2} = (C_n + P_0 + P_1)(G_0 + P_1)G_1$

$C_{n+4} = (C_n + P_0 + P_1 + P_2 + P_3)(G_0 + P_1 + P_2 + P_3)(G_1 + P_2 + P_3)(G_2 + P_3)G_3$

CONNECTION DIAGRAM
DIP (TOP VIEW)
PACKAGE OUTLINE 6B



$C_{n+2} = G_1(G_0 + P_1)C_n + P_1 + P_0)$ (Product of Max terms)
or
$\overline{C}_{n+2} = \overline{G}_1 + \overline{G}_0\overline{P}_1 + \overline{C}_n\overline{P}_1\overline{P}_0$ (Complement of the sum of Min terms)

$C_{n+4} = G_3(G_2 + P_3)(G_1 + P_2 + P_3)(G_0 + P_1 + P_2 + P_3)(C_n + P_0 + P_1 + P_2 + P_3$
or
$\overline{C}_{n+4} = \overline{G}_3 + \overline{G}_2\overline{P}_3 + \overline{G}_1\overline{P}_2\overline{P}_3 + \overline{G}_0\overline{P}_1\overline{P}_2\overline{P}_3 + \overline{C}_n\overline{P}_0\overline{P}_1\overline{P}_2\overline{P}_3$

$G_G = G_3(G_2 + P_3)(G_1 + P_2 + P_3)(G_0 + P_1 + P_2 + P_3)$
or
$\overline{G}_G = \overline{G}_3 + \overline{G}_2\overline{P}_3 + \overline{G}_1\overline{P}_2\overline{P}_3 + \overline{G}_0\overline{P}_1\overline{P}_2\overline{P}_3$

$P_G = \overline{P}_0 + \overline{P}_1 + \overline{P}_2 + \overline{P}_3$
or
$\overline{P}_G = \overline{P}_0\overline{P}_1\overline{P}_2\overline{P}_3$

TRUTH TABLE

INPUTS										OUTPUTS		
C_n	G_0	P_0	G_1	P_1	G_2	P_2	G_3	P_3	C_{n+2}	C_{n+4}	G_G	P_G
X	X	X	H	H					H			
H	H	X	H	X					H			
X	H	H	H	X					H			
X	X	X	L	X					L			
X	L	X	X	L					L			
L	X	L	X	L					L			
X	X	X	X	X	X	X	H	H		H		
X	X	X	X	X	H	H	H	X		H		
X	X	X	H	H	H	X	H	X		H		
X	H	H	H	X	H	X	H	X		H		
H	H	X	H	X	H	X	H	X		H		
X	X	X	X	X	X	X	L	X		L		
X	X	X	X	X	L	X	X	L		L		
X	X	X	L	X	X	L	X	L		L		
X	L	X	X	L	X	L	X	L		L		
L	X	L	X	L	X	L	X	L		L		
	X		X	X	X	X	H	H			H	
	X		X	X	H	H	H	X			H	
	X		H	H	H	X	H	X			H	
	H		H	X	H	X	H	X			H	
	X		X	X	X	X	L				L	
	X		X	X	L	X	X	L			L	
	X		L	X	X	L	X	L			L	
	L		X	L	X	L	X	L			L	
		H		X		X		X				H
		X		H		X		X				H
		X		X		H		X				H
		X		X		X		H				H
		L		L		L		L		•		L

L = LOW Voltage Level H = HIGH Voltage Level X = Don't Care

DC CHARACTERISTICS: $V_{EE} = -5.2$ V, $V_{CC} = GND$

SYMBOL	CHARACTERISTIC	LIMITS B	LIMITS TYP	LIMITS A	UNITS	T_A	CONDITIONS
I_{IH}	Input Current HIGH						
	G_0, G_1, C_n			270	μA	25 °C	$V_{IN} = V_{IHA}$
	G_2, G_3			225			
	P_0			355			
	P_1, P_3			440			
	P_2			395			
I_{EE}	Power Supply Current	−72	−59		mA	25 °C	Inputs and Outputs Open

SWITCHING CHARACTERISTICS: $V_{EE} = -5.2$ V, $T_A = 25$ °C

SYMBOL	CHARACTERISTIC	LIMITS B	LIMITS TYP	LIMITS A	UNITS	CONDITIONS
t_{PLH}, t_{PHL}	Propagation Delay LOW to HIGH, HIGH to LOW C_n to C_{n+2}	1.0	3.0	4.5	ns	See Figure 1, 3
t_{PLH}, t_{PHL}	Propagation Delay LOW to HIGH, HIGH to LOW G_3 to G	1.0	4.0	5.5	ns	See Figure 2, 3
t_{TLH}, t_{THL}	Output Transition Time LOW to HIGH, HIGH to LOW (20% to 80%) (80% to 20%)	0.8	3.5	5.5	ns	See Figure 1, 3

SWITCHING CIRCUIT AND WAVEFORMS

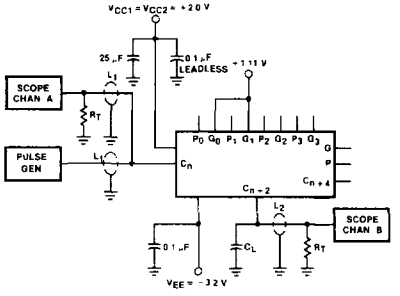


Fig. 1 For Output C_{n+2}

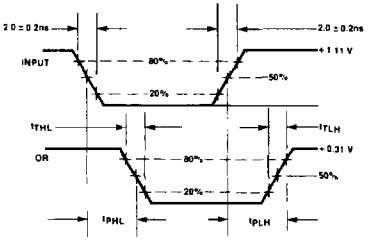


Fig. 3 For Both Outputs

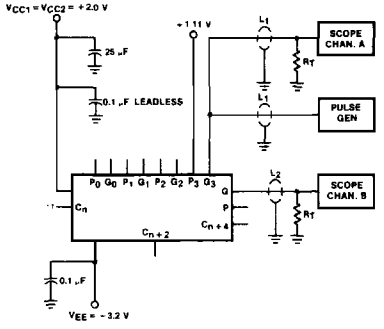


Fig. 2 For Output G

L_1 and L_2 = equal length 50 Ω impedance lines
$R_T = 50$ Ω termination of scope
C_L = Jig and stray capacitance < 5.0 pF
Decoupling 0.1 μF from gnd to V_{EE} and V_{CC}
$V_{CC1} = V_{CC2} = 2.0$ V
$V_{EE} = -3.2$ V