

# SANYO Semiconductors DATA SHEET

An ON Semiconductor Company



Bi-CMOS LSI For Home Stereo Systems FM/AM Tuner IC

### Overview

The LV23411V is single chip tuner IC, and FM/AM radio is able to be realized with few external parts.

### Functions

- FM tuner
- AM tuner
- MPX Stereo Decoder
- Tuning system

### Features

- No alignments necessary
- Reduction of external component counts
- Large audio output signal is available for home stereo systems
- Worldwide FM band support (64 to 108MHz)
- Worldwide AM band support (520 to 1710kHz)
- Soft-mute, Stereo-blend function
- LV23411 corresponds to Europe Immunity standard (EN55020-S1)
- I<sup>2</sup>C control interface

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## **Specifications**

#### Absolute Maximum Ratings at Ta = 25°C, GND1 = GND2 = GND3 = GND4 = GND5 = 0V

Parameter	Symbol	Conditions	Ratings	Unit
Maximum supply voltage	V <sub>CC</sub> max		10.0	V
Digital output voltage	V <sub>O</sub> max	SDA	3.6	V
Digital input voltage	V <sub>IN</sub> 1 max	SDA, SCL	3.6	V
	V <sub>IN</sub> 2 max	CLK IN	3.6	V
Allowable power dissipation	Pd max	Ta ≤ 70°C *1	450	mW
Operating temperature	Topr		-20 to +70	°C
Storage temperature	Tstg		-40 to +125	°C

\*1 : Mounted on a specified board. Board size is 114.3mm  $\times$  76.1mm  $\times$  1.6mm, glass epoxy.

#### **Operating Conditions** at $Ta = 25^{\circ}C$ , GND1 = GND2 = GND3 = GND4 = GND5 = 0V

Parameter	Symbol	Conditions Ratings		Unit
Recommended supply voltage	V <sub>CC</sub>		9.0	V
Operating supply voltage Range	V <sub>CC</sub> op	Register 1Eh bit 1 (LEVSHIF) = 0	4.5 to 6.5	V
* Note		Register 1Eh bit 1 (LEVSHIF) = 1	8.5 to 9.5	V

\* Note : supply the stabilized voltage.

#### Interface Conditions at Ta = -20 to $+70^{\circ}$ C, GND1 = GND2 = GND3 = GND4 = GND5 = 0V

Decemeter	Symbol			Linit		
Parameter	Symbol	Conditions	min	typ	max	Unit
High level input voltage	V <sub>IH</sub> 1	SDA, SCL	2.3		3.5	V
	V <sub>IH</sub> 2	CLK IN	2.3		3.5	V
Low level input voltage	V <sub>IL</sub> 1	SDA, SCL	0		0.5	V
	V <sub>IL</sub> 2	CLK IN	0		0.3	V
Output voltage	VO	SDA	0		3.5	V
Crystal frequency	fin	CLK IN		32.768		kHz
Crystal frequency accuracy	faccuracy		-100		+100	ppm

#### **Operating Characteristics** at $Ta = 25^{\circ}C$ , $V_{CC} = 9.0V$ , with the designated circuit.

Parameter	Symbol	Conditions		Unit						
i arameter	Gymbol			typ	max	0				
[FM characteristics ; MONO] : fc = 98	3MHz, V <sub>IN</sub> = 600	$IB\mu V$ , fm = 1kHz, De-emphasis = 50 $\mu$ s, IF = 225KHz,	BW = 45%							
MONO : 75kHz dev										
STEREO : L+R = 67.5kHz dev, Pilot = 7.5kHz dev										
Volume level = 3, Register 1Eh bit 1 (LEVSHIF) = 1, Pin 9 output, Audio filter = IHF-BP F, Soft mute = off ,Soft stereo = off										
Current drain	ICC FM	No input	35	40	45	mA				
30dB S/N sensitivity	SN30	S/N = 30dB input level		10	15	dBμV				
Signal-to-noise ratio	SNR	MONO	62	70		dB				
Total harmonic distortion	THD	MONO		0.5	1.5	%				
	THD-ST	STEREO		0.5	2.5	%				
Demodulation output	V <sub>O</sub> 3	MONO	518	775	1160	mVrms				
SD operation level	SD	FS = 4	17	25	33	dBμV				
Mute attenuation	Mute	MONO	60	75		dB				
Stereo separation	Sep	Pin 10 output/Pin 9 output	20	35		dB				
Carrier leak	CL	STEREO SNR, Audio filter = OFF	30	40		dB				
Stereo on level	ST-ON	L+R = 67.5kHz dev, Pilot level		3.0	6.5	%				
[AM characteristics] : $fc = 1MHz$ , $V_{IN}$	= 94dBµV, fm =	400Hz, mod = 30% IF = 53KHz, BW = 50%								
Volume level = 2, Register 1Eh bit 1	(LEVSHIF) = 1,	Pin 9 output, Audio filter = 15kHz LPF OFF	1							
Current drain	ICC AM	No input	30	35	40	mA				
20dB S/N sensitivity	SN20	S/N = 20dB input level		48	65	dBμV				
Signal-to-noise ratio	SNR		42	50		dB				
Total harmonic distortion	THD			0.8	2.8	%				
Demodulation output	V <sub>O</sub> 2		122	173	245	mVrms				
SD operation level	SD	FS = 4	46	54	64	dBµV				
Mute attenuation	Mute	15kHz LPF ON	50	65		dB				

## Package Dimensions

unit : mm (typ) 3259



## **Block Diagram**



Pin	descriptio	ons			
Pin	Pin name	I/O	Descriptions	Remarks	DC voltage
1	AM-ANT	I	AM antenna input	Connect to pin2 through Matching coil or Ferrite antenna.	-
2	AM-REF	0	Reference voltage for AM part	Connect to pin1 through Matching coil or Ferrite antenna.	2.2V
3	AM-CAP	I	AM capacitor bank	Exteranal inductor (recommendation value) is connected between this pin and GND.	-
4	GND1	-	AM antenna GND	Connected to GND	0V
5	VREF1	0	Reference voltage for analog	Capacitor of 1µF is connected between this pin and GND.	4.3V
6	MPX IN_OUT	0	Demodulato output	When RDS used, LC72725 is applicable	2.5V
7	AM RF-AGC	0	AM RF AGC output	Capacitor of 1µF is connected between this pin and GND.	-
8	GND2	-	Analog GND	Connected to GND	0V
9	L-OUT	0	Audio Lch output	According to the V <sub>CC</sub> _application, Reference Output_level setting is cangeable by Register Bit.	2.6V (3.7V)
10	R-OUT	0	Audio Rch output	Register 1Eh bit 1 (LEVSHIF) =1: Register 1Eh bit 1 (LEVSHIF) =0:	
11	V <sub>CC</sub> -Low	-	Voltage supply pin at low voltage operation mode	When using V <sub>CC</sub> < 6V, Connect to Pin15 directly	-
12	AM LCF	0	AM low_cut filter	Capacitor of 0.047uF is connected between this pin and GND.	2.2V
13	SD-OUT	0	SD indicator output	Active low output	3.0V (0.1V)
14	ST-OUT	0	ST indicator output	Active low output	3.0V (0.1V)
15	VCC	-	Voltage supply pin		-
16	CLK_IN	I	Reference clock input	32.768kHz crystal connected to GND. It is Also applicable to input directly clock signals ( square wave GND reference)	-
17	IF AGC CAP	-	IF-AGC monitor point (test)	Open	-
18	SD-ADJ	-	Adjustment for SD on level	Incase of changing SD on level, put Resistor between this pin and GND.	-
19	NC	I			-
20	SCL	I	I <sup>2</sup> C interface CLK input		-
21	SDA	I/O	I <sup>2</sup> C interface Data input/output		-
22	VREF2	0	Output voltage pin for V <sub>DD</sub>	V <sub>DD</sub> output_pin of 3.0V. This pin is applicable to supply the current other IC up to 10mA.	3.0V
23	GND3	-	Digital GND for control part		0V
24	L1	-	Local oscillator	39nH connected to pin 25	-
25	VREF3	0	Reference voltage for local OSC part		5.0V
26	L2	-	Local oscillator	39nH connected to pin 25	-
27	GND4	-	Analog GND for OSC part	Connected to GND	0V
28	FLL-CAP	-	Oscillator tuning voltage output	Capacitor of $0.1\mu F$ is connected between this pin and GND.	-
29	GND5	-	Analog GND for FMRF part	Connected to GND	0V
30	FM-ANT	I	FM antenna input 1	Input impedance is $75\Omega$	0.8V

Pin i	Pin internal circuit description							
Pin No.	Pin name	Pin voltage (V)	Description	Internal equivalent circuit				
1	AM-ANT	2.2	AM antenna input pin. The AM antenna coil is connected between pins 40 and this pin. R = $100\Omega$					
2	AM-REF	2.2	Reference voltage pin for AM. VAM-REF = 2.2V	(15) 2.2V Regulator 2)				
3	AM-CAP	-	Tuning pinl for AM. (AM Capacitor Bank)	CAP-BANK				
4	GND1	0	GND pin for Analogue AM_FE part.					
5	VREF1	4.3	Analogue part (tuner) reference bias terminal. VREF1 = 4.3V	(15) 4.3V Regulator 5				
6	MPX IN_OUT	2.5	FM demodulation output /input for MPX. R = 100Ω					
7	AM RF-AGC	-	Pin for AM_RF AGC. R1 = $2M\Omega$ R2 = $5k\Omega$ R3 = $250\Omega$ R4 = $1k\Omega$	$\begin{array}{c} \\ R2 \\ R2 \\ R4 \\ R4 \\ R4 \\ R4 \\ R4 \\ R4$				
8	GND2	0	GND pin for Analogue tuner part.					
9 10	L-OUT R-OUT	2.6 (3.7V when LEVSHIF = 1)	L-ch (R-ch) output pin. R = 100Ω R <sub>OUT</sub> = 150Ω					

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PIN NO.	Pin name	Pin voltage (V)	Description	Internal equivalent circuit
11	V <sub>CC</sub> -Low	-	when using with V <sub>CC</sub> < 6.0V, 11Pin-15 Pin is shorted.	15 5V Regulator (1) 4.3V Regulator
12	AM LCF	2.2	Terminal for AM Low-cut Filter. R1 = $250\Omega$ R2 = $100k\Omega$ R3 = $100k\Omega$ R4 = $50k\Omega$ R5 = $50k\Omega$	$12 \xrightarrow{R1}_{R2} \xrightarrow{R3}_{R5} \otimes \\ \otimes $
13	SD-OUT	3.0 (less than 0.1)	SD indicator output pin. Active Low output. R = 100kΩ	22 R≩ 13 SW ₩ ₩
14	ST-OUT	3.0 (less than 0.1)	FM stereo indicator output pin Active Low output R = 100kΩ	R ST SW T T
15	V <sub>CC</sub>	Vcc	Analogue part power supply pin. When using 8.5 to 9.5V, set to Register 1Eh Bit 1 (LEVSHIF) = 1 When using with $V_{CC} < 6.5V$ , set to Register 1Eh Bit 1 (LEVSHIF) = 0 And 11Pin-15Pin must be shorted "	
16	CLK_IN	2.1 (OSC mode)	For internal reference clock. 32.768kHz crystal connected to GND. It is Also applicable to input directly clock signals ( square wave GND_reference) $R = 100\Omega$	(16) R Crystal oscillator
17	IF AGC CAP	-	This pin is for test. Open R1 = 1.5kΩ, R2 = 1kΩ, R3 = 500Ω	
18	SD-ADJ	-	Open normally. Adjust pin for SD sensitivity with to kΩ resistor connected to GND	

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Pin No.	Pin name	Pin voltage (V)	Description	Internal equivalent circuit
19	NC	-		
20	SCL	-	Digital interface CLK line. R = 1kΩ	
21	SDA		Digital interface DATA line. (Interactive data communication line.) Require pull_up resistor 3.3k to 10k between this pin and Vref2 (V <sub>DD</sub> ). R = $250\Omega$	(21) R data
22	VREF2	3	Reference voltage output pin for Logic part. Vref2 = 3V	(15) Regulator (22)
23	GND3	0	GND pin for digital part (Control part).	
24 26	L1 L2	5	OSC coil of 39nH to be connected between this pin and pin 25.	24 CAP BANK BANK BANK
25	VREF3	5	Reference voltage pin for local oscillation circuit.	(15) 5V Regulator (25)
27	GND4	0	GND pin for local oscillation circuit.	
28	FLL-CAP	-	LPF pi n for controlled FLL internally. R = 80kΩ	
29	GND5	0	GND pin for local oscillation circuit.	

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Pin No.	Pin name	Pin voltage (V)	Description	Internal equivalent circuit
30	FM-ANT	0.8	FM antenna input pin FM. R = 1.5kΩ Rin = 75Ω	

### Used parts

Component	Parameter	Value	Tolerance	Туре	Supplier
L1	Local Osc Coil	39nH	5%	LL2012-FHL39NJ	ТОКО
L2	Local Osc Coil	39nH	5%	LL2012-FHL39NJ	ТОКО
L3	AM Loop antenna	18.1µH	5%	4910-CSL18R1JN1	SAGAMI
T1	AM RF matching	250µH	-	A90326057	COILS
				#7003RNS-A1109YZS	ТОКО
C1	Ripple Filter	1μF			
C2	AM RF AGC Capacitor	1μF			
C3	Coupling Capacitor	1μF			
C4	Coupling Capacitor	1μF			
C5	Supply Bypass Capacitor	0.1µF			
C6	Supply Bypass Capacitor	22µF			
C7	AM Low-cut Filter	0.1µF			
C8	Supply Bypass Capacitor	22µF			
C9	Osc Filter	0.1µF			
C10	Ripple Filter	0.1µF			
R1	Pulled-up Resistor	4.7kΩ			
R2	Pulled-up Resistor	4.7kΩ			
R3	SD Adjust Resistor	to kΩ			
BPF	FM ANT BPF	-	-	GFMB7	SOSHIN
X1	Crystal	32.768kHz	100ppm	DT-26	KDS
LO1	AM Ferrite antenna	260µH	TBD	-	-

### Format of Bus Transfers

Bus transfers are primarily based on the I<sup>2</sup>C primitives

- Start condition
- Repeated start condition
- Stop condition
- Byte write
- Byte read

Start, restart, and stop conditions are specified as shown in Table 1 below.



Fig. 1 the I<sup>2</sup>C start, repeated start and stop conditions.

For details, like timing, etc., refer to specifications of  $I^2C$ .

8-bit write

8-bit data is sent from the master microcomputer to LV23411.

Data bit consists of MSB first and LSB last.

Data transmission is latched at the rising edge of SCL in synchronization with the SCL clock generated at the master IC. Do not change data while SCL remains HIGH.

LV23411 outputs the ACK bit between eighth and ninth falling edges of SCL



Fig. 2 Signal pattern of the I<sup>2</sup>C byte write

Read is of the same form as write, only except that the data direction is opposite. Eight data bits are sent from LV23411 to the master while Ack is sent from the master to LV23411.



Fig. 3 Signal pattern of the I<sup>2</sup>C byte read

The serial clock SCL is supplied from the master side. It is essential that data bit is output from LV23411 in synchronization with the falling edge while the master side performs latching at the rising edge.

LV23411 latches ACK at the rising edge.

The sequence to write data D into the register A of LV23411 is shown below.

- Start condition
- write the device address (C0h)
- write the register address, A
- write the target data, D
- stop condition



Fig. 4 Register write through  $l^2C$ 

When one or more data has been provided for writing, only the first data is allowed to be written.

Read sequence

- start condition
- write the device address (C0h)
- write the register address, A
- repeated start condition (or stop + start in a single master network)
- write the device address + 1 (C1h)
- read the register contents D, transmit NACK (no more data to be read)
- stop condition



Fig. 5 Register read through  $I^2C$ 

#### Interrupt Pin INT

LV23411 has the dedicated interrupt output pin. For the active level to the host, either LOW or HIGH can be selected. The INT output pin is kept floating while the PWRAD bit is cleared during initialization.

Therefore, to avoid influence on the CPU side during initialization, it is recommended to secure the non-active state by means of the pull-up or pull-down resistor.

This enables direct INT output connection to non-masking interruption of the host CPU.

### Digital interface specification (interface specification : reference)

(1). Characteristics of SDA and SCL bus line relative to the  $I^2C$  bus interface



Deservation	Querra ha a l	Standar	d-mode	High_Spe	unit	
Parameter	Symbol	min	max	min	max	unit
SCL clock frequency	FSCL	0	100	0	400	kHz
Fall time of both SDA and SCL	Tf		300	20+0.1Cb	300	ns
Rise time of both SDA and SCL	Tr		1000	20+0.1Cb	300	ns
High time of SCL	T <sub>HIGH</sub>	4.0		0.6		μs
Low time of SCL	TLOW	4.7		1.3		μs
Hold time of STAT condition	<sup>T</sup> HD ; STA	4.0		0.6		μs
Hold time of Data	T <sub>HD</sub> ; DAT	0	3.45	0	0.9	μs
Set-up time of STAT condition	<sup>T</sup> SU ; STA	4.7		0.6		μs
Set-up time of STOP condition	T <sub>SU</sub> ; STO	4.0		0.6		μs
Set-up time of Data	T <sub>SU</sub> ; DAT	250		100		ns
Bus free time between a STOP and START condition	TBUF	4.7		1.3		μs
Capacitivie load for each bus line	Cb		400		400	pF

\*Cb = Total capacitance of one bus line

#### Description of the Register of LV23411V

### Register 00h - CHIP\_ID - Chip identify register (Read-Only)

7	6	5	4	3	2	1	0			
ID[7:0]										
Bit 7-0 :	ID[7:0] : 8-bit Chip ID									
	LV243411 : 1Bh									
Note : To abor	t the command, w	vrite any value in	this register.							

### Register 01h - CHIP\_REV - Chip Revision identify register (Read-Only)

0	—	•	, 0	•	• /			
7	6	5	4	3	2	1	0	
Revision[7:0]								
Bit 7-0 :	ID[7:0] : 8-bit Chip Revision							
	ES1:00h							
Note : To abort the command, write any value in this register.								

### Register 02h - RADIO\_STAT - Radio station status (Read-Only)

7	6	5	4	3	2	1	0				
IM_STAT	IM_FS[1:0]		MO_ST	FS[2:0]		•	TUNED				
Bit 7 :	<ul> <li>IM_STAT: State of Image-station avoidance</li> <li>0 = Normal (Possible to write)</li> <li>1 = The Image-station avoidance is being processed (Impossible to write)</li> <li>Note:</li> <li>This bit works only at Register14h_bit7 (IM_EVAS) is set to "1".</li> <li>The writing processing to LV23411 is prohibited when this bit is "1".</li> </ul>										
Bit 6-5 :	<ul> <li>IM_FS : Image-signal Fieldstrength</li> <li>0 : No image-signal</li> <li>1 : There are weak Image-signal that level is less -10dB or more weaker than desire's</li> <li>2 : The level of the image –signal is around 0 - 10dB compared with desire's</li> <li>3 : The level of the image-signal is +10dB or more stronger than that of desire's</li> </ul>										
Bit 4 :	MO_ST : Mono/Stereo indicator 0 = Forced monaural 1 = Normal (Receiving in stereo mode)										
Bit 3-1 :	$\begin{split} FS[2:0] &: Fieldstrength \\ 0 &: FS < 10 \ dB\mu V \\ 1 &: FS = 10 - 20 \ dB\mu V \\ 2 &: FS = 20 - 30 \ dB\mu V \\ & \\ 7 &: FS > 70 \ dB\mu V \end{split}$										
Bit 0 :	<ul> <li>TUNED : Radio tuning flag.</li> <li>0 = No tuned</li> <li>1 = Tuned</li> <li>Note : When the tuning command succeeds, this bit is set.</li> <li>This bit is cleared under 3 conditions as below.</li> <li>1. PW_RAD = 0</li> <li>2. Tuning Frequency</li> <li>3. When FLL becomes outside the correction range</li> </ul>										

Register 04h - TNPL - Tune position low (Read-Only)										
7 6 5 4 3 2 1 0										
TUNEPOS[7:0]										
Bit 7-0 : TUNEPOS[7:0] : Current RF Frequency (Low 8 bit)										

#### Register 05h - TNPH\_STAT - Tune position high/status (Read-Only)

-		-	-				
7	6	5	4	3	2	1	0
ERROR[1:0]		TUNEPOS[12	:8]				
Bit 7-6 :	ERROR[1:0] : E	Error code					
	ERROR[1:0]	]	Remark				
	0	(	OK, Command er	nd (No Error)			
	1	]	DAC Limit Error				
	2	(	Command forced End				
	3	(	Command busy				
Bit 5:0 :	TUNEPOS[13:8	] : Current RF Fr					

#### Register 06h - COUNT\_L - Counter low (Read-Only)

7	6	5	4	3	2	1	0
COUNT[7:0]							
Bit 7-0 :	COUNT[7:0] : C	Counter value (Lo	ow 8 bit)				

#### Register 07h - COUNT\_H - Counter High (Read-Only)

7	6	5	4	3	2	1	0			
COUNT[15:8]										
Bit 7-0: COUNT[15:8] : Counter value (High 8 bit)										

#### Register 08h - IF\_OSC - DAC for IF OSC (Read/Write)

7	6	5	4	3	2	1	0
IFOSC[7:0]							
Bit 7-0 :	IFOSC[7:0] : IF	Oscillator DAC					

#### Register 09h - IFBW-DAC for IF - Filter Band width (Read/Write)

7	6	5	4	3	2	1	0	
IFBW[7:0]								
Bit 7-0 :	IFBW[7:0] : IF-Filter Band width DAC							

#### Register 0Bh - STEREO\_OSC - DAC for Stereo Decoder OSC (Read/Write)

7	6	5	4	3	2	1	0
SDOSC[7:0]							
Bit 7-0 :	: SDOSC[7:0] : Stereo Decoder Oscillator DAC						

#### Register 0Ch - RF\_OSC - DAC for RF OSC (Read/Write)

			•	,			
7	6	5	4	3	2	1	0
RFCAP[7:0]							
Bit 7-0 :	RFOSC[7:0] : R	F Oscillator DAC					

#### Register 0Dh - RFCAP - RF Cap bank (Read/Write)

7	6	5	4	3	2	1	0
RFCAP[7:0]							
Bit 7-0 :	RFCAP[7:0] : R	F Oscillator Cap	acitor-Bank				

Register 0Eh - AMCAP1 - AM - ANT Cap bank1 (Read/Write)												
7	6	6         5         4         3         2         1         0										
AMCAP[7:0]												
Bit 7-0 : AMCAP[7:0] : AM Antenna Capacitor-Bank												
Note :												
The AM antenna capacitor bank is composed of 12 bits.												
High 4 bit is arranged at "AMCTRL" register.												

#### Register 0Fh - AMCTRL - AM Station Control (Read/Write)

7	1	~	4	2	2	1	0			
/	6	5	4	3	2	1	0			
AMDIV[2:0]			AM_CAL	ACAP11	ACAP10	ACAP9	ACAP8			
Bit 7-5 :	AMDIV[2:0] : A	M Clock Divide	r							
Bit 7 :	$AM\_CD2:AM$	Clock Divider bi	t 2.							
Bit 6 :	$AM\_CD1: AM$	Clock Divider bi	t 1.							
Bit 5 :	$AM\_CD0: AM$	Clock Divider bi	t 0.							
Note : The Plea	e AM_CD[2:0] is ase set AM_CD to	used to decrease o "0" at FM mode	frequency from e.	FM - band to AM	A - band.					
	AM CD	0[2:0] Div	vide-Rate	AM-RF frea	uency (In kHz)					
	0.1 Divider OFF 0 (FM mode)									
	2		224	338	- 483					
	3		160	474	- 676					
	4		112	676	- 966					
	5		80	947	- 1353					
	6		64	1183	- 1692					
	7		48	1578	- 2256					
Bit 4 :	NA (Fixed to "0	")								
Bit 3-0 :	AMCAP[11:8] : AM Antenna Capacitor-Bank									
Bit 3 :	AMCAP_bit 11									
Bit 2 :	AMCAP_bit 10									
Bit 1 :	AMCAP_bit 9									
Bit 0 :	AMCAP_bit 8									

Register 10h - DO\_REF\_CLK\_CNF - DO output mode and reference clock configuration (Read/Write)

7	6	5	4	3	2	1	0					
IPOL	DO_SEL[1:0]		EXT_CLK_CF	G[1:0]	FS_S[2:0]							
Bit 7-5 :	NA (Fixed to "0	")										
Bit 4-3 :	3 : EXT_CLK_CFG[1:0] : External Clock Setting											
	EXT_CLK_CFG[1:0] Reference clock											
	00	(	Off									
	01	(	Oscillator clock s	ource (External	Clock source)							
	10	3	32768Hz crystal	oscillator								
	11 No use											
Bit 2-0 :	FS_S[2:0] : SD (	Station Detector	) operation level	setting								

$\begin{array}{c c c c c c c c c c c c c c c c c c c $	Register 11h - IF_SEL - IF frequency selection (Read/Write)																			
$ \begin{array}{c c c c c c c c c c c c c c c c c c c $	7	(	5	5			4			3			2			1			0	
Bit 7 : FLL_MOD: FLL operation mode 0 : Smoothing Filter = OFF 1 : Smoothing Filter = ON          Bit 6-4 : AMIF[2:0] : IF frequency setting at AM mode $MIIF[2:0] : IF frequency setting at AM mode         MIIF[2:0] : IF frequency setting at AM mode         0 1 2 3 4 5 6 7         0 1 2 3 4 5 6 7 0 1 2 3 4 5 6 7 0 1 2 3 4 5 6 7 0 1 2 3 4 5 6 7 0 1 2 3 4 5 6 7 0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 15 15 15 15 15 15 15 15 15 15 15 15 15 10 $	FLL_N	AOD .	AMIF[2:0]							FN	AIF[3	:0]								
$\begin{array}{rrrrrrrrrrrrrrrrrrrrrrrrrrrrrrrrrrrr$	Bit 7 :	F	LL_MOD: F	FLL op	peratio	on mo	de													
I : Smoothing Filter = ON         Bit 6-4 : AMIF[2:0] : IF frequency setting at AM mode $AMIF[2:0]$ 0       1       2       3       4       5       6       7         0       1       2       3       4       5       6       7         20kHz       31kHz       42kHz       53kHz       64kHz       75kHz       86kHz       97kHz         Bit 3-0 : FMIF[3:0] : IF frequency setting at FM mode (kHz)         SE_AM       RF_SEL $\overline{0$ $\overline{1}$ $\overline{2}$ $\overline{3}$ $\overline{4}$ $\overline{5}$ $\overline{6}$ $\overline{7}$ Bit 3-0 : FMIF[3:0] : IF frequency setting at FM mode (kHz) $\overline{5}$ $\overline{6}$ $\overline{7}$ $\overline{9}$ $\overline{10}$ $\overline{11}$ $\overline{12}$ $\overline{3}$ $\overline{4}$ $\overline{5}$ $\overline{6}$ $\overline{7}$ $\overline{1}$ $\overline{1}$ $\overline{2}$ $\overline{3}$ $\overline{4}$ $\overline{5}$ $\overline{6}$ $\overline{7}$ <			0: Smoot	thing	Filter	= OF	F													
Bit 6-4 : AMIF[2:0] : IF frequency setting at AM mode         AMIF[2:0]         0       1       2       3       4       5       6       7         0       1       2       3       4       5       6       7         20kHz       31kHz       42kHz       53kHz       64kHz       75kHz       86kHz       97kHz         Bit 3-0 : FMIF[3:0] : IF frequency setting at FM mode (kHz)         SE_AM RF_SEL       FMIF[3:0] $\frac{10}{0}$ $\frac{1}{12.5}$ $\frac{1}{27.5}$ $\frac{1}{32.5}$ $\frac{1}{27.5}$ $\frac{1}{27.5}$ $\frac{1}{12.5}$ $\frac{1}{27.5}$ $\frac{1}{27.5}$ $\frac{1}{12.5}$ $\frac{1}{27.5}$ <th c<="" td=""><td colspan="11">1 : Smoothing Filter = ON</td><td></td></th>	<td colspan="11">1 : Smoothing Filter = ON</td> <td></td>	1 : Smoothing Filter = ON																		
$\begin{tabular}{ c c c c c c c c c c c c c c c c c c c$	Bit 6-4 : AMIF[2:0] : IF frequency setting at AM mode																			
$ \begin{array}{ c c c c c c c c c c c c c c c c c c c$	AMIF[2:0]																			
20kHz       31kHz       42kHz       53kHz       64kHz       75kHz       86kHz       97kHz         Bit 3-0 :       FMIF[3:0] : IF frequency setting at FM mode (kHz)         SE_AM       RF_SEL       FMIF[3:0]       FMIF[3:0]         0       0       1       2       3       4       5       6       7       8       9       10       11       12       13       14       15         0       0       112.5       137.5       150       162.5       175       187.5       212.5       225       237.5       250       262.5       275       287.5       312.5       325         0       1       112.5       127.5       142.5       157.5       172.5       187.5       202.5       217.5       262.5       277.5       292.5       307.5       322.5		0	1			2		3			4		5			6		7		
Bit 3-0 : FMIF[3:0] : IF frequency setting at FM mode (kHz) SE_AM       RF_SEL       FMIF[3:0]         0       0       1       2       3       4       5       6       7       8       9       10       11       12       13       14       15         0       0       112.5       125       137.5       150       162.5       175       187.5       212.5       225       237.5       250       262.5       275       287.5       312.5       325         0       1       112.5       127.5       142.5       157.5       175.5       187.5       202.5       217.5       262.5       277.5       292.5       307.5       322.5		20kHz	31kH	Z	42	kHz		53kH	Z	64	kHz		75kH	Z	86	kHz		97kH	z	
SE_AM         RF_SEL         FMIF[3:0]           0         1         2         3         4         5         6         7         8         9         10         11         12         13         14         15           0         0         112.5         125         137.5         150         162.5         175         187.5         212.5         225         237.5         250         262.5         275         287.5         312.5         325           0         1         112.5         127.5         142.5         157.5         175.5         187.5         202.5         217.5         262.5         277.5         292.5         307.5         322.5	Bit 3-0 : FMIF[3:0] : IF frequency setting at FM mode (kHz)																			
0         1         2         3         4         5         6         7         8         9         10         11         12         13         14         15           0         0         112.5         125         137.5         150         162.5         175         187.5         212.5         225         237.5         250         262.5         275         287.5         312.5         325           0         1         112.5         127.5         142.5         157.5         175.5         187.5         202.5         217.5         262.5         277.5         292.5         307.5         322.5		SE_AM	RF_SEL								FMIF	F[3:0]								
0         0         112.5         125         137.5         150         162.5         175         187.5         212.5         225         237.5         250         262.5         275         287.5         312.5         325           0         1         112.5         127.5         142.5         157.5         175.5         187.5         202.5         217.5         262.5         277.5         287.5         312.5         325	0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15																			
0 1 112.5 127.5 142.5 157.5 157.5 172.5 187.5 202.5 217.5 232.5 247.5 262.5 277.5 292.5 307.5 322.5		0	0	112.5	125	137.5	150	162.5	175	187.5	212.5	225	237.5	250	262.5	275	287.5	312.5	325	
		0	1	112.5	127.5	142.5	157.5	157.5	172.5	187.5	202.5	217.5	232.5	247.5	262.5	277.5	292.5	307.5	322.5	

## Register 12h - REF\_CLK\_MOD - Slope correction (Read/Write)

7	6	5	4	3	2	1	0			
REFMOD[7:0]										
Bit 7-0: REFMOD[7:0] : Reference clock collection										

7	egister 13h - SM_CTRL - Statemachine control (Read/Write)												
/	6	5	4	3	2	1	0						
FLL_ON	CLKS_SE[2:0]			nSD_PM	nIF_PM	CM_SE[1:0]							
Bit 7 : F	FLL_ON : FLL c	control											
C	= FLL OFF												
1	= FLL ON												
Bit 6-4 : 0	CLKS_SE : Cloc	k source selecti	on										
C	= No select												
	= Stereo Decod	ler Oscillator is	selected										
2	L = IF Oscillator	is selected	1 / 1										
5	= AM Antenna	Uscillator is selected	lected										
4	$= \Gamma M RF Oscil$	lator is selected	1										
J F	5 = AW KF Osci.	fiator is selected	1										
	r = roscient												
Note : Bit[6	5-4] set oscillator	r source.											
Selec	t arbitrary clock	oscillator at tur	ning or calibration	ons or measure.									
Bit 3 : r	nSD_PM : Stereo Decoder PLL mute												
C	= SD PLL Off	(Calibration)											
1	= SD PLL On (	(Normal operati	on)										
Bit 2 · r	IE PM · IE PI I	mute											
	- IF PLI Off (	Calibration)											
1	- IF PLL On (	Normal operatio	n)										
1		tornia operatio											
Bit 1-0 : 0	CM_SE : Comm	and mode select	tion										
0	= No command	1											
1	= Measure mod	le											
2	R = Calibration m	node											
3	= Radio tuning	(RF frequency	tuning) mode										
Nata - Thia	1		1.										
Note : This	t the orbitrory of	ct command mod	ue.										
The	command is ever	puted by setting	TARGET VAI	I/H									
	ommand is exec	cuted by setting	TAROLI_VAI	2_L/11.									
Command e	execution time :												
5	D calibration =	540ms											
I	F calibration $= 1$	34ms											
F	RF(FM) tuning = 105ms												
F	RF (AM) tuning	= 158ms											
	_												
l _	Note:												
F	lease wait the ti	me provided for	r the above-men	tioned before all	processing inclu	uding reading the r	egister after						
h	aving executed	the command.											

Register 14h - REF_CLK_PRS - Reference clock pre-scaler (Read/Write)												
7	6	5	4	3	2	1	0					
IM_EVAS	Reserved	WAIT_SEL	AM_FINE	REFPRE	E[3:0]							
Bit 7 :	IM_EVAS : Ima 0 = OFF 1 = ON (Recom	ge signal avoida mend)	ace function ON	/OFF								
Bit 6 :	Reserved : Fixed	Reserved : Fixed to "0"										
Bit 5 :	WAIT_SEL : Selection mute release standby time after tuning 0 = 8ms wait 1 = 4ms wait											
Bit 4 :	$AM_FINE : Sele 0 = No wait whe 1 = 2ms wait wh$	ection AM_ANT on DAC value is d en DAC value is	adjustment stan changed changed	dby time								
Bit 3-0 :	REFPRE[3:0] : Reference Clock pre- scaler 0 = 1 : 1 1 = 1 : 2 2 = 1 : 4  15 = 1 : 32768											

#### Register 15h - REF\_CLK\_DIV - Reference clock divider (Read/Write)

7	6	5	4	3	2	1	0			
REFDIV[7:0]										
Bit 7-0 :	REFDIV[7:0] : F 0 : Divide rate = 1 : Divide rate =  255 : Divide rate	Reference Clock 1 2 e = 256	Divider							

### Register 16h - TARGET VAL L - Target Value Low Register (Read/Write)

7         6         5         4         3         2         1         0											
TARGET[7:0]											
Bit 7-0: TARGET[7:0] : Target frequency low 8 bit :											
Tuning frequency or Calibration frequency : low byte											

#### Register 17h - TARGET\_VAL\_H - Target Value High Register (Read/Write)

7	6	5	4	3	2	1	0				
TARGET[15:8]											
Bit 7-0 : TARGET[15:8] : Target frequency high 8 bit : Tuning frequency or Calibration frequency : high byte											
With radio power ON, lower eight bits of the target frequency are set. Then, set higher eight bits of the target frequency to this register. The command is executed.											
TUNEPOS and TARGET :											

- AM mode : 1kHz span

- FM mode : 10kHz span

Register 18	8h - RADIO_CT	RL1 - Radi	o control 1 (	Read/Write)								
7	6	5	4	3	2	1	0					
IQC_CTR	IFPOL	OSC_LEV	[1:0]	DEEM	VOL[1:0	]	EN_AMHC					
Bit 7 :	IQC_CTR : I/Q	phase change	•		•		·					
	0 = Normal mo	de (Upper het	erodyne)									
	1 = I/Q phase cl	hange : for im	age signal avo	idance (Lower heter	odyne)							
Note : U	Jsually, no-need to	change										
Ditc	IE nole abanga	by State Meel										
BILO:	0 - The IF frequencies	by State Maci	line I to local frequ	ency (Normal)								
	1 = The IF freq	uency is subtr	acted from loc:	al frequency								
Note : U	Jsually, no-need to	change		ai nequency								
Bit 5-4 :	OSC_LEV[1:0] : RF-OSC oscillation level setting											
	0 = minimum le	evel										
	$3 = \max \lim l$	evel										
	Note : 3dB step	s, Level $= 2$ is	recommended	1								
Bit 3 ·		nhasis sotting										
DIUS.	$0 = 50 \text{ us} \cdot \text{Kore}$	a China Euro	ne Ianan									
	$1 = 75 \mu s : USA$		pe, sapan									
		-										
Bit 2-1 :	VOL[1:0] : Vol	ume setting										
	$0 = \min($	VOL0)										
	$3 = \max($	VOL3)										
Dit 0 .	EN AMUCAA	M Uigh out E	Silter ON/OFE									
BILU.	O = AM HCE O	IVI HIgh-cut F										
	1 = AM HCF O	)N										
I = AM HCF ON												

### Register 19h - RADIO\_CTRL2 - Radio control 2 (Read/Write)

		1	r							
6	5	4	3	2	1	0				
Reserved	EN_AMM	Reserved	IF_AGC_LEV	RF_AGC_LEV	/[1:0]	EN_RFAGC				
Reserved : Fixed	to "0"									
Reserved : Fixed to "1"										
EN AMM : AM Mute ON/OFF										
0 = AM mute OFF										
1 = AM mute ON										
Reserved : Fixed to "0"										
IE ACC LEV.	IF AGC Level (	ontrol								
$\Pi = AGC \text{ slow m}$	n-AUC Level C	onuoi								
1 = AGC first me	ode									
RF_AGC_LEV[	1:0] : RF-AGC L	evel Control								
0 = AGC  slow m	ode									
1 = AGC normal mode										
3 = AGC first mode										
EN REAGC · R	F-AGC ON/OFF									
0 = AGC OFF										
1 = AGC ON (Normal)										
	6         Reserved         Reserved : Fixed         EN_AMM : AM         0 = AM mute OF         1 = AM mute OF         1 = AM mute OF         Reserved : Fixed         IF_AGC_LEV :         0 = AGC slow m         1 = AGC first med         RF_AGC_LEV[         0 = AGC slow m         1 = AGC normal         3 = AGC first med         EN_RFAGC : R         0 = AGC OFF         1 = AGC ON (N	6       5         Reserved       EN_AMM         Reserved : Fixed to "0"         Reserved : Fixed to "1"         EN_AMM : AM Mute ON/OFF         0 = AM mute OFF         1 = AM mute OFF         1 = AM mute ON         Reserved : Fixed to "0"         IF_AGC_LEV : IF-AGC Level C         0 = AGC slow mode         1 = AGC first mode         RF_AGC_LEV[1:0] : RF-AGC L         0 = AGC slow mode         1 = AGC normal mode         3 = AGC first mode         EN_RFAGC : RF-AGC ON/OFF         0 = AGC OFF         1 = AGC ON (Normal)	6       5       4         Reserved       EN_AMM       Reserved         Reserved : Fixed to "0"       Reserved : Fixed to "1"         EN_AMM : AM Mute ON/OFF       0 = AM mute OFF         0 = AM mute OFF       1 = AM mute ON         Reserved : Fixed to "0"       IF_AGC_LEV : IF-AGC Level Control         0 = AGC slow mode       1 = AGC first mode         RF_AGC_LEV[1:0] : RF-AGC Level Control       0 = AGC slow mode         1 = AGC normal mode       3 = AGC first mode         EN_RFAGC : RF-AGC ON/OFF       0 = AGC OFF         1 = AGC ON (Normal)       1 = AGC ON (Normal)	6       5       4       3         Reserved       EN_AMM       Reserved       IF_AGC_LEV         Reserved : Fixed to "0"       Reserved : Fixed to "1"       EN_AMM : AM Mute ON/OFF         0 = AM mute OFF       1 = AM mute ON         Reserved : Fixed to "0"       IF_AGC_LEV : IF-AGC Level Control         0 = AGC slow mode       1 = AGC first mode         RF_AGC_LEV[1:0] : RF-AGC Level Control       0 = AGC slow mode         1 = AGC first mode       Sacconstructure         RF_AGC_LEV[1:0] : RF-AGC Level Control       0 = AGC slow mode         1 = AGC first mode       Sacconstructure         RF_AGC_LEV[1:0] : RF-AGC Level Control       0 = AGC slow mode         1 = AGC first mode       Sacconstructure         8 = AGC first mode       Sacconstructure         9 = AGC ormal mode       Sacconstructure         9 = AGC first mode       Sacconstructure         8 = AGC first mode       Sacconstructure         9 = AGC OFF       1 = AGC ON(Normal)	6       5       4       3       2         Reserved       EN_AMM       Reserved       IF_AGC_LEV       RF_AGC_LEV         Reserved : Fixed to "0"         Reserved : Fixed to "1"         EN_AMM : AM Mute ON/OFF         0 = AM mute OFF         1 = AM mute ON         Reserved : Fixed to "0"         IF_AGC_LEV : IF-AGC Level Control         0 = AGC slow mode         1 = AGC first mode         RF_AGC_LEV[1:0] : RF-AGC Level Control         0 = AGC slow mode         1 = AGC first mode         RF_AGC_LEV[1:0] : RF-AGC Level Control         0 = AGC slow mode         1 = AGC normal mode         3 = AGC first mode         EN_RFAGC : RF-AGC ON/OFF         0 = AGC OFF         1 = AGC ON (Normal)	6       5       4       3       2       1         Reserved       EN_AMM       Reserved       IF_AGC_LEV       RF_AGC_LEV[1:0]         Reserved : Fixed to "0"         Reserved : Fixed to "1"         EN_AMM : AM Mute ON/OFF         0 = AM mute OFF         1 = AM mute ON         Reserved : Fixed to "0"         IF_AGC_LEV : IF-AGC Level Control         0 = AGC slow mode         1 = AGC first mode         RF_AGC_LEV[1:0] : RF-AGC Level Control         0 = AGC slow mode         1 = AGC first mode         S = AGC first mode         EN_RFAGC : RF-AGC ON/OFF         0 = AGC OFF         1 = AGC ON (Normal)				

Register 1Al	Register 1Ah - RADIO_CTRL3 - Radio control 3 (Read/Write)										
7	6	5	4	3	2	1	0				
DEEM_100	NA		IF_AGC_CAP	AM_WIDE_A	GC_OFF	AM_WIDE_A	GC_ON				
Bit 7 :	DEEM_100 : Ac $0 = 0\mu s$ (Default $1 = 100\mu s$ (DEE	dditional De-em t setting) M = 1 : 75μS)	phasis (100µs)								
Bit 6 :	NA	NA									
Bit 4 :	$IF\_AGC\_CAP$ 0 = OFF (Normal) 1 = ON										
Bit 3-2 :	AM_WIDE_AGC_OFF[1:0] : AM WIDE AGC OFF Level Control 0 = First mode 3 = Slow mode										
Bit 1-0 :	AM_WIDE_AGC_ON[1:0] : AM WIDE AGC ON Level Control 0 = WIDE AGC OFF 1 = First mode 3 = Slow mode										

Register 1Ch - STEREO\_CTRL1 - Stereo control 1 (Read/Write)

					1	1					
7	6	5	4	3	2	1	0				
CRC[1:0]		SS_SP2	Reserved	Reserved	PICAN_EN	FOSTEREO	ST_M				
Bit 7-6 :	CRC[1:0] : Capture Range Control 0 = Narrow mode										
	3 = Wide mode										
D:+ 5 .											
BIL J.	0 : First mode - OFF										
	0. First mode – OFF 1. First mode – ON (Recommend)										
	1.115(1000 - 01)(100000000)										
Bit 4 :	Reserved : Fixed	l to "0"									
Bit 3 :	Reserved : Fixed to "0										
Bit 2 :	PICAN_EN : PI	LOT signal Cano	cellation ON/OF								
	0 = OFF										
	I = OIV (Recommend)										
Bit 1 :	FOSTEREO : Forced Stereo										
	0 = OFF (Normal)										
	1 = ON										
Bit 0 :	ST_M : Mono/Stereo setting										
	0 = Stereo on (Normal)										
	1 = Stereo off (F	Forced mono)									

7	6	5	4	3	2	1	0			
NA	·		FOAMAGC	Reserved	OVER_MOD	CPAJ[2:0]	·			
Bit 7-5 :	NA									
Bit 4 :	FOAMAGC									
	0: Forced - AGC = OFF									
	1 : Forced - AGC = ON									
Bit 3 :	Reserved: Fixed to "0"									
Bit 2 :	OVER_MOD : Over-modulation detector ON/OFF									
	0 = OFF									
	1 = ON									
Bit 1-0 :	CPAJ[1:0] : Cha	annel separati	on adjacent							
	0 = Minimum S	0 = Minimum Sub-signal level								
	7 - Maximum S	ub signal lay	al							

Register 1Eh - RADIO\_CTRL4 - Radio control 4 (Read/Write)

7	6	5	4	3	2	1	0			
SOFTST[2:0]			SOFTMU[2:0]			LEVSHIF	FO_SOFTT			
Bit 7-5 :	SOFTST[2:0] : S	Soft Stereo Funct	ion (Stereo-Blen	d)		·	•			
	0 : Soft Stereo =	OFF								
	7 : Soft Stereo = Lev7 (Max)									
Bit 4-2 :	: SOFTMU[2:0] : Soft Audio mute Function									
	0: Soft mute = $0$	OFF								
	7 : Soft mute = $Lev7$ (Max)									
Bit 1 :	it 1 : LEVSHIF : Audio Line-out DC level shift									
	$0 = \text{Normal DC level (V}_{CC} = 5.0\text{V})$									
	1 = DC level is shifted (V <sub>CC</sub> =9.0V)									
Bit 0: FO_SOFTST : Forced Soft Stereo Function										
	0 : ON (Normal)									
	1 : OFF									

Register 1Fh - RADIO_CTRL5 - Radio control 5 (Read/Write)									
7	6	5	4	3	2	1	0		
RF_SEL	IFRIM	nAGC_SPD	SE_FM/AM	AMP_CTR	MUTE	AM_CAL	PW_RAD		
Bit 7 :	RF_SEL : RF tuning range select 0 = Normal ( Japan/USA/Europe) 1 = OILT (65MHz to 74MHz)								
Bit 6 :	IFRIM : IF OSC limit setting 0 : Max = 350kHz (FM mode) 1 : Max = 150kHz (AM mode)								
Bit 5 :	nAGC_SPD : IF AGC speed setting 0 = High speed (FM mode) 1 = Normal (AM mode)								
Bit 4 :	SE_FM/AM : AM/FM mode select 0 = FM mode 1 = AM mode								
Bit 3 :	AMP_CTR : Audio Amp ON/OFF 0 = OFF 1 = ON								
Bit 2 :	MUTE : Audio Mute ON/OFF 0 = ON 1 = OFF								
Bit 1 :	AM_CAL : AM Calibration (Antenna tuning mode) 0 = AM Receiving mode (Normal) 1 = AM Calibration mode (AM antenna tuning mode)								
Note : Set this bit to "1", if ANT calibration frequency is measured.									
Bit 0 :	PW_RAD: Radio Power 0 = Power OFF (power save mode) 1 = Power ON								
<ul> <li>*1 : After the V<sub>CC</sub> voltage is impressed, PW_RAD is automatically set to "0" in 50ms.</li> <li>*2 : When the V<sub>CC</sub> voltage is dropped once, content of registers other than PW_RAD becomes irregular.</li> </ul>									

**Test Circuit** 



### **Application Circuit Example**



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