

# FRAM MB85R4M2T

The MB85R4M2T is an FRAM chip consisting of 262,144 words×16 bits of nonvolatile memory cells fabricated using ferroelectric process and CMOS process technologies.

The MB85R4M2T uses a pseudo-SRAM interface that is compatible with conventional asynchronous SRAM.

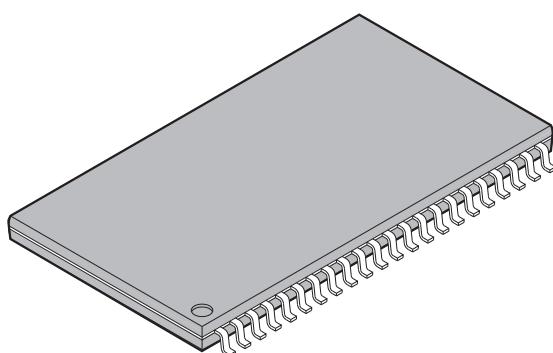
## FEATURES

- Bit configuration : 262,144 words×16 bits
- LB and UB data byte control : Available Configuration of 524,288 words × 8 bits
- Read/write endurance :  $10^{13}$  times / 16 bits
- Data retention : 10 years (+85 °C)
- Operating power supply voltage : 1.8V to 3.6V
- Low power operation : Operating power supply current 20 mA (Max)  
Standby current 150  $\mu$ A (Max)  
Sleep current 20  $\mu$ A (Max)
- Operation ambient temperature range : -40 °C to +85 °C
- Package : 44-pin plastic TSOP (FPT-44P-M34)  
RoHS compliant

## ORDERING INFORMATION

Product name	Package	Shipping form
MB85R4M2TFN-G-ASE1	44-pin plastic TSOP (FPT-44P-M34)	Tray

## OUTLINE OF PACKAGE



Plastic TSOP, 44-pin  
(FPT-44P-M34)

## PIN ASSIGNMENT

(TOP VIEW)

A4	1	44	A5
A3	2	43	A6
A2	3	42	A7
A1	4	41	/OE
A0	5	40	/UB
/CE	6	39	/LB
I/O0	7	38	I/O15
I/O1	8	37	I/O14
I/O2	9	36	I/O13
I/O3	10	35	I/O12
VDD	11	34	VSS
VSS	12	33	VDD
I/O4	13	32	I/O11
I/O5	14	31	I/O10
I/O6	15	30	I/O9
I/O7	16	29	I/O8
/WE	17	28	/ZZ
A17	18	27	A8
A16	19	26	A9
A15	20	25	A10
A14	21	24	A11
A13	22	23	A12

Pin name	Description
A0 to A17	Address Input pins
I/O0 to I/O15	Data Input / Output pins
/CE	Chip Enable Input pin
/WE	Write Enable Input pin
/OE	Output Enable Input pin
/ZZ	Sleep Mode Input pin
/LB, /UB	Lower/Upper byte Control Input pins
VDD	Supply Voltage pin
VSS	Ground pin

FPT-44P-M34

## BLOCK DIAGRAM

