2

256K x 4 CMOS Dynamic RAM
Page Mode

MCM514256B
MCM51L4256B

The MCM514256B is a 0.8μ CMOS high-speed, dynamic random access memory. It is organized as 262,144 four-bit words and fabricated with CMOS silicon-gate process technology. Advanced circuit design and fine line processing provide high performance, improved reliability, and low cost.

The MCM514256B requires only nine address lines; row and column address inputs are multiplexed. The device is packaged in a 300-mil SOJ plastic package, and a 100-mil zig-zag in-line package (ZIP).

- Three-State Data Output
- Fast Page Mode
- TTL-Compatible Inputs and Output
- $\overline{RAS}$ Only Refresh
- $\overline{CAS}$ Before $\overline{RAS}$ Refresh
- Hidden Refresh
- 512 Cycle Refresh:
    MCM514256B = 8 ms
    MCM51L4256B = 64 ms
- Unlatched Data Out at Cycle End Allows Two Dimensional Chip Selection
- Fast Access Time (t_{RAC}):
    MCM514256B-60 and MCM51L4256B-60 = 60 ns (Max)
    MCM514256B-80 and MCM51L4256B-80 = 80 ns (Max)
- Low Active Power Dissipation:
    MCM514256B-60 and MCM51L4256B-60 = 495 mW (Max)
    MCM514256B-80 and MCM51L4256B-80 = 385 mW (Max)
- Low Standby Power Dissipation:
    MCM514256B and MCM51L4256B = 11 mW (Max), TTL Levels
    MCM514256B = 5.5 mW (Max), CMOS Levels
    MCM51L4256B = 1.1 mW (Max), CMOS Levels

**J PACKAGE
300-MIL SOJ
CASE 822**
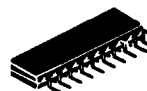
**Z PACKAGE
PLASTIC
ZIG-ZAG IN-LINE
CASE 836**

| PIN NAMES	
A0–A8	Address Input
DQ0–DQ3	Data Input/Output
$\overline{G}$	Output Enable
$\overline{W}$	Read/Write Input
$\overline{RAS}$	Row Address Strobe
$\overline{CAS}$	Column Address Strobe
V_{CC}	Power Supply (+ 5 V)
V_{SS}	Ground
NC	No Connection

PIN ASSIGNMENT

ZIG-ZAG IN-LINE
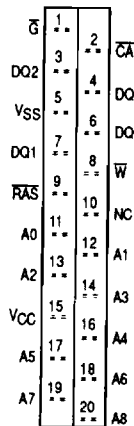
SMALL OUTLINE
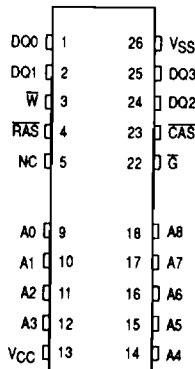
This document contains information on a new product. Specifications and information herein are subject to change without notice.

MCM514256B • MCM51L4256B

BLOCK DIAGRAM
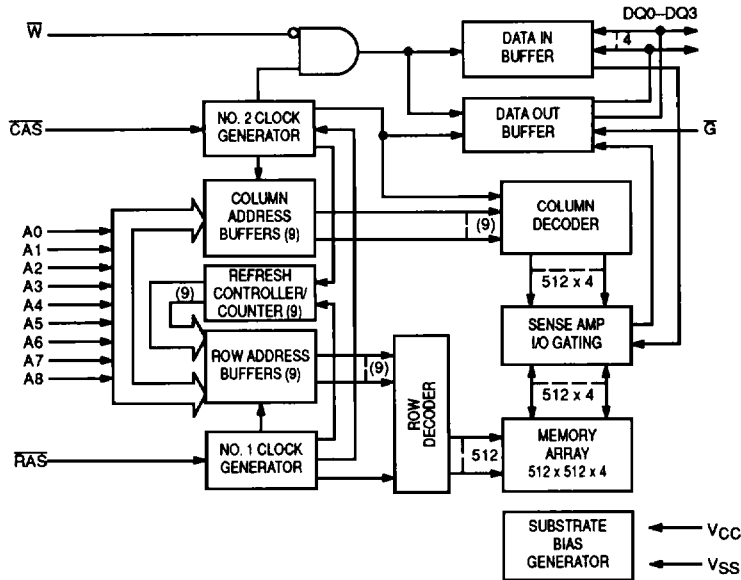
ABSOLUTE MAXIMUM RATING (See Note)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	–1 to +7	V
Voltage Relative to V_{SS} for Any Pin Except V_{CC}	V_{in}, V_{out}	–1 to +7	V
Data Out Current	I_{out}	50	mA
Power Dissipation	P_D	600	mW
Operating Temperature Range	T_A	0 to +70	°C
Storage Temperature Range	T_{stg}	–55 to +150	°C

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high-impedance circuit.

DC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ±10%, T_A = 0 to 70°C, Unless Otherwise Noted)

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Supply Voltage (Operating Voltage Range)	V_{CC}	4.5	5.0	5.5	V	1
	V_{SS}	0	0	0		
Logic High Voltage, All Inputs	V_{IH}	2.4	—	6.5	V	1
Logic Low Voltage, All Inputs	V_{IL}	–1.0	—	0.8	V	1

MCM514256B • MCM51L4256B

DC CHARACTERISTICS

Characteristic	Symbol	Min	Max	Unit	Notes
V$_{CC}$ Power Supply Current MCM514256B-60 and MCM51L4256B-60, t$_{RC}$ = 110 ns MCM514256B-80 and MCM51L4256B-80, t$_{RC}$ = 150 ns	I$_{CC1}$	— —	90 70	mA	3
V$_{CC}$ Power Supply Current (Standby) ($\overline{RAS}$=$\overline{CAS}$=V$_{IH}$) MCM514256B and MCM51L4256B	I$_{CC2}$	—	2	mA	
V$_{CC}$ Power Supply Current During $\overline{RAS}$ Only Refresh Cycles ($\overline{CAS}$=V$_{IH}$) MCM514256B-60 and MCM51L4256B-60, t$_{RC}$ = 110 ns MCM514256B-80 and MCM51L4256B-80, t$_{RC}$ = 150 ns	I$_{CC3}$	— —	90 70	mA	3
V$_{CC}$ Power Supply Current During Fast Page Mode Cycle ($\overline{RAS}$ = V$_{IL}$) MCM514256B-60 and MCM51L4256B-60, t$_{PC}$ = 40 ns MCM514256B-80 and MCM51L4256B-80, t$_{PC}$ = 45 ns	I$_{CC4}$	— —	60 50	mA	3, 4
V$_{CC}$ Power Supply Current (Standby) ($\overline{RAS}$=$\overline{CAS}$=V$_{CC}$–0.2 V) MCM514256B- MCM51L4256B-	I$_{CC5}$	— —	1.0 200	mA μA	
V$_{CC}$ Power Supply Current During $\overline{CAS}$ Before $\overline{RAS}$ Refresh Cycle MCM514256B-60 and MCM51L4256B-60, t$_{RC}$ = 110 ns MCM514256B-80 and MCM51L4256B-80, t$_{RC}$ = 150 ns	I$_{CC6}$	— —	90 70	mA	3
V$_{CC}$ Power Supply Current, Battery Backup Mode (t$_{RC}$ = 125 μs, t$_{RAS}$ = 1 μs, $\overline{CAS}$=$\overline{CAS}$ Before $\overline{RAS}$ Cycle or 0.2 V, A0–A8, $\overline{W}$, D = V$_{CC}$ – 0.2 V or 0.2 V) MCM51L4256B-	I$_{CC5}$	—	300	μA	3
Input Leakage Current (0 V ≤ V$_{in}$ ≤ 6.5 V)	I$_{lkg(I)}$	–10	10	μA	
Output Leakage Current ($\overline{CAS}$ = V$_{IH}$, 0 V ≤ V$_{out}$ ≤ 5.5 V, Output Disable)	I$_{lkg(O)}$	–10	10	μA	
Output High Voltage (I$_{OH}$ = –5 mA)	V$_{OH}$	2.4	—	V	
Output Low Voltage (I$_{OL}$ = 4.2 mA)	V$_{OL}$	—	0.4	V	

CAPACITANCE (f = 1.0 MHz, T$_A$ = 25°C, V$_{CC}$ = 5 V, Periodically Sampled Rather Than 100% Tested)

Parameter		Symbol	Max	Unit	Notes
Input Capacitance	A0–A8	C$_{in}$	5	pF	4
	$\overline{G}$, $\overline{RAS}$, $\overline{CAS}$, $\overline{W}$		7		
I/O Capacitance ($\overline{CAS}$ = V$_{IH}$ to Disable Output)	DQ0–DQ3	C$_{out}$	7	pF	4

NOTES:
1. All voltages referenced to V$_{SS}$.
2. Current is a function of cycle rate and output loading; maximum current is measured at the fastest cycle rate with the output open.
3. Measured with one address transition per page mode cycle.
4. Capacitance measured with a Boonton Meter or effective capacitance calculated from the equation: C = IΔt/ΔV.

MCM514256B • MCM51L4256B

AC OPERATING CONDITIONS AND CHARACTERISTICS

$(V_{CC} = 5.0 \text{ V} \pm 10\%, T_A = 0 \text{ to } 70°C, \text{ Unless Otherwise Noted})$

READ, WRITE, AND READ-WRITE CYCLES (See Notes 1, 2, 3, and 4)

Parameter	Symbol		MCM514256B-60 MCM51L4256B-60		MCM514256B-80 MCM51L4256B-80		Units	Notes
	Std	Alt	Min	Max	Min	Max		
Random Read or Write Cycle Time	t_{RELREL}	t_{RC}	110	—	150	—	ns	5
Read-Write Cycle Time	t_{RELREL}	t_{RMW}	165	—	205	—	ns	5
Fast Page Mode Cycle Time	t_{CELCEL}	t_{PC}	40	—	45	—	ns	
Fast Page Mode Read-Write Cycle Time	t_{CELCEL}	t_{PRMW}	95	—	100	—	ns	
Access Time from $\overline{RAS}$	t_{RELQV}	t_{RAC}	—	60	—	80	ns	6, 7
Access Time from $\overline{CAS}$	t_{CELQV}	t_{CAC}	—	20	—	20	ns	6, 8
Access Time from Column Address	t_{AVQV}	t_{AA}	—	30	—	40	ns	6, 9
Access Time from $\overline{CAS}$ Precharge	t_{CEHQV}	t_{CPA}	—	35	—	45	ns	6
$\overline{CAS}$ to Output in Low-Z	t_{CELQX}	t_{CLZ}	0	—	0	—	ns	6
Output Buffer and Turn-Off Delay	t_{CEHQZ}	t_{OFF}	0	20	0	20	ns	10
Transition Time (Rise and Fall)	t_T	t_T	3	50	3	50	ns	
$\overline{RAS}$ Precharge Time	t_{REHREL}	t_{RP}	40	—	60	—	ns	
$\overline{RAS}$ Pulse Width	t_{RELREH}	t_{RAS}	60	10,000	80	10,000	ns	
$\overline{RAS}$ Pulse Width (Fast Page Mode)	t_{RELREH}	t_{RASP}	60	100,000	80	100,000	ns	
$\overline{RAS}$ Hold Time	t_{CELREH}	t_{RSH}	20	—	20	—	ns	
$\overline{RAS}$ Hold Time from $\overline{CAS}$ Precharge (Page Mode Cycle Only)	t_{CELREH}	t_{RHCP}	35	—	40	—	ns	
$\overline{CAS}$ Hold Time	t_{RELCEH}	t_{CSH}	60	—	80	—	ns	
$\overline{CAS}$ Pulse Width	t_{CELCEH}	t_{CAS}	20	10,000	20	10,000	ns	
$\overline{RAS}$ to $\overline{CAS}$ Delay Time	t_{RELCEL}	t_{RCD}	20	40	20	60	ns	11
$\overline{RAS}$ to Column Address Delay Time	t_{RELAV}	t_{RAD}	15	30	15	40	ns	12
$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	t_{CEHREL}	t_{CRP}	5	—	5	—	ns	
$\overline{CAS}$ Precharge Time	t_{CEHCEL}	t_{CP}	10	—	10	—	ns	
Row Address Setup Time	t_{AVREL}	t_{ASR}	0	—	0	—	ns	
Row Address Hold Time	t_{RELAX}	t_{RAH}	10	—	10	—	ns	

(continued)

NOTES:
1. V_{IH} min and V_{IL} max are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} and V_{IL}.
2. An initial pause of 200 μs is required after power-up followed by 8 $\overline{RAS}$ cycles before proper device operation is guaranteed.
3. The transition time specification applies for all input signals. In addition to meeting the transition rate specification, all input signals must transition between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}) in a monotonic manner.
4. AC measurements $t_T = 5.0$ ns.
5. The specifications for t_{RC} (min) and t_{RMW} (min) are used only to indicate cycle time at which proper operation over the full temperature range $(0°C \leq T_A \leq 70°C)$ is assured.
6. Measured with a current load equivalent to 2 TTL $(- 200 \text{ μA}, + 4 \text{ mA})$ loads and 100 pF with the data output trip points set at $V_{OH} = 2.0$ V and $V_{OL} = 0.8$ V.
7. Assumes that $t_{RCD} \leq t_{RCD}$ (max).
8. Assumes that $t_{RCD} \geq t_{RCD}$ (max).
9. Assumes that $t_{RAD} \geq t_{RAD}$ (max).
10. t_{OFF} (max) and/or t_{GZ} (max) defines the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.
11. Operation within the t_{RCD} (max) limit ensures that t_{RAC} (max) can be met. t_{RCD} (max) is specified as a reference point only; if t_{RCD} is greater than the specified t_{RCD} (max) limit, then access time is controlled exclusively by t_{CAC}.
12. Operation within the t_{RAD} (max) limit ensures that t_{RAC} (max) can be met. t_{RAD} (max) is specified as a reference point only; if t_{RAD} is greater than the specified t_{RAD} (max) limit, then access time is controlled exclusively by t_{AA}.

MCM514256B • MCM51L4256B

READ, WRITE, AND READ-WRITE CYCLES (Continued)

| Parameter	Symbol		MCM514256B-60 MCM51L4256B-60		MCM514256B-80 MCM51L4256B-80		Unit	Notes
	Std	Alt	Min	Max	Min	Max		
Column Address Setup Time	t_{AVCEL}	t_{ASC}	0	—	0	—	ns	
Column Address Hold Time	t_{CELAX}	t_{CAH}	15	—	15	—	ns	
Column Address Hold Time Referenced to RAS	t_{RELAX}	t_{AR}	50	—	60	—	ns	
Column Address to RAS Lead Time	t_{AVREH}	t_{RAL}	30	—	40	—	ns	
Read Command Setup Time	t_{WHCEL}	t_{RCS}	0	—	0	—	ns	
Read Command Hold Time	t_{CEHWX}	t_{RCH}	0	—	0	—	ns	13
Read Command Hold Time Referenced to RAS	t_{REHWX}	t_{RRH}	0	—	0	—	ns	13
Write Command Hold Time Referenced to CAS	t_{CELWH}	t_{WCH}	10	—	15	—	ns	
Write Command Hold Time Referenced to RAS	t_{RELWH}	t_{WCR}	45	—	60	—	ns	
Write Command Pulse Width	t_{WLWH}	t_{WP}	10	—	15	—	ns	
Write Command to RAS Lead Time	t_{WLREH}	t_{RWL}	20	—	20	—	ns	
Write Command to CAS Lead Time	t_{WLCEH}	t_{CWL}	20	—	20	—	ns	
Data in Setup Time	t_{DVCEL}	t_{DS}	0	—	0	—	ns	14
Data in Hold Time	t_{CELDX}	t_{DH}	15	—	15	—	ns	14
Data in Hold Time Referenced to RAS	t_{RELDX}	t_{DHR}	50	—	60	—	ns	
Refresh Period MCM514256B	t_{RVRV}	t_{RFSH}	—	8	—	8	ms	
MCM51L4256B			—	64	—	64		
Write Command Setup Time	t_{WLCEL}	t_{WCS}	0	—	0	—	ns	15
CAS to Write Delay	t_{CELWL}	t_{CWD}	50	—	50	—	ns	15
RAS to Write Delay	t_{RELWL}	t_{RWD}	90	—	110	—	ns	15
Column Address to Write Delay Time	t_{AVWL}	t_{AWD}	60	—	70	—	ns	15
CAS Precharge to Write Delay	t_{CEHWL}	t_{CPWD}	65	—	70	—	ns	15
CAS Setup Time for CAS Before RAS Refresh	t_{RELCEL}	t_{CSR}	5	—	5	—	ns	
CAS Hold Time for CAS Before RAS Refresh	t_{RELCEH}	t_{CHR}	15	—	15	—	ns	
RAS Precharge to CAS Active Time	t_{REHCEL}	t_{RPC}	0	—	0	—	ns	
CAS Precharge Time for CAS Before RAS Counter Test	t_{CEHCEL}	t_{CPT}	30	—	40	—	ns	
RAS Hold Time Referenced to G	t_{GLREH}	t_{ROH}	10	—	10	—	ns	
G Access Time	t_{GLQV}	t_{GA}	—	20	—	20	ns	
G to Data Delay	t_{GLHDX}	t_{GD}	20	—	20	—	ns	
Output Buffer Turn-Off Delay Time from G	t_{GHQZ}	t_{GZ}	0	20	0	20	ns	10
G Command Hold Time	t_{WLGL}	t_{GH}	20	—	20	—	ns	
Output Disable Setup Time	t_{GHCEL}	t_{GS}	0	—	0	—	ns	

NOTES:
13. Either t_{RRH} or t_{RCH} must be satisfied for a read cycle.
14. These parameters are referenced to CAS leading edge in early write cycles and to W leading edge in delayed write or read-write cycles.
15. t_{WCS}, t_{RWD}, t_{CWD}, t_{CPWD}, and t_{AWD} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only; if $t_{WCS} \geq t_{WCS}$ (min), the cycle is an early write cycle and the data out pin will remain open circuit (high impedance) throughout the entire cycle; if $t_{CWD} \geq t_{CWD}$ (min), $t_{RWD} \geq t_{RWD}$ (min), $t_{CPWD} \geq t_{CPWD}$ (min), and $t_{AWD} \geq t_{AWD}$ (min), the cycle is a read-write cycle and the data out will contain data read from the selected cell. If neither of these sets of conditions is satisfied, the condition of the data out (at access time) is indeterminate.
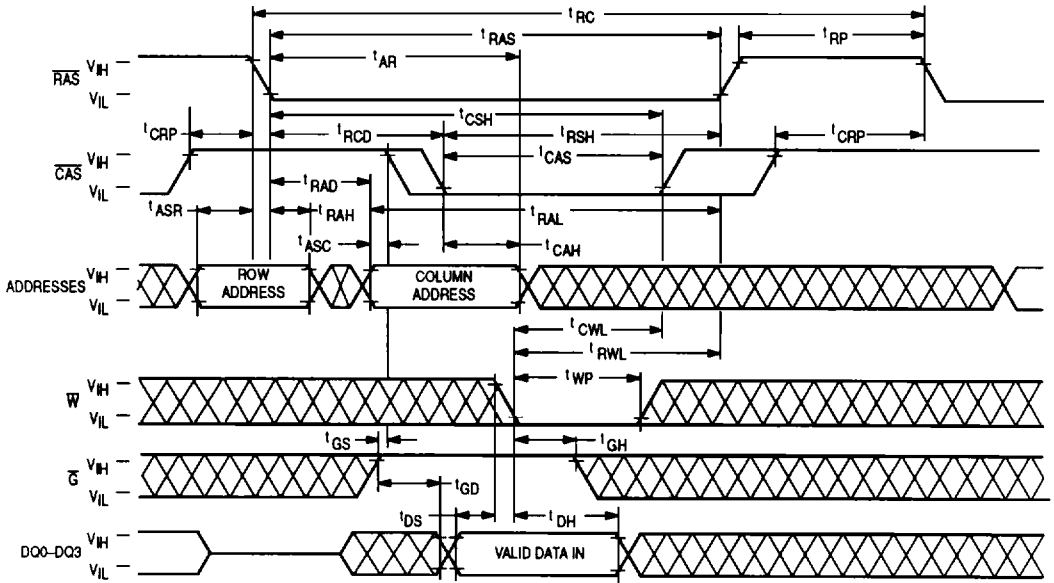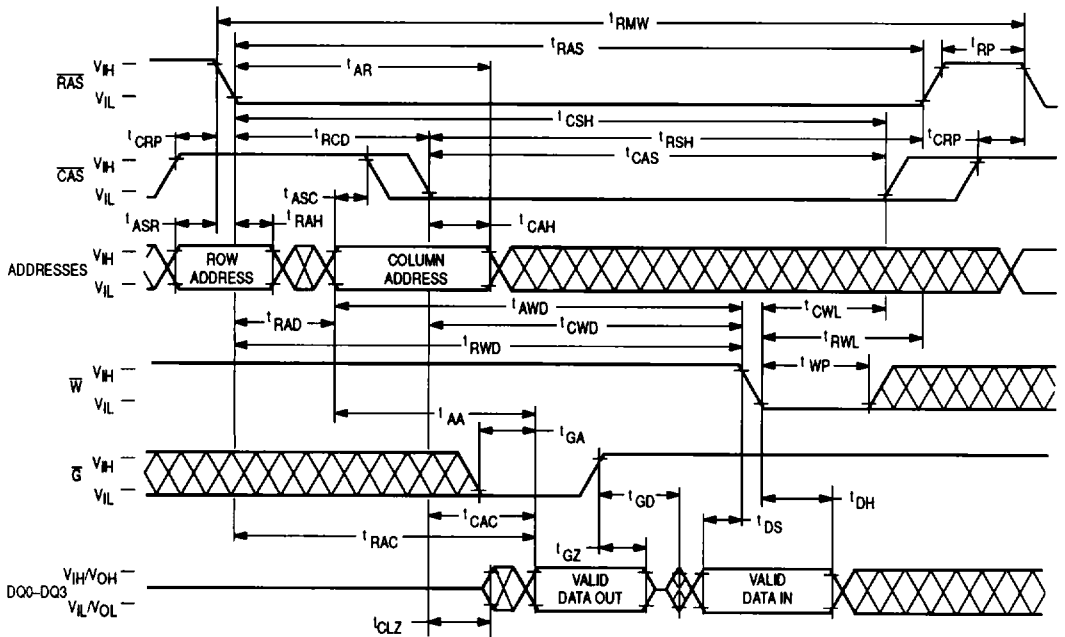
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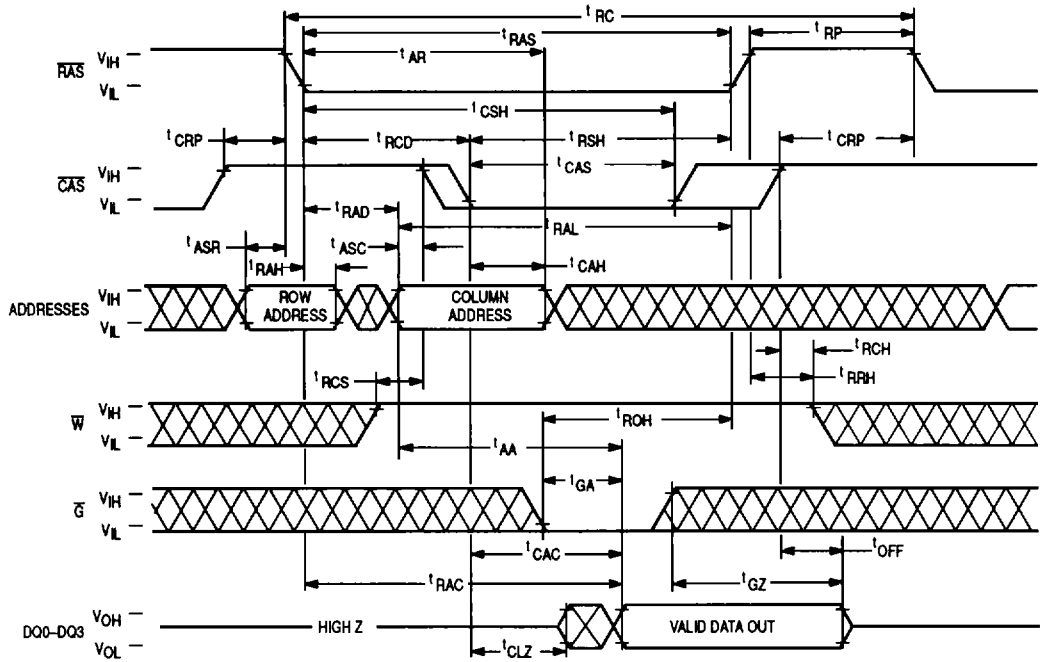
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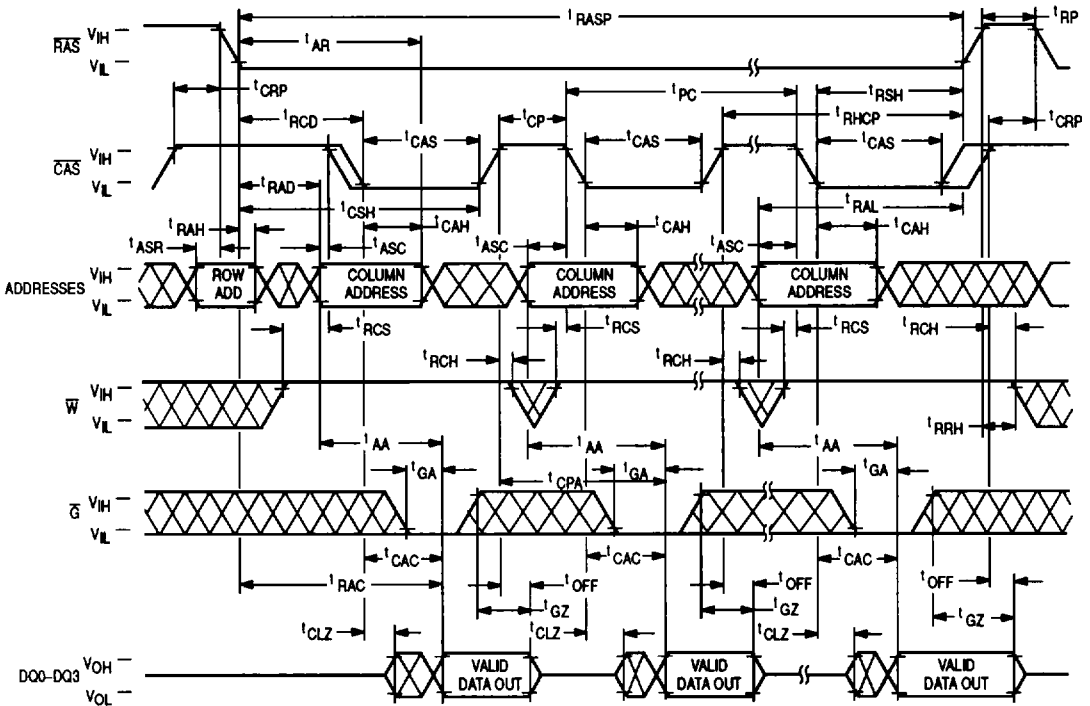
EARLY WRITE CYCLE
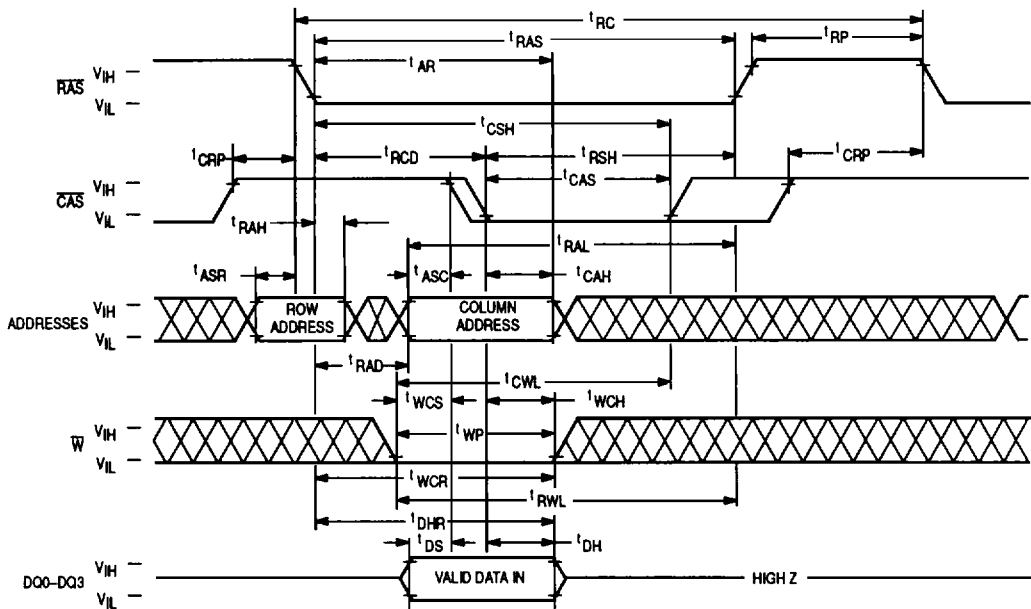
MOTOROLA MEMORY DATA

$\overline{G}$ CONTROLLED LATE WRITE CYCLE

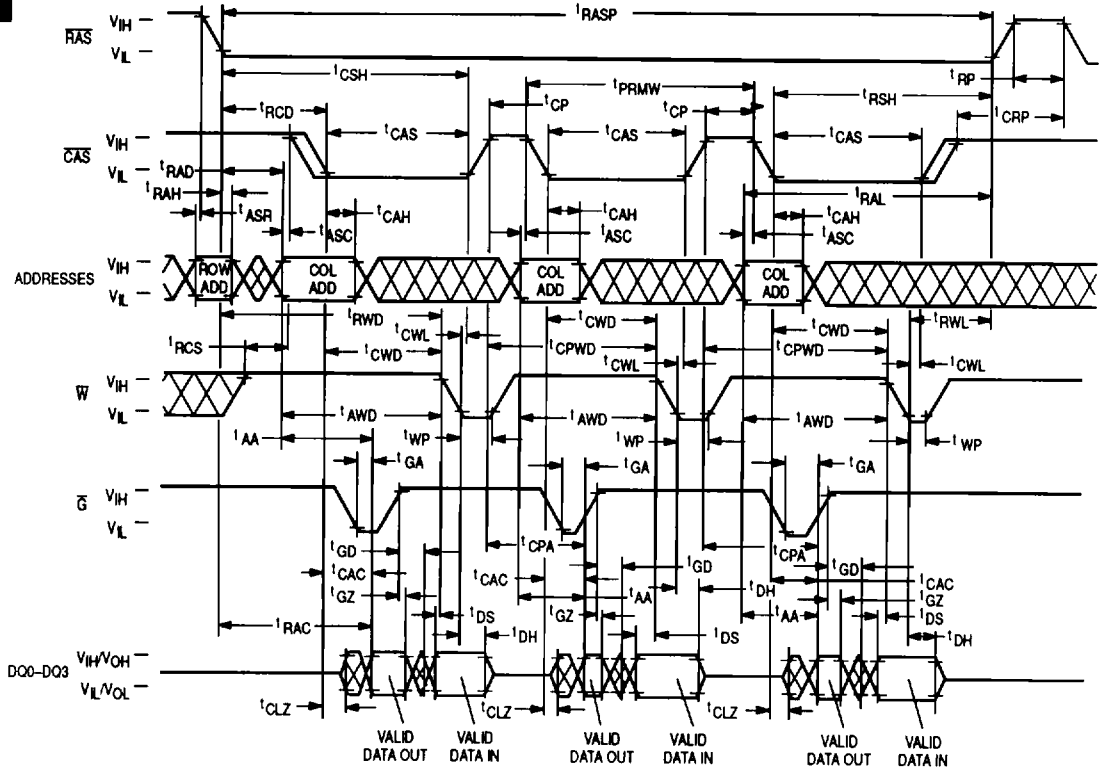## READ-WRITE CYCLE

MOTOROLA MEMORY DATA

FAST PAGE MODE READ CYCLE

FAST PAGE MODE EARLY WRITE CYCLE

2

FAST PAGE MODE READ-WRITE CYCLE

MCM514256B • MCM51L4256B

RAS ONLY REFRESH CYCLE
(W and G are Don't Care)
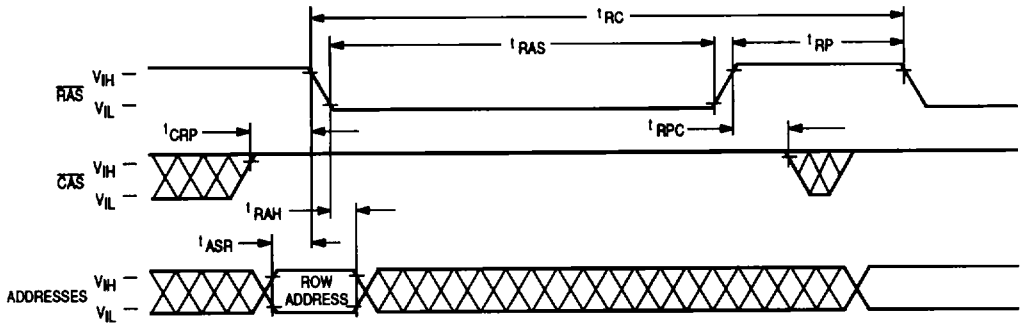
CAS BEFORE RAS REFRESH CYCLE
(W, G, and A0–A8 are Don't Care)

2

HIDDEN REFRESH CYCLE (READ)

HIDDEN REFRESH CYCLE (EARLY WRITE)
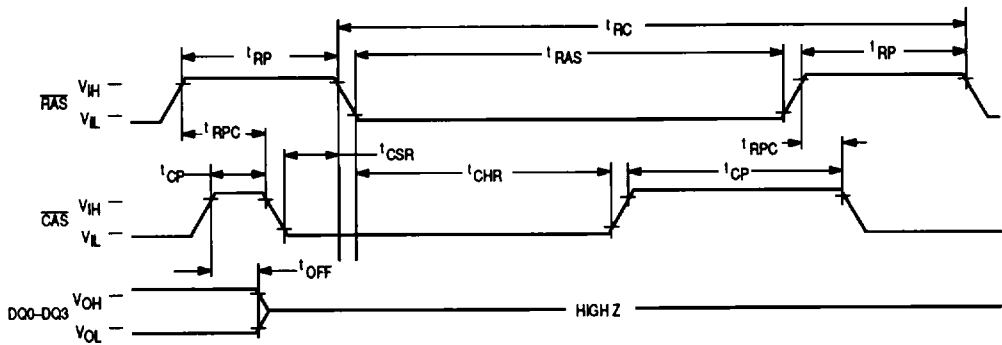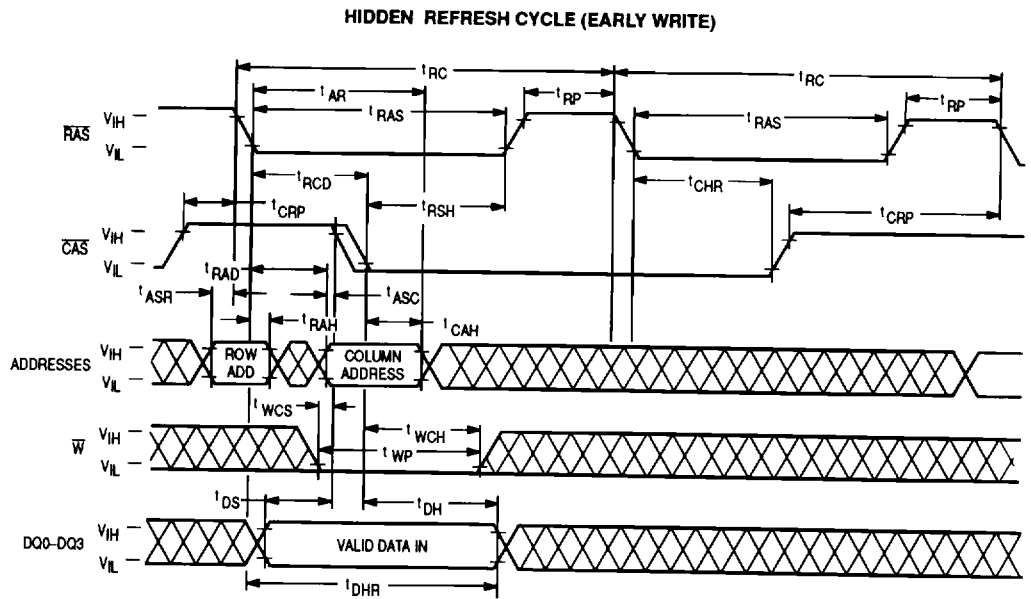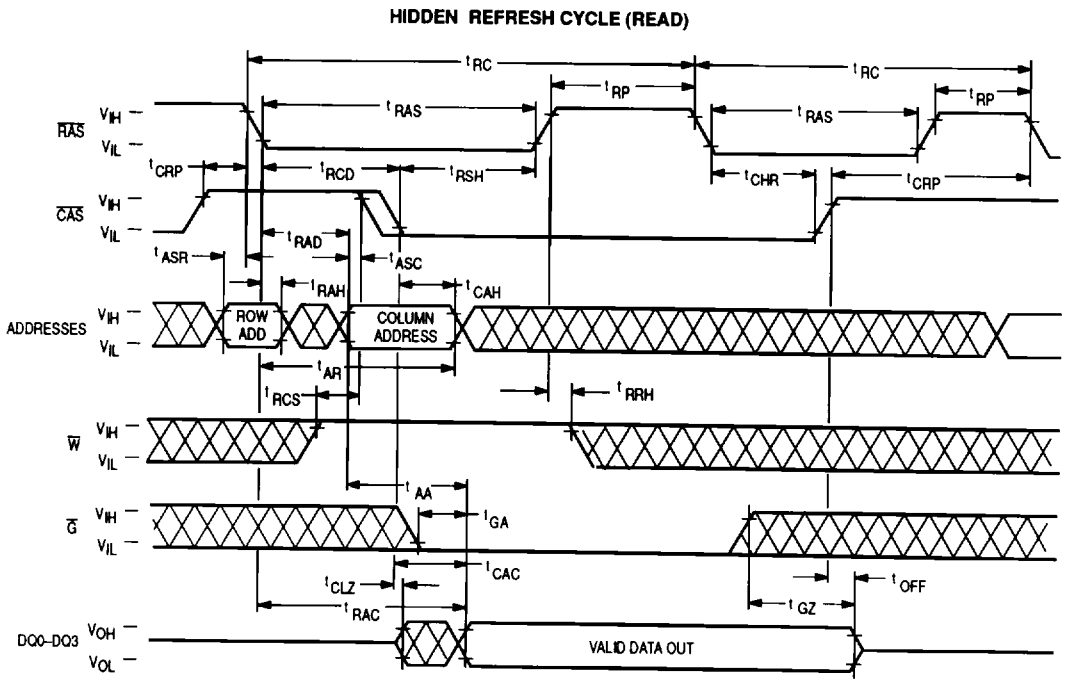
$\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH COUNTER TEST CYCLE
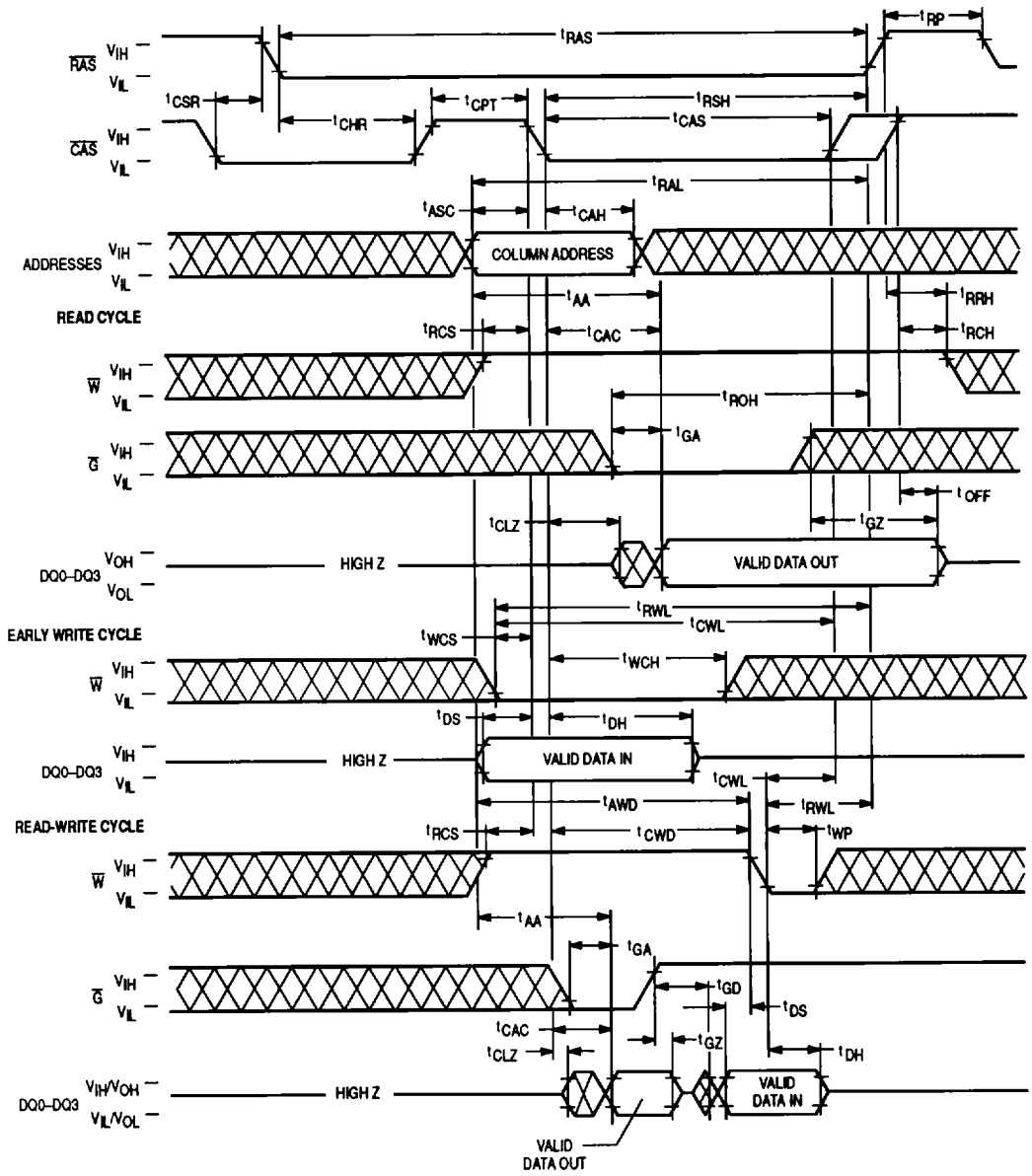
DEVICE INITIALIZATION

On power-up an initial pause of 200 microseconds is required for the internal substrate generator to establish the correct bias voltage. This must be followed by a minimum of eight active cycles of the row address strobe (clock) to initialize all dynamic nodes within the RAM. During an extended inactive state (greater than 8 milliseconds with the device powered up), a wakeup sequence of eight active cycles is necessary to ensure proper operation.

ADDRESSING THE RAM

The nine address pins on the device are time multiplexed at the beginning of a memory cycle by two clocks, row address strobe ($\overline{RAS}$) and column address strobe ($\overline{CAS}$), into two separate 9-bit address fields. A total of eighteen address bits, nine rows and nine columns, will decode one of the 262,144 bit locations in the device. $\overline{RAS}$ active transition is followed by $\overline{CAS}$ active transition (active = V_{IL}, t_{RCD} minimum) for all read or write cycles. The delay between $\overline{RAS}$ and $\overline{CAS}$ active transitions, referred to as the **multiplex window**, gives a system designer flexibility in setting up the external addresses into the RAM.

The external $\overline{CAS}$ signal is ignored until an internal $\overline{RAS}$ signal is available. This gate feature on the external $\overline{CAS}$ clock enables the internal $\overline{CAS}$ line as soon as the row address hold time (t_{RAH}) specification is met (and defines t_{RCD} minimum). The multiplex window can be used to absorb skew delays in switching the address bus from row to column addresses and in generating the $\overline{CAS}$ clock.

There are two other variations in addressing the 256Kx4 RAM: $\overline{RAS}$ only refresh cycle and $\overline{CAS}$ before $\overline{RAS}$ refresh cycle. Both are discussed in separate sections that follow.

READ CYCLE

The DRAM may be read with four different cycles: normal random read cycle, page mode read cycle, read-write cycle, and page mode read-write cycle. The normal read cycle is outlined here, while the other cycles are discussed in separate sections.

The normal read cycle begins as described in **ADDRESSING THE RAM**, with $\overline{RAS}$ and $\overline{CAS}$ active transitions latching the desired bit location. The write ($\overline{W}$) input level must be high (V_{IH}), t_{RCS} (minimum) before the $\overline{CAS}$ active transition, to enable read mode.

Both the $\overline{RAS}$ and $\overline{CAS}$ clocks trigger a sequence of events which are controlled by several delayed internal clocks. The internal clocks are linked in such a manner that the read access time of the device is independent of the address multiplex window. Both $\overline{CAS}$ and output enable ($\overline{G}$) control read access time: $\overline{CAS}$ must be active before or at t_{RCD} maximum and $\overline{G}$ must be active t_{RAC}-t_{GA} (both minimum) after $\overline{RAS}$ active transition to guarantee valid data out (Q) at t_{RAC} (access time from $\overline{RAS}$ active transition). If the t_{RCD} maximum is exceeded and/or $\overline{G}$ active transition does not occur in time, read access time is determined by either the $\overline{CAS}$ or $\overline{G}$ clock active transition (t_{CAC} or t_{GA}).

The $\overline{RAS}$ and $\overline{CAS}$ clocks must remain active for a minimum time of t_{RAS} and t_{CAS} respectively, to complete the read cycle. $\overline{W}$ must remain high throughout the cycle, and for time t_{RRH} or t_{RCH} after $\overline{RAS}$ or $\overline{CAS}$ inactive transition, respectively, to maintain the data at that bit location. Once $\overline{RAS}$ transitions to inactive, it must remain inactive for a minimum time of t_{RP} to precharge the internal device circuitry for the next active

cycle. Q is valid, but not latched, as long as the $\overline{CAS}$ and $\overline{G}$ clocks are active. When either the $\overline{CAS}$ or $\overline{G}$ clock transitions to inactive, the output will switch to High Z, t_{OFF} or t_{GZ} after the inactive transition.

WRITE CYCLE

The DRAM may be written with any of four cycles: early write, late write, page mode early write, and page mode read-write. Early and late write modes are discussed here, while page mode write operations are covered in another section.

A write cycle begins as described in **ADDRESSING THE RAM**. Write mode is enabled by the transition of $\overline{W}$ to active (V_{IL}). Early and late write modes are distinguished by the active transition of $\overline{W}$, with respect to $\overline{CAS}$. Minimum active time t_{RAS} and t_{CAS}, and precharge time t_{RP} apply to write mode, as in the read mode.

An early write cycle is characterized by $\overline{W}$ active transition at minimum time t_{WCS} before $\overline{CAS}$ active transition. Data In (D) is referenced to $\overline{CAS}$ in an early write cycle. $\overline{RAS}$ and $\overline{CAS}$ clocks must stay active for t_{RWL} and t_{CWL}, respectively, after the start of the early write operation to complete the cycle.

Q remains High Z throughout an early write cycle because $\overline{W}$ active transition precedes or coincides with $\overline{CAS}$ active transition, keeping data out buffers disabled, effectively disabling $\overline{G}$.

A late write cycle (referred to as $\overline{G}$ controlled write) occurs when $\overline{W}$ active transition is made after $\overline{CAS}$ active transition. $\overline{W}$ active transition could be delayed for almost 10 microseconds after $\overline{CAS}$ active transition, ($t_{RCD} + t_{CWD} + t_{RWL} + t_T$) $\leq t_{RAS}$, if timing minimums (t_{RCD}, t_{RWL}, and t_T) are maintained. D is referenced to $\overline{W}$ active transition in a late write cycle. Output buffers are enabled by $\overline{CAS}$ active transition but Q may be indeterminate—see note 15 of AC operating conditions table. Parameters t_{RWL} and t_{CWL} also apply to late write cycles.

READ-WRITE CYCLE

A read-write cycle performs a read and then a write at the same address, during the same cycle. This cycle is basically a late write cycle, as discussed in the **WRITE CYCLE** section, except $\overline{W}$ must remain high for t_{CWD} minimum after the $\overline{CAS}$ active transition, to guarantee valid Q before writing the bit.

PAGE MODE CYCLES

Page mode allows fast successive data operations at all 512 column locations on a selected row of the 256Kx4 dynamic RAM. Read access time in page mode (t_{CAC}) is typically half the regular $\overline{RAS}$ clock access time, t_{RAC}. Page mode operation consists of keeping $\overline{RAS}$ active while toggling $\overline{CAS}$ between V_{IH} and V_{IL}. The row is latched by $\overline{RAS}$ active transition, while each $\overline{CAS}$ active transition allows selection of a new column location on the row.

A page mode cycle is initiated by a normal read, write, or read-write cycle, as described in prior sections. Once the timing requirements for the first cycle are met, $\overline{CAS}$ transitions to inactive for minimum t_{CP}, while $\overline{RAS}$ remains low (V_{IL}). The second $\overline{CAS}$ active transition while $\overline{RAS}$ is low initiates the first page mode cycle (t_{PC} or t_{PRWC}). Either a read, write, or read-write operation can be performed in a page mode cycle, subject to the same conditions as in normal operation (previously described). These operations can be intermixed in consecutive page mode cycles and performed in any order. The maximum number of consecutive page mode cycles is limited by t_{RASP}. Page mode operation is ended when $\overline{RAS}$

MOTOROLA MEMORY DATA

transitions to inactive, coincident with or following $\overline{CAS}$ inactive transition.

REFRESH CYCLES

The dynamic RAM design is based on capacitor charge storage for each bit in the array. This charge degrades with time and temperature, thus each bit must be periodically refreshed (recharged) to maintain the correct bit state. Bits in the MCM514256B require refresh every 8 milliseconds while refresh time for the MCM51L4256B is 64 milliseconds..

Refresh is accomplished by cycling through the 512 row addresses in sequence within the specified refresh time. All the bits on a row are refreshed simultaneously when the row is addressed. Distributed refresh implies a row refresh every 15.6 microseconds for the MCM514256B and 124.8 microseconds for the MCM51L4256B. Burst refresh, a refresh of all 512 rows consecutively, must be performed every 8 milliseconds on the MCM514256B and 64 milliseconds on the MCM51L4256B.

A normal read, write, or read-write operation to the RAM will refresh all the bits (2048) associated with the particular row decoded. Three other methods of refresh, $\overline{RAS}$-only refresh, $\overline{CAS}$ before $\overline{RAS}$ refresh, and Hidden refresh are available on this device for greater system flexibility.

$\overline{RAS}$-Only Refresh

$\overline{RAS}$-only refresh consists of $\overline{RAS}$ transition to active, latching the row address to be refreshed, while $\overline{CAS}$ remains high (V_{IH}) throughout the cycle. An external counter is employed to ensure all rows are refreshed within the specified limit.

$\overline{CAS}$ Before $\overline{RAS}$ Refresh

$\overline{CAS}$ before $\overline{RAS}$ refresh is enabled by bringing $\overline{CAS}$ active before $\overline{RAS}$. This clock order actives an internal refresh counter that generates the row address to be refreshed. External address lines are ignored during the automatic refresh cycle. The output buffer remains at the same state it was in during the previous cycle (hidden refresh).

Hidden Refresh

Hidden refresh allows refresh cycles to occur while maintaining valid data at the output pin. Holding $\overline{CAS}$ active at the end of a read or write cycle, while $\overline{RAS}$ cycles inactive for t_{RP} and back to active, starts the hidden refresh. This is essentially the execution of a $\overline{CAS}$ before $\overline{RAS}$ refresh from a cycle in progress (see Figure 1).

$\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH COUNTER TEST

The internal refresh counter of this device can be tested with a $\overline{CAS}$ before $\overline{RAS}$ refresh counter test. This test is performed with a read-write operation. During the test, the internal refresh counter generates the row address, while the external address supplies the column address. The entire array is refreshed after 512 cycles, as indicated by the check data written in each row. See $\overline{CAS}$ before $\overline{RAS}$ refresh counter test cycle timing diagram.

The test can be performed after a minimum of eight $\overline{CAS}$ before $\overline{RAS}$ initialization cycles. Test procedure:

1. Write "0"s into all memory cells with normal write mode.
2. Select a column address, read "0" out and write "1" into the cell by performing the $\overline{CAS}$ before $\overline{RAS}$ refresh counter test, read-write cycle. Repeat this operation 512 times.
3. Read the "1"s which were written in step 2 in normal read mode.
4. Using the same starting column address as in step 2, read "1" out and write "0" into the cell by performing the $\overline{CAS}$ before $\overline{RAS}$ refresh counter test, read-write cycle. Repeat this operation 512 times.
5. Read "0"s which were written in step 4 in normal read mode.
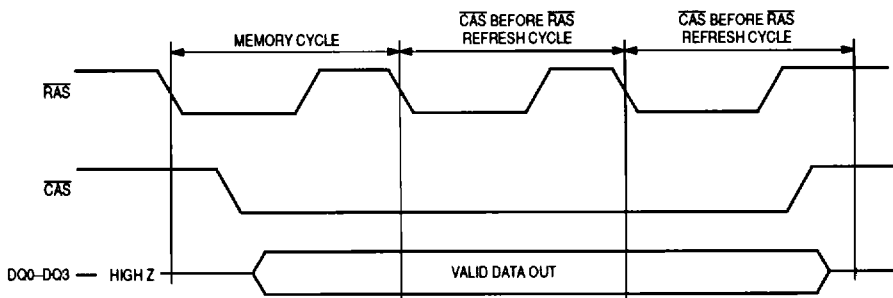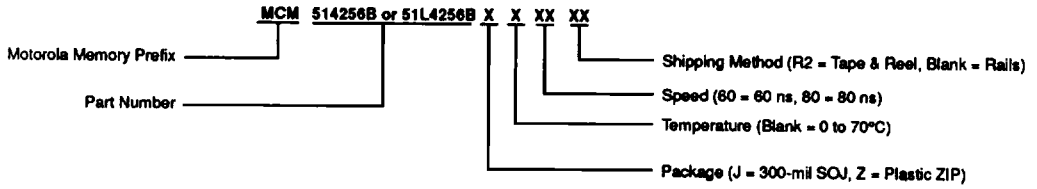6. Repeat steps 1 to 5 using complement data.

Figure 1. Hidden Refresh Cycle

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ORDERING INFORMATION
(Order by Full Part Number)

MCM 514256B or 51L4256B X X XX XX

Motorola Memory Prefix

Part Number

Shipping Method (R2 = Tape & Reel, Blank = Rails)

Speed (60 = 60 ns, 80 = 80 ns)

Temperature (Blank = 0 to 70°C)

Package (J = 300-mil SOJ, Z = Plastic ZIP)

Commercial Temperature Range 0 to 70°C

Full Part Numbers—		
MCM514256BJ60	MCM514256BJ60R2	MCM514256BZ60
MCM514256BJ80	MCM514256BJ80R2	MCM514256BZ80
MCM51L4256BJ60	MCM51L4256BJ60R2	MCM51L4256BZ60
MCM51L4256BJ80	MCM51L4256BJ80R2	MCM51L4256BZ80