MSM6544

84-DOT LCD DRIVER

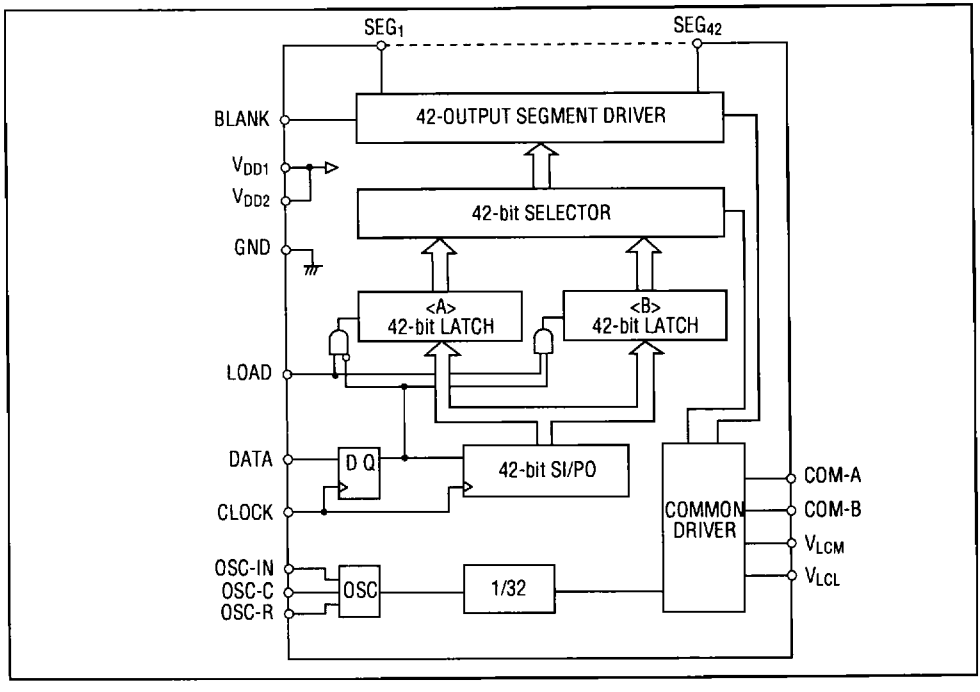
GENERAL DESCRIPTION

The MSM6544 is a dual, 42-segment duplex driver which can drive LCD panel up to a maximum of 84 segments.
The LCD module can be compactly fabricated using a 56-pin QFP. An internal RC oscillator is provided for ease of use.

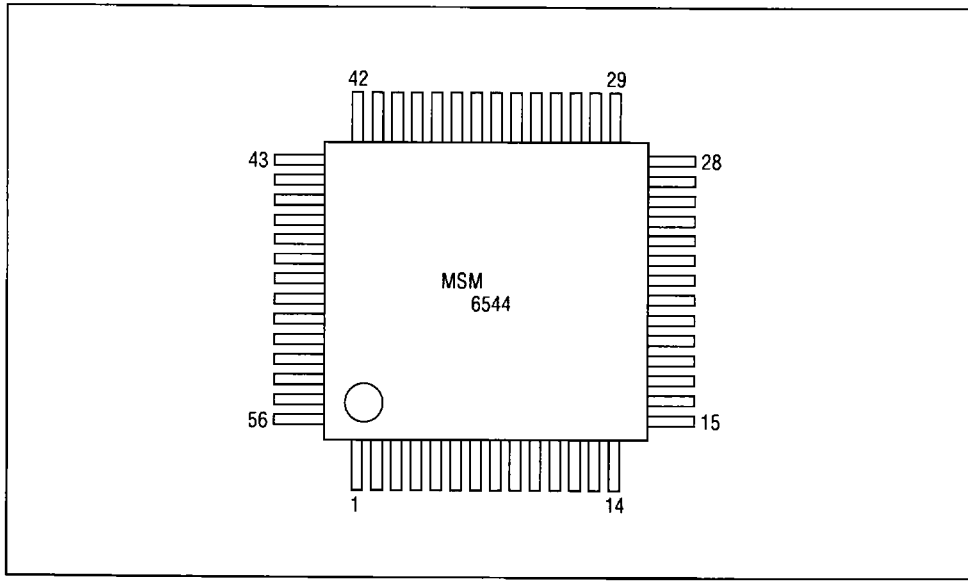
FEATURES

- Power supply voltage (V_{DD}) : 3 to 6V
- LCD driving voltage : 3 to V_{DD}
- Operating temperature : -40 to +85°C
- Applicable LCD panel : 1/2 duty 84 (MAX) segments
- Data transmitting clock : 4 MHz (MAX)
- Package : 56-Pin Plastic QFP (QFP56-P-910-K)
  : 56-Pin V Plastic QFP (QFP56-P-910-VK)

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATION



1	SEG_{29}	15	OSC-IN	29	SEG_2	43	SEG_{16}
2	SEG_{30}	16	OSC-C	30	SEG_3	44	SEG_{17}
3	SEG_{31}	17	OSC-R	31	SEG_4	45	SEG_{18}
4	SEG_{32}	18	LOAD	32	SEG_5	46	SEG_{19}
5	SEG_{33}	19	DATA	33	SEG_6	47	SEG_{20}
6	SEG_{34}	20	CLOCK	34	SEG_7	48	SEG_{21}
7	SEG_{35}	21	V_{DD1}	35	SEG_8	49	V_{DD2}
8	SEG_{36}	22	BLANK	36	SEG_9	50	SEG_{22}
9	SEG_{37}	23	GND	37	SEG_{10}	51	SEG_{23}
10	SEG_{38}	24	V_{LCL}	38	SEG_{11}	52	SEG_{24}
11	SEG_{39}	25	COM-A	39	SEG_{12}	53	SEG_{25}
12	SEG_{40}	26	V_{LCM}	40	SEG_{13}	54	SEG_{26}
13	SEG_{41}	27	COM-B	41	SEG_{14}	55	SEG_{27}
14	SEG_{42}	28	SEG_1	42	SEG_{15}	56	SEG_{28}

ELECTRICAL CHARACTERISTICS

• Absolute Maximum Ratings

Parameter	Symbol	Condition	Rating	Unit
Supply Voltage	V_{DD}	T_a = 25°C	-0.3 to +6.5	V
Input Voltage	V_I	T_a = 25°C	GND-0.3 to V_{DD} +0.3	V
Storage Temperature	T_{stg}	———	-55 to +150	°C

Note: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

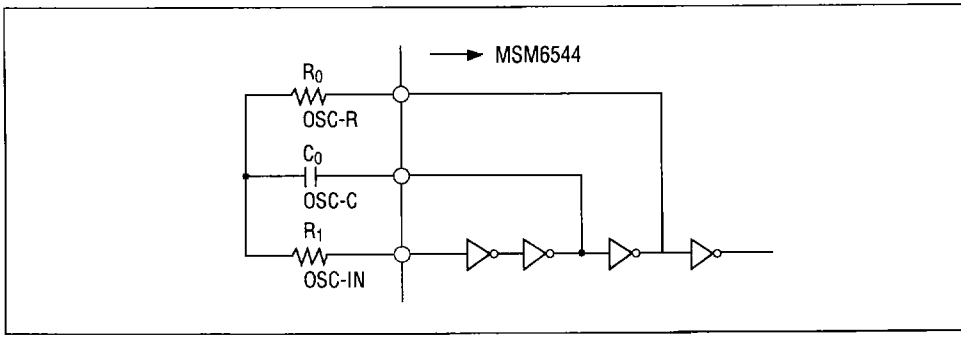
• Operating Range

Parameter	Symbol	Condition	Rating	Unit
Supply Voltage	V_{DD}	———	3 to 6	V
Operating Temperature	T_{OP}	———	-40 to +85	°C
LCD Driving Circuit	V_{DD} - V_{LCL}	———	3 to V_{DD}	V

• Recommendable Operating Conditions (OSC Circuit)

Parameter	Symbol	Corresponding Pin	Condition	Min.	Typ.	Max.	Unit
Resistor for Oscillation	R_0	OSC-R		10	–	68	kΩ
Capacitor for Oscillation	C_0	OSC-C	Film condenser	0.001	–	0.047	μF
Resistor for Current Restriction	R_1	OSC-IN	———	33	–	220	kΩ
Common Signal Frequency	f_{COM}	COM-A COM-B	———	25	–	250	Hz

• External Component Hookup for RC Oscillator



• DC Characteristics

(V_{DD} = 5.0V Ta = -40 to +85°C)

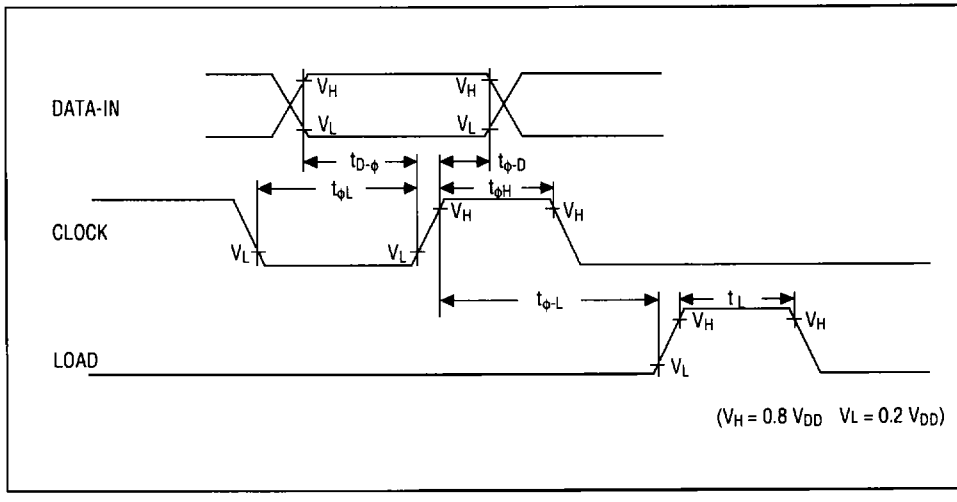
Parameter	Symbol	Corresponding Pin	Condition	Min.	Typ.	Max.	Unit
High Input Voltage	V_{IH}	BLANK LOAD DATA CLOCK	———	3.6	–	–	V
Low Input Voltage	V_{IL}		———	–	–	1.0	V
Input Leakage Current	I_{LI}	OSC-IN	V_I = 5.0V/0V	–	–	±1	µA
High Output Voltage	V_{OH}	OSC-R OSC-C	I_O = -200µA	4.5	–	–	V
		All segment outputs	V_{LCM} = 2.5V V_{LCL} = 0V I_O= -30µA	4.8	–	–	V
		COM-A COM-B	V_{LCM} = 2.5V V_{LCL} = 0V I_O= -150µA	4.8	–	–	V
"M" Output Voltage	V_{OM}	COM-A COM-B	V_{LCM} = 2.5V V_{LCL} = 0V I_O= ±150µA	2.3	–	2.7	V
Low Output Voltage	V_{OL}	OSC-R OSC-C	I_O = -200µA	–	–	0.5	V
		All segment outputs	V_{LCM} = 2.5V V_{LCL} = 0V I_O= 30µA	–	–	0.2	V
		COM-A COM-B	V_{LCM} = 2.5V V_{LCL} = 0V I_O= 150µA	–	–	0.2	V
Segment Output Impedance	R_{SEG}	All segment outputs	V_{LCM} = (5+V_{LCL})/2 V_{LCL} = 0 to 2V	–	–	10	kΩ
Common Output Impedance	R_{COM}	COM-A COM-B	V_{LCM} = (5+V_{LCL})/2 V_{LCL} = 0 to 2V	–	–	1.5	kΩ
Static Consumption Current	I_{DD1}	V_{DD}	Fix all inputs to "H"or "L"	–	–	100	µA
Dynamic Consumption Current	I_{DD2}		At no load, oscillation R_o = 47kΩ C_o = 0.0047µF R_1 =150kΩ	–	0.22	0.5	mA

• Switching Characteristics

(V_{DD} = 3.0 to 6.0V, Ta = -40 to +85°C)

Parameter	Symbol	Corresponding Pin	Condition	Min.	Max.	Unit
Maximum Clock Pulse Frepuency	$f_{\phi MAX}$	CLOCK	–	4	–	MHz
Clock Pulse Width, High	$t_{\phi H}$		–	100	–	nS
Clock Pulse Width, Low	$t_{\phi L}$		–	100	–	nS
Data Set-up Time	$t_{D-\phi}$	DATA	–	80	–	nS
Data Holding Time	$t_{\phi-D}$	CLOCK	–	40	–	nS
Load Pulse Width	t_L	LOAD	–	100	–	nS
Clock-load Timing	$t_{\phi-L}$	CLOCK LOAD	–	100	–	nS
OSC-IN Maximum Input Frequency	$f_{OSC\ MAX}$	OSC-IN	–	20	–	kHz

INPUT TIMING DIAGRAM



PIN DESCRIPTION

- **OSC-IN, OSC-C, OSC-R**
  The RC oscillator circuit for 3-terminal type can be fabricated. In this case, since the OSC-IN terminal operates at the high impedance state, it is susceptible to noise.

- **DATA-IN**
  This is the display data input terminal, H equals segment on and L equals segment off.

- **CLOCK**
  Data is input on the rising edge of this clock.

- **LOAD**
  This is the signal for latching the shift register data. When this pin is set at a high level, the shift register data is transmitted to LATCH <A> or LATCH <B>.

- **SEG1 ~ SEG42**
  These pins drive the LCD segments.

- **COM-A, COM-B**
  These pins drive the LCD common.

- **V_{DD2}**
  This is connected to the V_{DD1} terminal internally.

- **V_{LCM}**
  This is the center bias terminal of the LCD, apply the middle voltage of V_{DD} and V_{LCL}.

- **V_{LCL}**
  This is the power supply terminal of LCD driver. The contrast of the LCD can be adjusted by changing this terminal voltage, but do not set this terminal to the voltage to less than the Ground level.

DATA INPUT DESCRIPTION

The data input consists of 3-timing units as follows.

i) SEG-DATA unit (42-bit)
ii) SEL bit unit (1-bit)
iii) LOAD unit

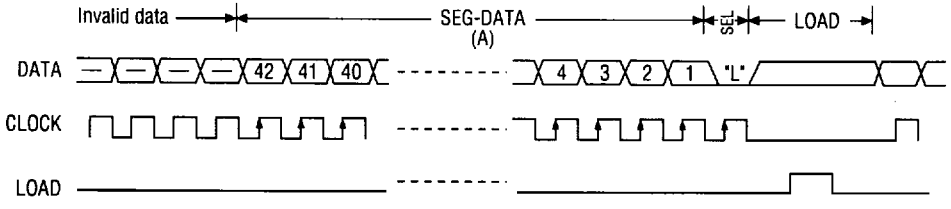
A total 43 bits of 42-bit segment data and 1-bit select bit are taken in the 43-bit shift register at the rising edge of the clock.
The segment data corresponds to "L" segment off and "H" segment on. Input the segment data from SEG42 to SEG1 in order.
The select bit following the segment data is a bit to specify the transmitting end of the segment data. The selection is performed as follows.

"L" : LATCH <A> Corresponding to COM-A
"H" : LATCH <B> Corresponding to COM-B

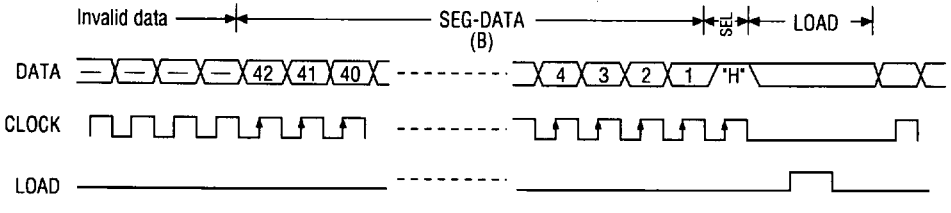
The data from the shift register to LATCH <A> or LATCH <B> is transmitted by "H" level of LOAD signal.
The indication corresponding to the latch for the transmitting end is also changed at the same time with the transmission.

DATA INPUT TIMING

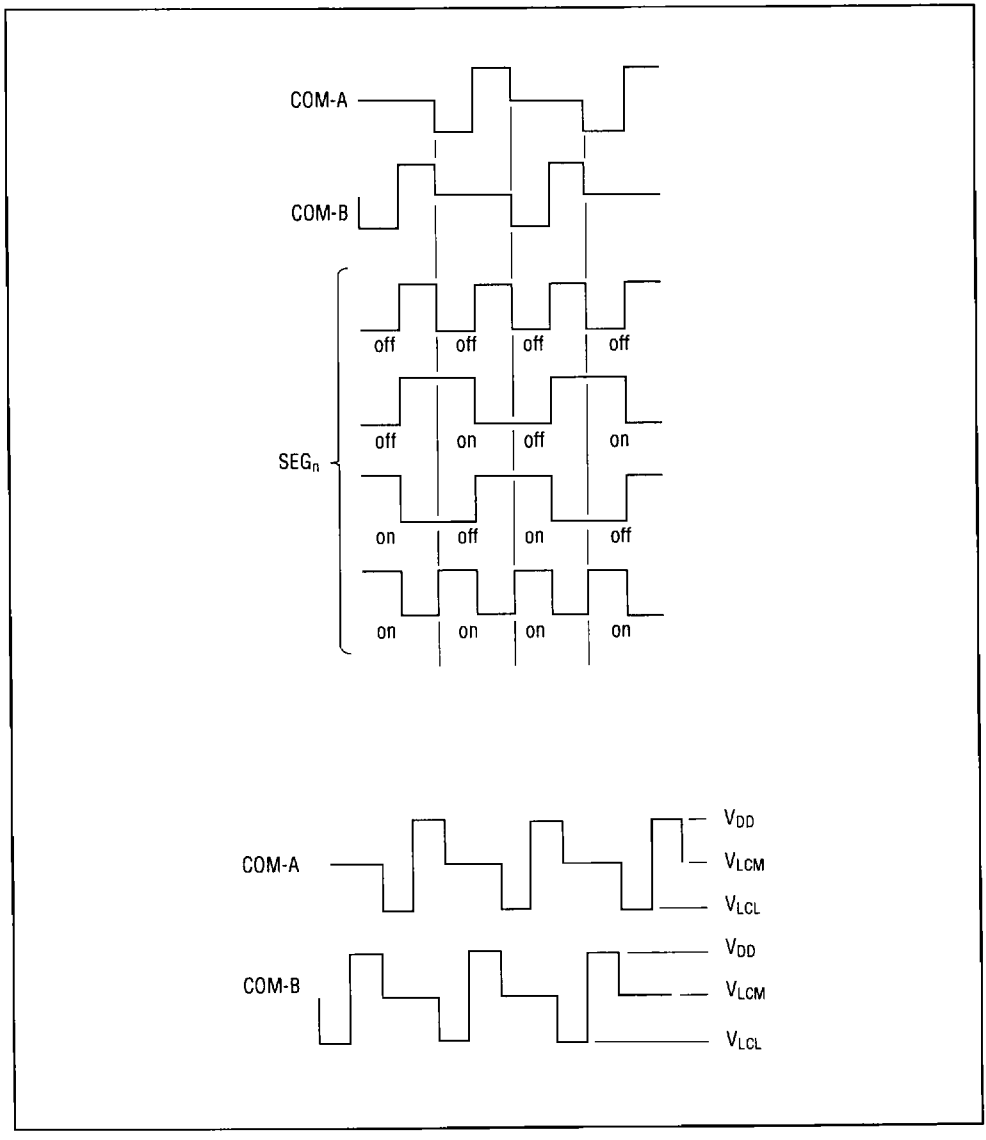
DATA Input Timing for COM-A



DATA Input Timing for COM-B



OUTPUT WAVEFORM



APPLICATION CIRCUIT