NB3N51034

3.3V, Crystal to 100MHz/ 200MHz Quad HCSL/LVDS Clock Generator

The NB3N51034 is a high precision, low phase noise clock generator that supports spread spectrum designed for PCI Express applications. This device takes a 25 MHz fundamental mode parallel resonant crystal and generates 4 differential HCSL/LVDS outputs at 100 MHz or 200 MHz (See Figure 6 for LVDS interface). The NB3N51034 provides selectable spread options of −0.5%, −1.0%, −1.5%, for applications demanding low Electromagnetic Interference (EMI). No spread setting is also available.

Features

- Uses 25 MHz Fundamental Mode Parallel Resonant Crystal
- Power Down Mode
- 4 Low Skew HCSL or LVDS Outputs
- OE Tri−States Outputs
- Spread of −0.5%, −1.0%, −1.5% and No Spread
- PCIe Gen 1, 2, 3 Jitter Compliant
- Phase Noise (SS OFF) @ 100 MHz:

Offset	Noise Power
100 Hz	−110 dBc/Hz
1 kHz	−123 dBc/Hz
10 kHz	−134 dBc/Hz
100 kHz	−137 dBc/Hz
1 MHz	−138 dBc/Hz
10 MHz	−154 dBc/Hz

- Operating Range 3.3 V ±5%
- Industrial Temperature Range −40°C to +85°C
- Functionally Compatible with IDT557−05, IDT5V41066, IDT5V41236
- These are Pb−Free Devices

Applications

- Networking
- Consumer
- Computing and Peripherals
- Industrial Equipment
- PCIe Clock Generation Gen I, Gen II and Gen III

End Products

- Switch and Router
- Set Top Box, LCD TV
- Servers, Desktop Computers
- Automated Test Equipment

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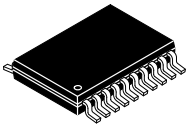
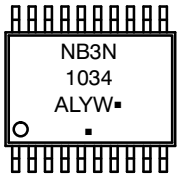


TSSOP−20
DT SUFFIX
CASE 948E

MARKING DIAGRAM



A	= Assembly Location
L	= Wafer Lot
Y	= Year
W	= Work Week
▪	= Pb−Free Package

(Note: Microdot may be in either location)

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 8 of this data sheet.

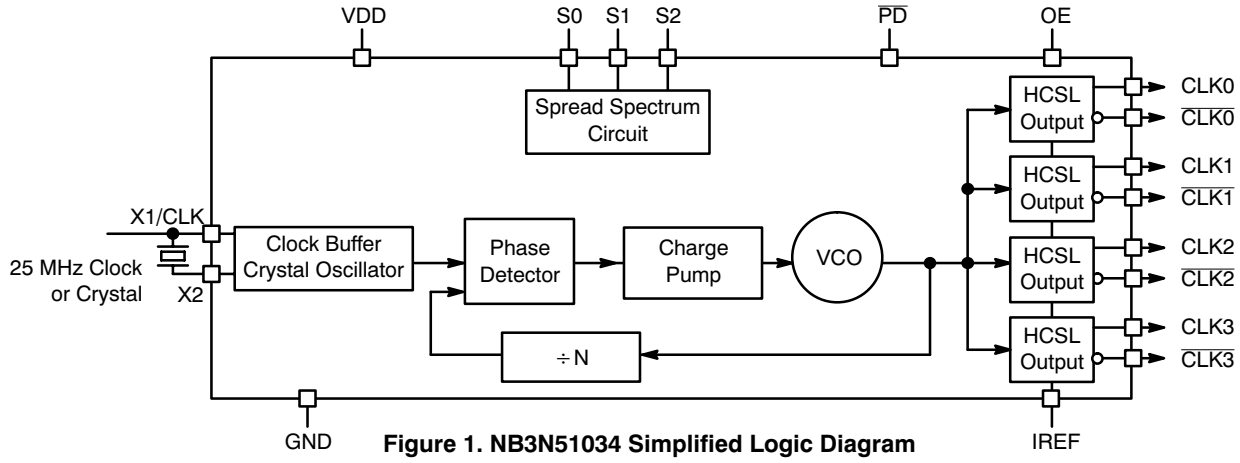


Figure 1. NB3N51034 Simplified Logic Diagram

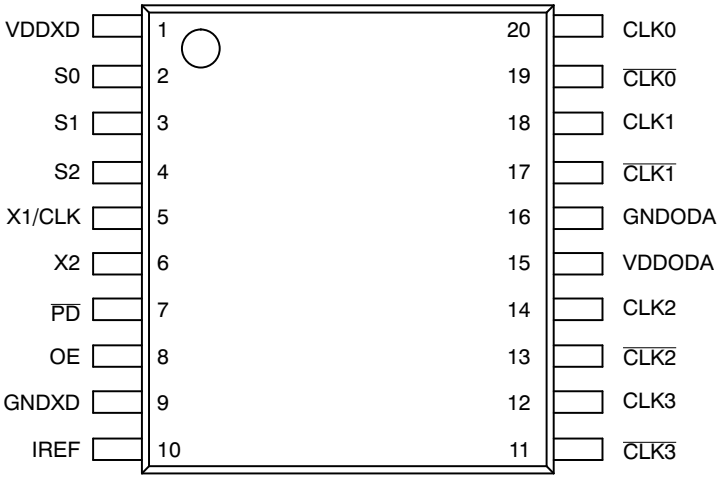


Figure 2. Pin Configuration (Top View)

Table 1. PIN DESCRIPTION

Pin	Symbol	I/O	Description
1	VDDXD	Power	Connect to a +3.3 V source.
2	S0	Input	Spread Spectrum Select pin 0. See Spread Spectrum Select table. Internal pull−up resistor.
3	S1	Input	Spread Spectrum Select pin 1. See Spread Spectrum Select table. Internal pull−up resistor.
4	S2	Input	Spread Spectrum Select pin 2. See Spread Spectrum Select table. Internal pull−up resistor.
5	X1/CLK	Input	Crystal interface or single−ended reference clock input.
6	X2	Output	Crystal interface. Float this pin for reference clock input CLK.
7	$\overline{PD}$	Input	Power down. Internal pull−up resistor.
8	OE	Input	Output enable. Tri−state output (High=enable outputs, Low=disable outputs). Internal pull−up resistor.
9	GNDXD	Power	Connect to digital circuit ground.
10	I_{REF}	Output	Precision resistor attached to this pin is connected to the internal current reference.
11	$\overline{CLK3}$	Output	Selectable 100/200 MHz Spread Spectrum differential compliment output clock 3.
12	CLK3	Output	Selectable 100/200 MHz Spread Spectrum differential true output clock 3.
13	$\overline{CLK2}$	Output	Selectable 100/200 MHz Spread Spectrum differential compliment output clock 2.
14	CLK2	Output	Selectable 100/200 MHz Spread Spectrum differential true output clock 2.
15	VDDODA	Power	Connect to a +3.3 V analog source.
16	GNDODA	Power	Output and analog circuit ground.
17	$\overline{CLK1}$	Output	Selectable 100/200 MHz Spread Spectrum differential compliment output clock 1.
18	CLK1	Output	Selectable 100/200 MHz Spread Spectrum differential true output clock 1.
19	$\overline{CLK0}$	Output	Selectable 100/200 MHz Spread Spectrum differential compliment output clock 0.
20	CLK0	Output	Selectable 100/200 MHz Spread Spectrum differential true output clock 0.

Table 2. OUTPUT FREQUENCY AND SPREAD SPECTRUM SELECT TABLE

S2	S1	S0	Spread%	Spread Type	Output Frequency
0	0	0	−0.5	Down	100
0	0	1	−1.0	Down	100
0	1	0	−1.5	Down	100
0	1	1	No Spread	N/A	100
1	0	0	−0.5	Down	200
1	0	1	−1.0	Down	200
1	1	0	−1.5	Down	200
1	1	1	No Spread	N/A	200

Recommended Crystal Parameters

Crystal	Fundamental AT−Cut
Frequency	25 MHz
Load Capacitance	16−20 pF
Shunt Capacitance, C0	7 pF Max
Equivalent Series Resistance	50 Ω Max
Initial Accuracy at 25 °C	±20 ppm
Temperature Stability	±30 ppm
Aging	±20 ppm

Table 3. ATTRIBUTES

Characteristic		Value
Internal Input Default State Resistor (OE, Sx, $\overline{PD}$)		110 kΩ
ESD Protection	Human Body Model	2 kV
Moisture Sensitivity, Indefinite Time Out of Dray Pack (Note 1)		Level 1
Flammability Rating	Oxygen Index: 28 to 34	UL 94 V−0 @ 0.125 in
Transistor Count		132,000
Meets or exceeds JEDEC Spec EIA/JESD78 IC Latchup Test		

1. For additional information, see Application Note AND8003/D.

Table 4. MAXIMUM RATINGS (Note 2)

Symbol	Parameter	Condition 1	Condition 2	Rating	Units
V_{DD}	Positive Power Supply	GND = 0 V		4.6	V
V_I	Input Voltage (V_{IN})	GND = 0 V	GND ≤ V_I ≤ V_{DD}	−0.5 V to V_{DD}+0.5 V	V
T_A	Operating Temperature Range			−40 to +85	°C
T_{stg}	Storage Temperature Range			−65 to +150	°C
θ_{JA}	Thermal Resistance (Junction−to−Ambient)	0 lfpm 500 lfpm	TSSOP−20 TSSOP−20	140 50	°C/W °C/W
θ_{JC}	Thermal Resistance (Junction−to−Case)	(Note 3)	TSSOP−20	23 to 41	°C/W
T_{sol}	Wave Solder			265	°C

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

2. Maximum ratings applied to the device are individual stress limit values (not normal operating conditions) and not valid simultaneously. If stress limits are exceeded device functional operation is not implied, damage may occur and reliability may be affected.
3. JEDEC standard multilayer board − 2S2P (2 signal, 2 power).

Table 5. DC CHARACTERISTICS (V_{DD} = 3.3 V ±5%, GND = 0 V, T_A = −40°C to +85°C, Note 4)

Symbol	Characteristic	Min	Typ	Max	Unit
VDD	Power Supply Voltage	3.135	3.3	3.465	V
I_{DD}	Power Supply Current, 200 Mhz output, SSON		135		mA
I_{DDOE}	Power Supply Current when OE is Set Low		60		mA
I_{DDPD}	Power Supply Current ($\overline{PD}$ = Low, no load)		1.5		mA
V_{IH}	Input HIGH Voltage (X1/CLK, S0, S1, S2 and OE)	2000		V_{DD} + 300	mV
V_{IL}	Input LOW Voltage (X1/CLK, S0, S1, S2 and OE)	GND − 300		800	mV

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfpm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

4. Measurement taken with outputs terminated with R_S = 33.2 Ω, R_L = 50 Ω, with test load capacitance of 2 pF and current biasing resistor set at 475 Ω. See Figure 5. Guaranteed by characterization.

Table 6. AC CHARACTERISTICS (V_{DD} = 3.3 V ±5%, GND = 0 V, T_A = −40°C to +85°C; Note 5)

Symbol	Characteristic	Min	Typ	Max	Unit
f_{CLKIN}	Clock/Crystal Input Frequency		25		MHz
f_{CLKOUT}	Output Clock Frequency		100/200		MHz
Vmax	Absolute Maximum Output Voltage (Notes 6, 7)			1150	mV
Vmin	Absolute Minimum Output Voltage (Notes 6, 8)	−300			mV
Vrb	Ringback Voltage (Notes 9, 10)	−100		100	mV
VOH	Output High Voltage (Note 6)	660		850	mV
VOL	Output Low Voltage (Note 6)	−150		27	mV
V_{CROSS}	Absolute Crossing Voltage (Notes 6, 10, 11)	250		550	mV
ΔV_{CROSS}	Total Variation of V_{CROSS} (Notes 6, 10, 12)			140	mV
f_{MOD}	Spread Spectrum Modulation Frequency	30	31.5	33.33	kHz
SSC_{RED}	Spectral Reduction (Note 13), 3rd harmonic		−10		dB
t_{SKEW}	Within Device Output to Output Skew			40	ps
ϕ_{NOISE}	Phase−Noise Performance SS OFF f_{CLKout} = 100 MHz				dBc/Hz
	@ 100 Hz offset from carrier		−110		
	@ 1 kHz offset from carrier		−123		
	@ 10 kHz offset from carrier		−134		
	@ 100 kHz offset from carrier		−137		
	@ 1 MHz offset from carrier		−138		
	@ 10 MHz offset from carrier		−154		
t_{OE}	Output Enable/Disable Time (All outputs) (Note 14)			10	μs
t_{DUTY_CYCLE}	Output Clock Duty Cycle (Measured at cross point)	45	50	55	%
t_R	Output Risetime (Measured from 175 mV to 525 mV, Figure 7)	175	340	700	ps
t_F	Output Falltime (Measured from 525 mV to 175 mV, Figure 7)	175	400	700	ps
Δt_R	Output Risetime Variation (Single−Ended)			125	ps
Δt_F	Output Falltime Variation (Single−Ended)			125	ps
Stabilization Time	Stabilization Time From Powerup V_{DD} = 3.3 V		3.0		ms

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfpm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

5. Measurement taken from differential output on single−ended channel terminated with R_S = 33.2 Ω, R_L = 50 Ω, with test load capacitance of 2 pF and current biasing resistor set at 475 Ω. See Figure 5. Guaranteed by characterization.
6. Measurement taken from single-ended waveform
7. Defined as the maximum instantaneous voltage value including positive overshoot
8. Defined as the maximum instantaneous voltage value including negative overshoot
9. Measurement taken from differential waveform
10. Measured at crossing point where the instantaneous voltage value of the rising edge of CLKx+ equals the falling edge of CLKx-.
11. Refers to the total variation from the lowest crossing point to the highest, regardless of which edge is crossing. Refers to all crossing points for this measurement.
12. Defined as the total variation of all crossing voltage of rising CLKx+ and falling CLKx-. This is maximum allowed variance in the VCROSS for any particular system.
13. Spread spectrum clocking enabled.
14. Output pins are tri−stated when OE is asserted LOW. Output pins are driven differentially when OE is HIGH unless device is in power down mode, $\overline{PD}$ = Low.

Table 7. AC ELECTRICAL CHARACTERISTICS – PCI EXPRESS JITTER SPECIFICATIONS,
V_{DD} = 3.3 V ± 5%, T_A = −40°C to 85°C

Symbol	Parameter	Test Conditions		Min	Typ	Max	PCIe Industry Spec	Unit
tj (PCIe Gen 1)	Phase Jitter Peak−to−Peak (Notes 16 and 19)	f = 100 MHz, 25 MHz Crystal Input Evaluation Band: 0 Hz – Nyquist (clock frequency/2)	SSOFF		10	20	86	ps
			SSON (−0.5%)		19	28		
tREFCLK_HF_RMS (PCIe Gen 2)	Phase Jitter RMS (Notes 17 and 19)	f = 100 MHz, 25 MHz Crystal Input High Band: 1.5 MHz – Nyquist (clock frequency/2)	SSOFF		1.0	1.8	3.1	ps
			SSON (−0.5%)		1.1	1.9		
tREFCLK_LF_RMS (PCIe Gen 2)	Phase Jitter RMS (Notes 17 and 19)	f = 100 MHz, 25 MHz Crystal Input Low Band: 10 kHz – 1.5 MHz	SSOFF		0.1	0.15	3.0	ps
			SSON (−0.5%)		0.8	1.1		
tREFCLK_RMS (PCIe Gen 3)	Phase Jitter RMS (Notes 18 and 19)	f = 100 MHz, 25 MHz Crystal Input Evaluation Band: 0 Hz – Nyquist (clock frequency/2)	SSOFF		0.35	0.7	1.0	ps
			SSON (−0.5%)		0.55	0.8		

15. Electrical parameters are guaranteed over the specified ambient operating temperature range, which is established when the device is mounted in a test socket with maintained transverse airflow greater than 500 lfpm. The device will meet specifications after thermal equilibrium has been reached under these conditions.
16. Peak−to−Peak jitter after applying system transfer function for the Common Clock Architecture. Maximum limit for PCI Express Gen 1 is 86 ps peak−to−peak for a sample size of 10^6 clock periods.
17. RMS jitter after applying the two evaluation bands to the two transfer functions defined in the Common Clock Architecture and reporting the worst case results for each evaluation band. Maximum limit for PCI Express Generation 2 is 3.1 ps RMS for tREFCLK_HF_RMS (High Band) and 3.0ps RMS for tREFCLK_LF_RMS (Low Band).
18. RMS jitter after applying system transfer function for the common clock architecture.
19. Measurement taken from differential output on single−ended channel terminated with R_S = 33.2 Ω, R_L = 50 Ω, with test load capacitance of 2 pF and current biasing resistor set at 475 Ω. See Figure 5. This parameter is guaranteed by characterization. Not tested in production.

PHASE NOISE

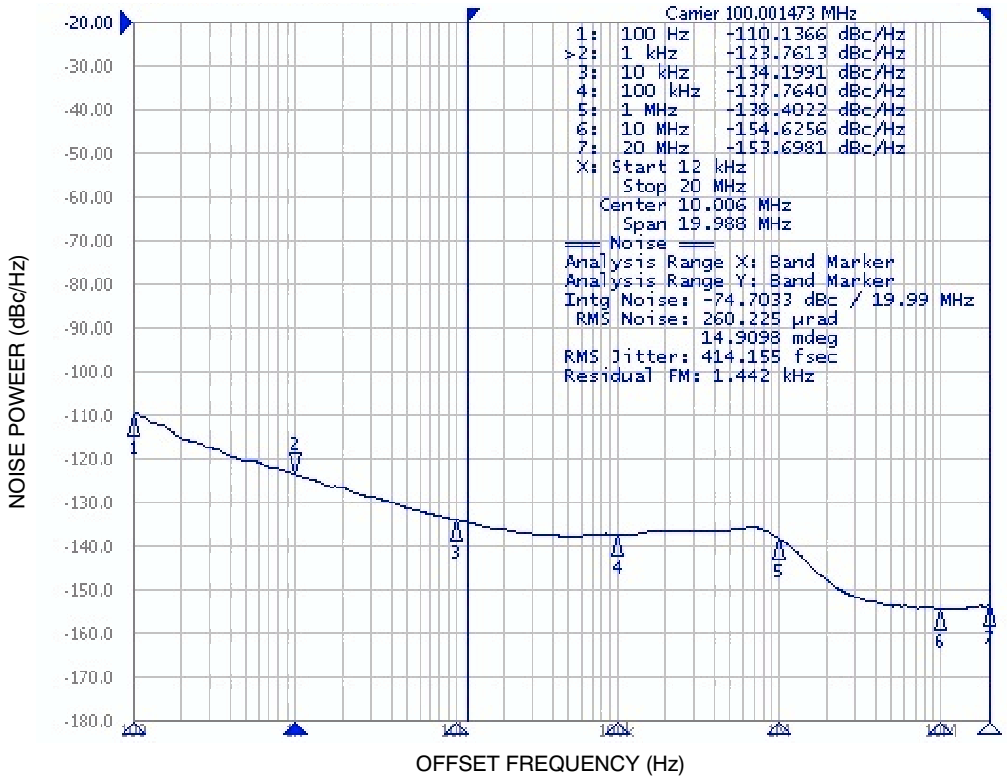


Figure 3. Typical Phase Noise at 100 MHz; integration range 12 kHz to 20 MHz (Input source at 25 MHz and HCSL output termination)

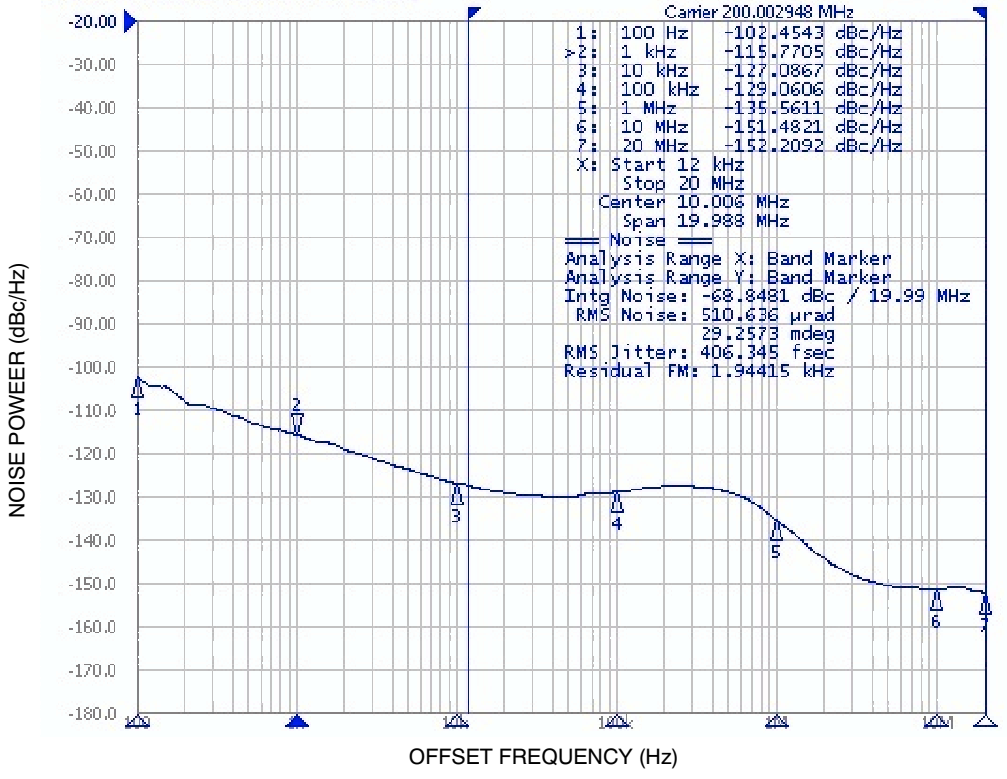


Figure 4. Typical Phase Noise at 200 MHz; integration range 12 kHz to 20 MHz (Input source at 25 MHz and HCSL output termination)

HCSL INTERFACE

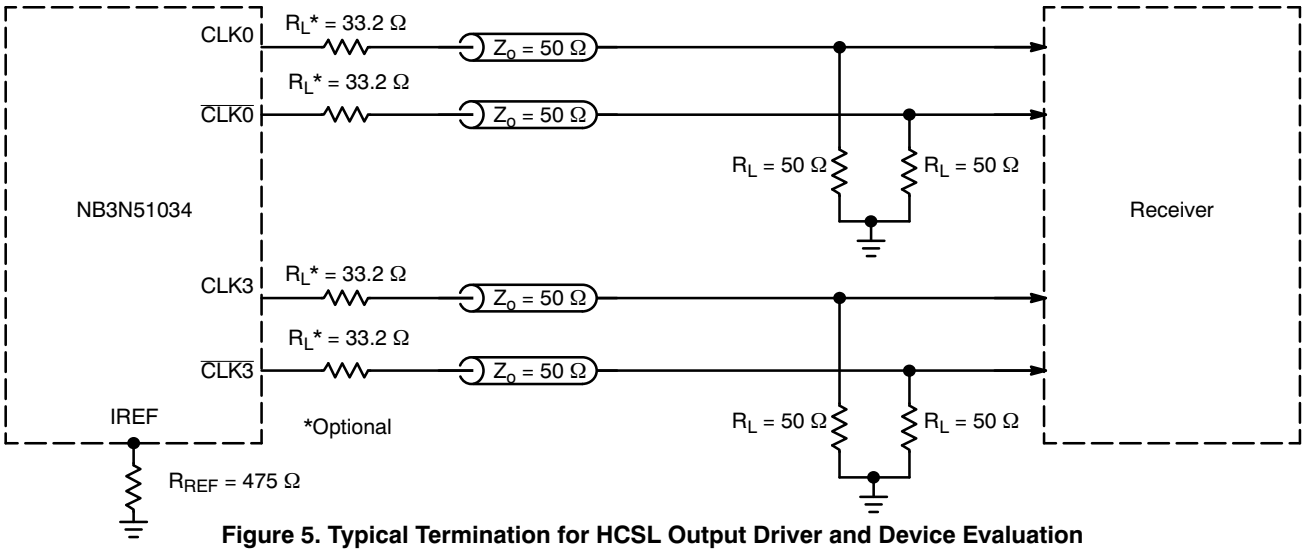


Figure 5. Typical Termination for HCSL Output Driver and Device Evaluation

LVDS COMPATIBLE INTERFACE

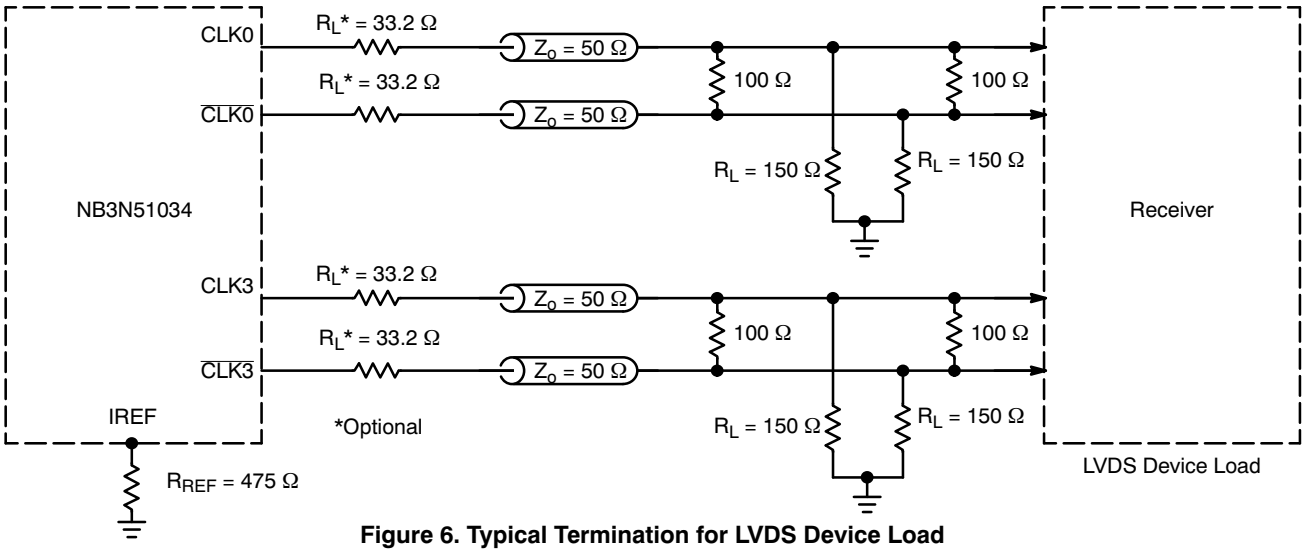


Figure 6. Typical Termination for LVDS Device Load

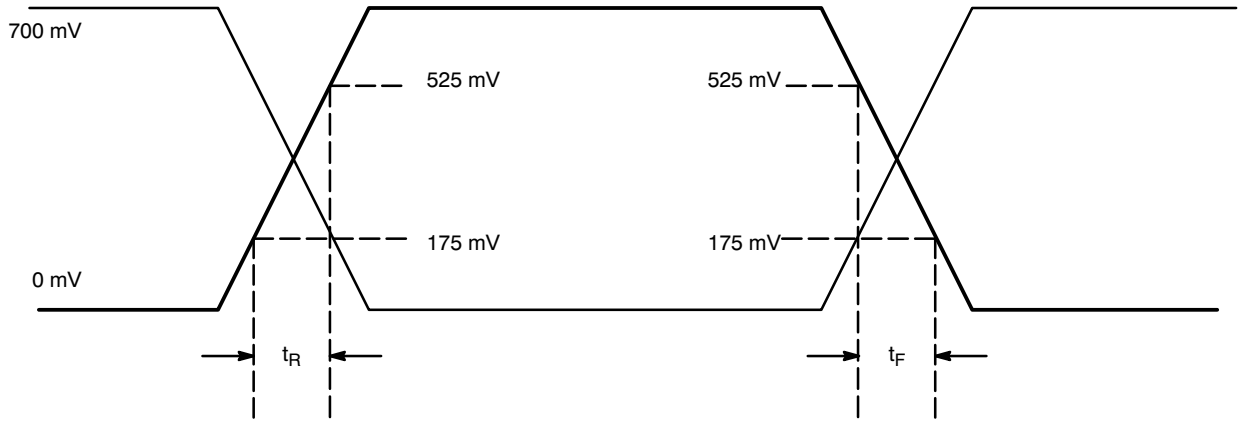


Figure 7. HCSL Output Parameter Characteristics

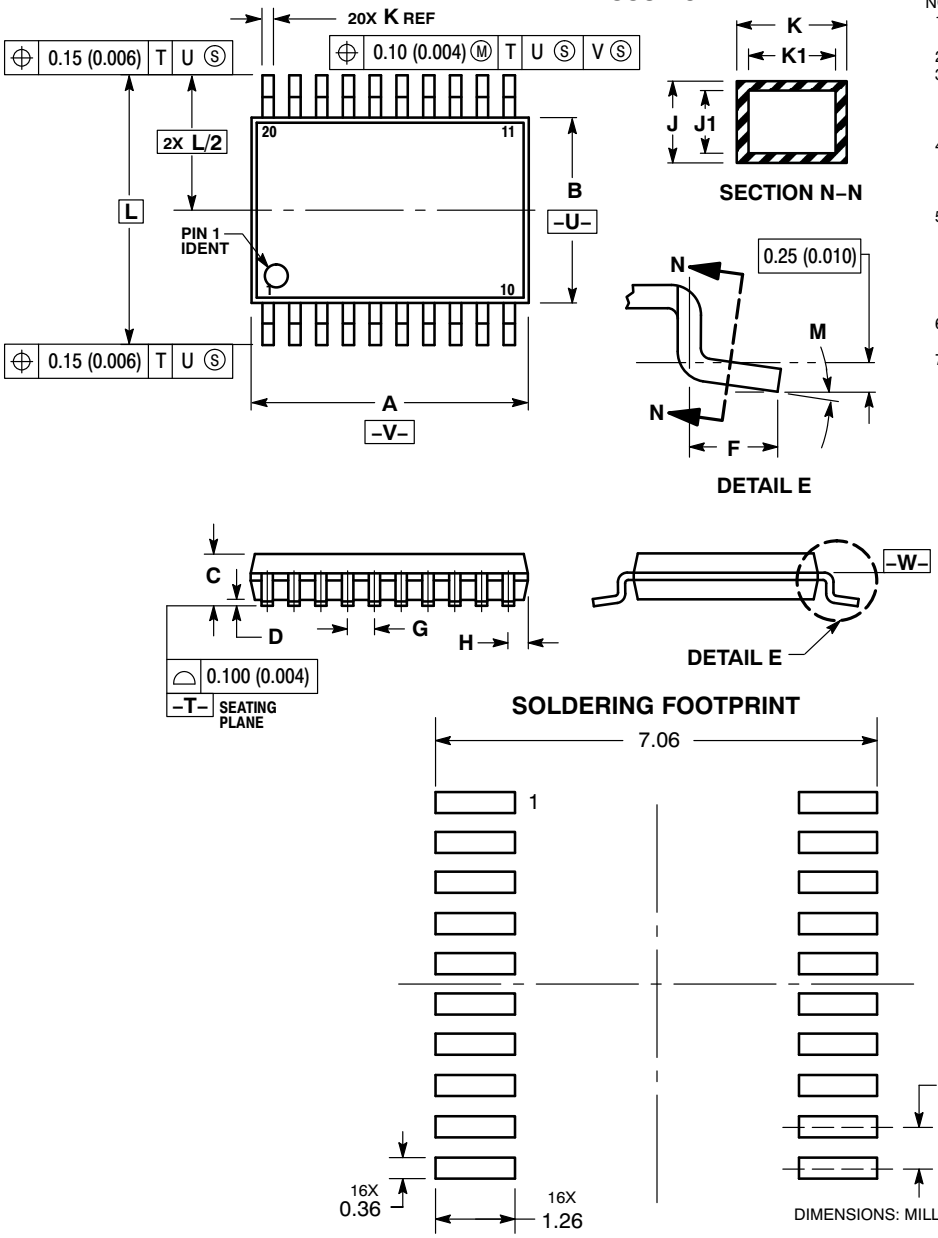
ORDERING INFORMATION

Device	Package	Shipping†
NB3N51034DTG	TSSOP−20 (Pb−Free)	75 Units / Rail
NB3N51034DTR2G	TSSOP−20 (Pb−Free)	2500 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

PACKAGE DIMENSIONS

TSSOP−20
CASE 948E−02
ISSUE C



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
7. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE −W−.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	6.40	6.60	0.252	0.260
B	4.30	4.50	0.169	0.177
C	---	1.20	---	0.047
D	0.05	0.15	0.002	0.006
F	0.50	0.75	0.020	0.030
G	0.65 BSC		0.026 BSC	
H	0.27	0.37	0.011	0.015
J	0.09	0.20	0.004	0.008
J1	0.09	0.16	0.004	0.006
K	0.19	0.30	0.007	0.012
K1	0.19	0.25	0.007	0.010
L	6.40 BSC		0.252 BSC	
M	0°	8°	0°	8°

SOLDERING FOOTPRINT

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