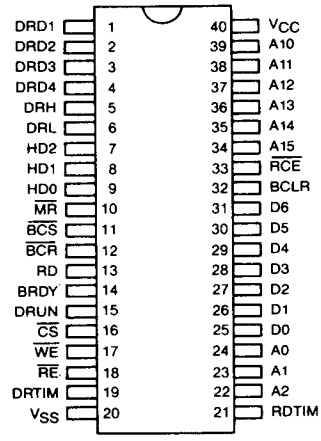
# WD1100-21 Buffer Manager Support Device

**FEATURES**

- 6-BIT AUTO-INCREMENTING ADDRESS BUS
- 128, 256, 512, OR 1024 BYTES PER SECTOR DETECTOR
- SELECTS UP TO 4 DISK DRIVES
- SELECTS UP TO 8 HEADS PER DRIVE
- PROVIDES A RAM CHIP ENABLE AND READY SIGNAL
- TTL, MOS COMPATIBLE
- 40 PIN DIP PACKAGE
- NMOS TECHNOLOGY
- SINGLE + 5 VDC SUPPLY

**DESCRIPTION**

The WD1100-21 Buffer Manager Support Device is designed to interface up to four disk drives and eight heads per drive, to a WD1010-05 and Sector Buffer. The WD1100-21 accepts the SDH Register information (Sector Size, Drive, Head) and selects the appropriate drive and head. It receives the data from the disk and develops RD and DRUN (Read Data and Data Run) suitable for the WD1010-05. The WD1100-21 also selects the Sector Buffer and provides six of the address lines. The other four address lines must be implemented externally. The WD1100-21 signals BRDY (Buffer Ready) when the buffer counter reaches the value stored in the SDH Register.




**PIN DESIGNATION**

**PIN DESCRIPTION**

| PIN NUMBER | MNEMONIC | PIN NAME | I/O | FUNCTION |
|---|---|---|---|---|
| 1 | DRD1 | READ DATA 1 | I | This signal is data read from disk drive 1. It is shaped and placed on output pin 13. |
| 2 | DRD2 | READ DATA 2 | I | This signal is data read from disk drive 2. It is shaped and placed on output pin 13. |
| 3 | DRD3 | READ DATA 3 | I | This signal is data read from disk drive 3. It is shaped and placed on output pin 13. |
| 4 | DRD4 | READ DATA 4 | I | This signal is data read from disk drive 4. It is shaped and placed on output pin 13. |
| 5 | DRH | DRIVE SELECT HIGH | I | Most significant bit of the drive select number. Must be encoded externally. |
| 6 | DRL | DRIVE SELECT LOW | I | Least significant bit of drive select number. Must be encoded externally. |
| 7 | HD2 | HEAD SELECT 2 | I | Bit 2 of the head select number. Must be encoded externally. |
| 8 | HD1 | HEAD SELECT 1 | I | Bit 1 of the head select number. Must be encoded externally. |
| 9 | HD0 | HEAD SELECT 0 | I | Bit 0 of the head select number. Must be encoded externally. |
| 10 | $\overline{MR}$ | MASTER RESET | I | Asserted, it initializes all internal logic including the SDH Register. |
| 11 | $\overline{BCS}$ | BUFFER CHIP SELECT | I | Asserted, this signal asserts RCE. |
| 12 | $\overline{BCR}$ | BUFFER COUNTER RESET | I | This signal resets the buffer address counter to zero making A10 thru A15 = 0. |
| 13 | RD | READ DATA | 0 | This is the MFM data read from the disk, shaped and made compatible with the WD1010-05. |
| 14 | BRDY | BUFFER READY | 0 | This signal is asserted when the buffer counter (A10 thru A15) has reached the sector size specified in the SDH Register, 128, 256, 512, or 1024. |
| 15 | DRUN | DATA RUN | 0 | This signal is asserted when a field of ones or zeroes has been detected. |
| 16 | $\overline{CS}$ | CHIP SELECT | I | Must be asserted to write into the SDH Register, increment the Buffer Address Counter, and assert $\overline{RCE}$. |
| 17 | $\overline{WE}$ | READ ENABLE | I | Must be asserted to write into the SDH Register. $\overline{WE}$ or $\overline{RE}$ must be asserted to increment the Buffer Address Counter. |
| 18 | $\overline{RE}$ | READ ENABLE | I | $\overline{RE}$ or $\overline{WE}$ must be asserted to increment the Buffer Address Counter. |
| 19 | DRTIM | DRUN TIMING | I | An external load used to adjust DRUN to nominal pulse width of 250 nsec. |
| 20 | $V_{SS}$ | GROUND | I | Ground. |
| 21 | RDTIM | RD TIMING | I | An external load for adjusting the pulse width of RD. 1K ohms creates approx. 90 nsec. |
| 22 thru 24 | A2 thru A0 | ADDRESS 2 thru ADDRESS 0 | I | A2 thru A0 are used to address the SDH Register (A2-A0 = 6) and increment the Buffer Address Counter (A2-A0 = 0). |

**PIN DESCRIPTION (Continued)**

| PIN NUMBER | MNEMONIC | PIN NAME | I/O | FUNCTION |
|---|---|---|---|---|
| 25 thru 31 | DO thru D6 | DATA 0 thru DATA 6 | I | 7-Bit data bus used to write into the SDH Register. |
| 32 | BCLR | BUFFER CLEAR | O | Asserted, this signal indicates that the Buffer Address Counter has been cleared. |
| 33 | $\overline{RCE}$ | $\overline{RAM\ CHIP\ ENABLE}$ | O | Asserted by BCS, or CS and A0 thru A2 equal to zero. Used to enable access to the data buffer. |
| 34 thru 39 | A10 thru A15 | BUFFER ADDRESS 10 thru 15 | O | Buffer Address Counter. Used to address the Data Buffer. |
| 40 | $V_{CC}$ | POWER SOURCE | | +5V Power Supply |

**ARCHITECTURE**

The WD1100-21 is composed of a 7-Bit SDH Register (the extension bit, bit 7 is not included), 11-Bit Sector Buffer Counter, and miscellaneous control signals. The content of the SDH Register is used to select the drive and head, and limit the Sector Buffer Counter to the size decoded by bits 5 and 6.

Figure 1 is a block diagram illustrating the relationship of the timing and control signals with the SDH Register and Sector Buffer Counter.

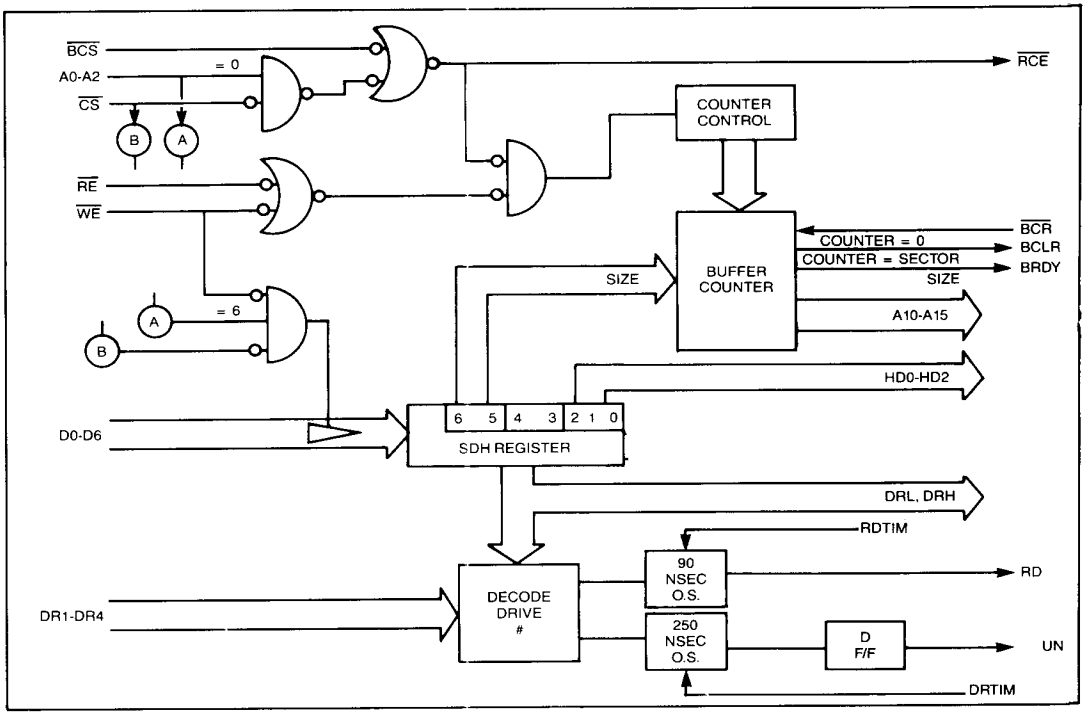



**FIGURE 1. WD1100-21 BLOCK DIAGRAM**

## OPERATIONAL DESCRIPTION

The Host, to write to the SDH Register asserts $\overline{CS}$ and $\overline{WE}$, and places an address of zero on A0 thru A2.

| 6 5 | 4 3 | 2 1 0 |
|---|---|---|
| SIZE | DRIVE | HEAD |

SDH bits 2-1-0 make up signals HD2 HD1 and HD0 and are encoded externally to select one of eight heads. SDH bits 4 and 3 make up signals DRH and DRL, and they are encoded externally to select one of four drives. Bits 4 and 3 are also used internally to enable the appropriate input signal DRD1 thru DRD4 from the drive reading data. Bits 6 and 5 are encoded as follows and asserts BRDY (Buffer Ready) when the Sector Buffer Counter reaches the designated amount.

| SDH6 | SDH5 | SIZE |
|---|---|---|
| 0 | 0 | 256 |
| 0 | 1 | 512 |
| 1 | 0 | 1024 |
| 1 | 1 | 128 |

Sector Buffer Counter is an 11-bit binary counter used to address the Sector Buffer and generate the BCLR and BRDY signals. Only address bits A10 thru A15 are supplied by the counter, the other five bits must be implemented externally. BCR asserted by the WD1010-05 resets the counter to zero. The counter in turn, asserts BCLR which is used to reset the five remaining address bits. The Sector Buffer may be written into and Read from by the Host and Disk.

The Host, to access the Sector Buffer, must place an address of zero on A0 thru A2, assert CS to select the WD1100-21, WE to write, or RE to read. This is done for each byte written to, or read from the Sector Buffer. In turn the WD1100-21 asserts $\overline{RCE}$ enabling the Sector Buffer, and increments the Sector Buffer Counter by one. when the count specified by SDH6 and SDH5 is reached, BRDY is asserted indicating the end of the Sector Buffer.

Reading or writing to the Sector Buffer from the disk is done in much the same manner. The difference is, that the WD1010-05 supplies the $\overline{WE}$ and $\overline{RE}$ instead of the Host. The WD1010-05 also replaces the $\overline{CS}$ with $\overline{BCS}$.

The drive selected by DRL and DRH, inputs its Read Data on one of the DRD1 thru DRD4 lines. SDH4 and SDH3 enables the appropriate signal and passes it on to an O.S. to be shaped and widened for use by a WD1010-05. The DRUN signal is produced by gating the selected DRD signal to an O.S. followed by a D flip flop.

## ADJUSTMENTS

RD pulse width is established by the load placed on RDTIM. See Table 2 and Note 1.

DRUN is controlled by the resistance placed on DRTIM. Select DRD1 with the SDH Register. Then place a 5 MHz signal on DRD1 while monitoring DRUN on pin 15. It should be high. Then a 2.5 MHz signal is placed on the DRD1 input. DRUN should be low. The resistance chosen should be midway between DRUN just going high at 5 MHz. See Table 2 and Note 2.

## ELECTRICAL CHARACTERISTICS

## MAXIMUM RATINGS

Ambient Temperature under bias . . . . . 0°C (32°F) to 50°C (122°F).
Voltage on any pin with respect to $V_{SS}$ . . . . -0.2V to 7.0V
Power dissipation . . . . . 1.5 Watts

## STORAGE TEMPERATURE

Plastic . . . . . -55°C(-67°F) to 125°C (257°F)
Ceramic . . . . . -55°C(-67°F) to 150°C (302°F)

**NOTE:**

Maximum limits indicate where permanent device damage occurs. Continuous operation at these limits is not intended and should be limited to those conditions specified in the DC Electrical Characteristics.

### TABLE 1. DC OPERATING CHARACTERISTICS

$T_A$ = 0°C (32°F) to 70°C (158°F), $V_{CC}$ = +5V ± .25V, $V_{SS}$ = 0V

| SYMBOL | CHARACTERISTIC | MIN | TYP | MAX | UNIT | CONDITIONS |
|---|---|---|---|---|---|---|
| $I_{IL}$ | Input Leakage | | | -10 | A | Pins 1-4, 25-31 |
| $I_{OL}$ | Output Leakage | | | 10 | A | Pins 1-4, 25-31 |
| $I_{IP}$ | Input Pullup | 0.1 | | 1.6 | mA | Pins 10-12, 16-18, 22-24 |
| $V_{IH}$ | Voltage Input High | 2.0 | | | V | |
| $V_{IL}$ | Voltage Input Low | -0.2 | | 0.8 | V | |
| $V_{OH}$ | Voltage Output High | 2.4 | | | V | $I_{OH}$ = -100μA |
| $V_{OL}$ | Voltage Output Low | | | 0.4 | V | $I_{OL}$ = 1.6mA |
| $V_{CC}$ | Supply Voltage | 4.75 | 5.0 | 5.25 | V | |
| $I_{CC}$ | Supply Current | | 200 | 250 | mA | Outputs Open |

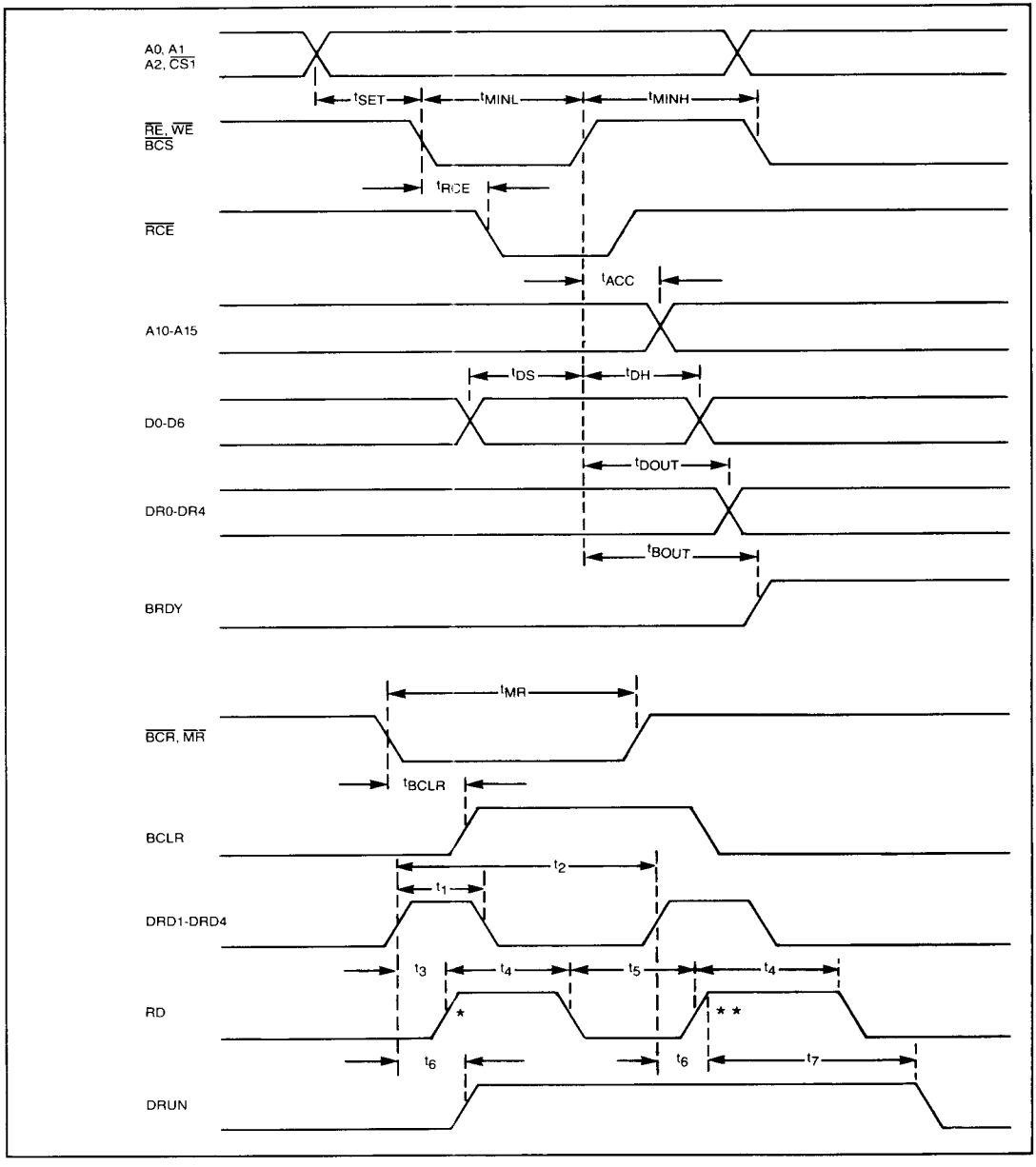


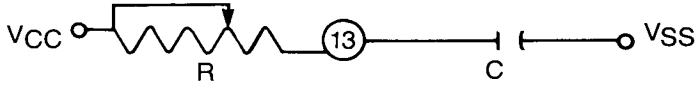

**FIGURE 2. AC TIMING**

*Trigger DRUN
**Retrigger DRUN

**TABLE 2. TIMING CHARACTERISTICS** **All units in nsec.**

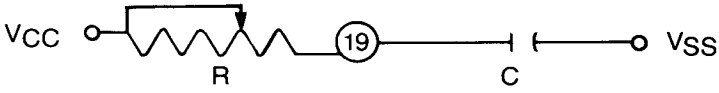
| SYMBOL | CHARACTERISTIC | MIN | TYP | MAX | CONDITIONS |
|---|---|---|---|---|---|
| $t_{SET}$ | A0 thru A2 and $\overline{CS}$ setup | 0 | | | |
| $t_{MINL}$ | $\overline{RE}$, $\overline{WE}$, and $\overline{BCS}$ low | 200 | | | |
| $t_{MINH}$ | $\overline{RE}$, $\overline{WE}$, and $\overline{BCS}$ high | 100 | | | |
| $t_{RCE}$ | $\overline{RCE}$ delay from $\overline{BCS}$ or $\overline{CS}$ | | | 100 | C = 50 pf |
| $t_{ACC}$ | A10 thru A15 delay from $\overline{RE}$ or $\overline{WE}$ | | | 200 | C = 50 pf |
| $t_{DS}$ | D0 thru D6 setup time | 50 | | | |
| $t_{DH}$ | D0 thru D6 hold time | 100 | | | |
| $t_{DOUT}$ | DR1 thru DR4 delay | | | 170 | C = 50 pf |
| $t_{BOUT}$ | $\overline{BRDY}$ delay | | | 250 | C = 50 pf |
| $t_{MR}$ | $\overline{MR}$ and $\overline{BCR}$ pulse width | 150 | | | |
| $t_{BCLR}$ | BCLR delay from $\overline{MR}$ or $\overline{BCR}$ | | | 200 | C = 50 pf |
| $t_1$ | DRD1 thru DRD 4 width | 25 | | | |
| $t_2$ | DRD1 thru DRD4 cycle time | | 200 | | |
| $t_3$ | RD delay from DRD1 thru DRD4 | | | 200 | C = 50 pf |
| $t_4$ | RD high | 90 | 100 | 110 | Note 1 |
| $t_5$ | RD low | | | | $t_2 - t_4$ |
| $t_6$ | DRUN delay from DRD1 thru DRD4 | | | 200 | Note 2 |
| $t_7$ | DRUN | 225 | 250 | 275 | |

**NOTE 1.**




TYP - R = 10 Kohms, C = 150 pf
Adjust R to meet characteristics for $t_4$. Typical values for $t_4$ and $t_5$ are for 5MHz data rate.

**NOTE 2.**




R = 10 Kohms, C = 150 pf
Adjust R to meet characteristics for $t_7$.