AN5033

TV Tuning Control Circuit

Outline

The AN5033 is an integrated circuit designed for tuner control circuit of TV electronic tuning system using a semiconductor memory.

Features

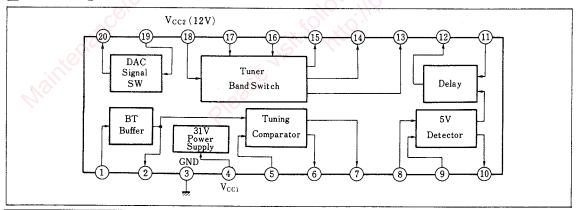
- Consists of peripheral part of electronic tuning system with semiconductor memories
- Reference voltage stabilizer for electronic tuning incorporated
- Power supply voltage rise up detection circuit incorporated

Unit: mm 10 □20 20 b19 18 **1**15 7 **-**13 8-9[**-**12 10□ 1.0 ± 0.25 -8.6±0.3- $4.7 \pm 0.25 \ \ 3.05 \pm 0.25$ $\sqrt[]{0.35^{+0.2}_{-0.05}}$ 20-Lead DIL Plastic Package

Pin

Pin No.	Pin Name	Pin No.	Pin Name
1	BT Voltage Input	11	CR Constant
2	BT Voltage Output	12	Reset Output
3	GND	13	BV Output
4	31V Regulator (V _{CC1})	14	BU Output
5	Pre-set Voltage Input	15	BS Output
6	Tuning Control Output	16	Band SW Input(1)
7	Switching Output	17	Band SW Input(2)
8	V _{CC3}	18	Vcc2
9	Ref. Voltage Input	19	DAC Signal Input
10	CE Det. Output	20	DAC Signal Output

Block Diagram



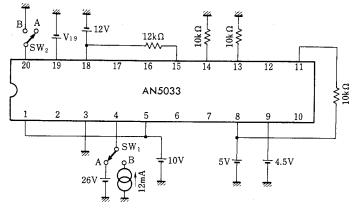
■ Absolute Maximum Ratings (Ta=25°C)

	Item		Symbol	Rat	ing	Unit	
	Supply Voltage V _{CC2}		V ₁₈₋₃	15		V	
	Supply Voltage	Vcc3	V_{8-3}	8		V	
Voltage Current	Circuit Voltage		V ₆₋₄ V ₇₋₃	0	+12	V	
			V ₁₅₋₃	0	+29	V	
			V_{19-3}	0	+ 8	V	
	Supply Current		I_4	0	+15	mA	
	Circuit Current		I ₆ , I ₇	0	+10	mA	
Current			I ₁₀ I ₁₂	-0.3	+ 5	mA	
			I ₁₃	-40	0	mA	
			I ₁₄	-30	0.	mA	
			I ₁₅	0	20	mA	
Power Dissipa	ation		P_{D}	85	50	mW	
Temperature	Operating Ambient Temperature		Торг	-20~+70		С	
1 omperature	Storage Temperature		T_{stg}	-55~+150		°C	

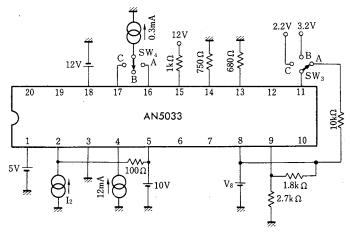
■ Electrical Characteristics (Ta=25°C)

Item	Symbol	Test	C I'r'		typ.	max.	Unit
		Circuit	Condition	min.			
V _{cc1} Circuit Current	I ₄	1	$S_1=A, V_{19}=0, S_2=A$	4.7	6.1	7.5	mA
V _{CC2} Circuit Current	I ₁₃	1	$S_1=B, V_{19}=0, S_2=A$	5.8	7.5	9.2	mA
V _{cc3} Circuit Current	I ₈	1	$S_1=B, V_{19}=0, S_2=A$	6.5	8.4	10.3	mA
DAI Input Current	I ₁₉	1	$S_1=B, V_{18}=4V, S_2=A$	1.5	2.2	2.9	mA
LFO Output Current	-I ₂₀	1	$S_1=B, V_{19}=0, S_2=B$	0.7	1.1	1.8	m A
BTI Input Current	I ₁	1	$S_1=B, V_{18}=0, S_2=A$	-1.0	-0.1	0	μΑ
BTI-BTO Voltege Difference	V_{1-2}	1	$S_1=B, V_{19}=0, S_2=A$	0	0.18	0.36	V
VRI Input Current	I _s	1	$S_1=B, V_{19}=0, S_2=A$	-15	- 5	0	μΑ
	V ₁₂₋₃₍₂₎	2	$V_8=4V, S_3=A, S_4=B$	0	0.1	0.3	V
V_{CC3} Rise-up Detection	V ₁₂₋₈	2	$V_8=5V, S_3=B, S_4=B$	-0.1	0	0.1	V
	V ₁₂₋₃₍₃₎	2	$V_8=5V, S_3=C, S_4=B$	0	0.1	0.3	V
BSI Terminal Voltage	V ₁₆₋₃	2	$V_8=5V$, $S_3=A$, $S_4=B$		2.2	2.5	v
DSI Terrimiai Voltage	V ₁₇₋₃			1.9			
BVO Output Voltage	V_{13-3}	2	$V_8=5V, S_3=A, S_4=B$	11.1	11.5	12.0	V
BUO Output Voltage	V ₁₄₋₃	2	$V_8=5V, S_3=A, S_4=A$	11.1	11.5	12.0	v
BSO Output Voltage	V ₁₆₋₃	2	$V_8=5V, S_3=A, S_4=B$	0	0.3	0.7	v
BSO Output Current	I ₁₅	2	$V_8=5V, S_3=A, S_4=C$	0		1	μΑ
V _{CC1} Voltage Regulator	V ₄₋₃	1	$S_1=B, V_{19}=0, S_2=A$	29.5	31.5	33.5	v
V _{cci} Operating Resistance	r ₄	1	$S_1=B, V_{19}=0, S_2=A$		10	25	Ω

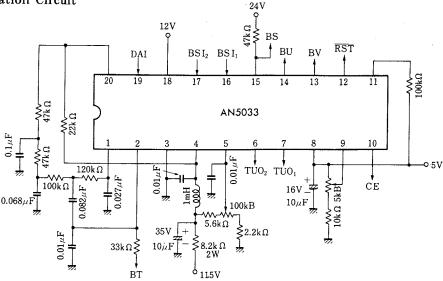
Test Circuit 1 $(I_{1, 4, 5, 8, 18, 19}, -I_{20}, V_{1-2}, V_{4-3}, r_4)$



Test Circuit 2 $(I_{15},\,V_{12-3(2)},\,V_{12-3(3)},\,V_{12-8},\,V_{13,\,14,\,15,\,16,\,17-3})$



Application Circuit



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