

DESCRIPTION

The HY628400A is a high-speed, low power and 4M bits CMOS SRAM organized as 512K words by 8 bits. The HY628400A uses Hyundai's high performance twin tub CMOS process technology and was designed for high-speed and low power circuit technology. It is particularly well suited for use in high-density and low power system applications. This device has a data retention mode that guarantees data to remain valid at the minimum power supply voltage of 2.0V.

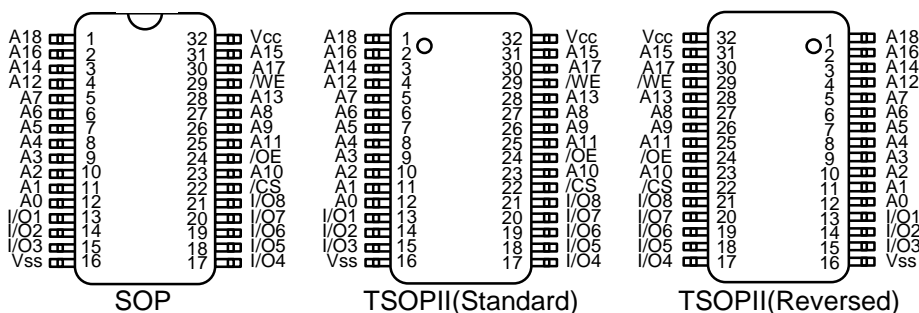
FEATURES

- Fully static operation and Tri-state outputs
- TTL compatible inputs and outputs
- Low power consumption
- Battery backup(L/LL-part)
 - . 2.0V(min) data retention
- Standard pin configuration
 - . 32pin 525mil SOP
 - . 32pin 400mil TSOP-II
 - (Standard and Reversed)

Product No.	Voltage	Speed	Operation	Standby Current(uA)		Temperature (°C)
	(V)	(ns)	Current/Icc(mA)	L	LL	
HY628400A	4.5~5.5	55/70/85	10	100	30	0~70

Note 1. Current value is max.

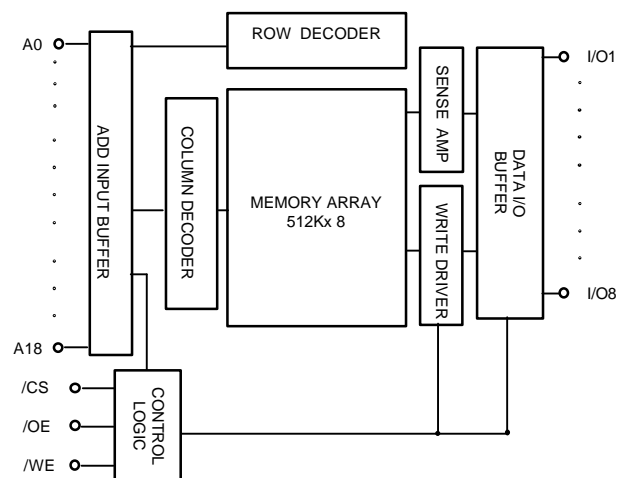
PIN CONNECTION



PIN DESCRIPTION

Pin Name	Pin Function
/CS	Chip Select
/WE	Write Enable
/OE	Output Enable
A0 ~ A18	Address Inputs
I/O1 ~ I/O8	Data Inputs/Outputs
Vcc	Power(4.5~5.5V)
Vss	Ground

BLOCK DIAGRAM



ORDERING INFORMATION

Part No.	Speed	Power	Temp	Package
HY628400ALG	55/70/85	L-part		SOP
HY628400ALLG	55/70/85	LL-part		SOP
HY628400ALT2	55/70/85	L-part		TSOP-II(Standard)
HY628400ALLT2	55/70/85	LL-part		TSOP-II(Standard)
HY628400ALR2	55/70/85	L-part		TSOP-II(Reversed)
HY628400ALLR2	55/70/85	LL-part		TSOP-II(Reversed)

ABSOLUTE MAXIMUM RATING (1)

Symbol	Parameter	Rating	Unit	Remark
V _{CC} , V _{IN} , V _{OUT}	Power Supply, Input/Output Voltage	-0.5 to 7.0	V	
T _A	Operating Temperature	0 to 70	°C	HY628400A
T _{STG}	Storage Temperature	-65 to 125	°C	
P _D	Power Dissipation	1.0	W	
T _{SOLDER}	Lead Soldering Temperature & Time	260 • 10	°C•sec	

Note

- Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is stress rating only and the functional operation of the device under these or any other conditions above those indicated in the operation of this specification is not implied. Exposure to the absolute maximum rating conditions for extended period may affect reliability.

TRUTH TABLE

/CS	/WE	/OE	MODE	I/O OPERATION	Power
H	X	X	Deselected	High-Z	Standby
L	H	H	Output Disabled	High-Z	Active
L	H	L	Read	Data Out	Active
L	L	X	Write	Data In	Active

Note :

- H=V_{IH}, L=V_{IL}, X=don't care (V_{IH} or V_{IL})

RECOMMENDED DC OPERATING CONDITION

$T_A = 0; \text{ to } 70; \text{ (Normal)}$

Symbol	Parameter	Min.	Typ.	Max.	Unit
V _{CC}	Supply Voltage	4.5	5.0	5.5	V
V _{SS}	Ground	0	0	0	V
V _{IH}	Input High Voltage	2.2	-	V _{CC} +0.5	V
V _{IL}	Input Low Voltage	-0.5(1)	-	0.8	V

Note :

1. V_{IL} = -1.5V for pulse width less than 30ns and not 100% tested.

DC ELECTRICAL CHARACTERISTICS

$T_A = 0^\circ\text{C to } 70^\circ\text{C}$ unless otherwise specified

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit	
I _{LI}	Input Leakage Current	$V_{SS} \leq V_{IN} \leq V_{CC}$	-1	-	1	uA	
I _{LO}	Output Leakage Current	$V_{SS} \leq V_{OUT} \leq V_{CC}$, /CS = V _{IH} or /OE = V _{IH} or /WE = V _{IL}	-1	-	1	uA	
I _{CC}	Operating Power Supply Current	/CS = V _{IL} , V _{IN} = V _{IH} or V _{IL} , I _{I/O} = 0mA	-	-	10	mA	
I _{CC1}	Average Operating Current	/CS = V _{IL} Min Duty Cycle = 100%, V _{IN} = V _{IH} or V _{IL} , I _{I/O} = 0mA	-	-	60	mA	
I _{SB}	TTL Standby Current (TTL Input)	/CS = V _{IH}	-	-	2	mA	
I _{SB1}	Standby Current (CMOS Input)	/CS \geq V _{CC} - 0.2V	L	-	-	100	uA
			LL	-	-	30	uA
V _{OL}	Output Low Voltage	I _{OL} = 2.1mA	-	-	0.4	V	
V _{OH}	Output High Voltage	I _{OH} = -1mA	2.4	-	-	V	

Note : Typical values are at V_{CC} = 5.0V, T_A = 25°C

CAPACITANCE

Temp = 25°C, f = 1.0MHz

Symbol	Parameter	Condition	Max.	Unit
C _{IN}	Input Capacitance	V _{IN} = 0V	6	pF
C _{OUT}	Output Capacitance	V _{I/O} = 0V	8	pF

Note : This parameter is sampled and not 100% tested

AC CHARACTERISTICS

TA = 0°C to 70°C unless otherwise specified

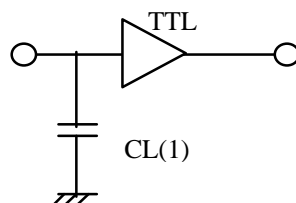
#	Symbol	Parameter	55ns		70ns		85ns		Unit
			Min.	Max.	Min.	Max.	Min	Max.	
READ CYCLE									
1	tRC	Read Cycle Time	55	-	70	-	85	-	ns
2	tAA	Address Access Time	-	55	-	70	-	85	ns
3	tACS	Chip Select Access Time	-	55	-	70	-	85	ns
4	tOE	Output Enable to Output Valid	-	25	-	40	-	45	ns
5	tCLZ	Chip Select to Output in Low Z	10	-	10	-	10	-	ns
6	tOLZ	Output Enable to Output in Low Z	5	-	5	-	5	-	ns
7	tCHZ	Chip Deselecting to Output in High Z	0	20	0	25	0	30	ns
8	tOHZ	Out Disable to Output in High Z	0	20	0	25	0	30	ns
9	tOH	Output Hold from Address Change	10	-	10	-	10	-	ns
WRITE CYCLE									
10	tWC	Write Cycle Time	55	-	70	-	85	-	ns
11	tCW	Chip Selection to End of Write	45	-	60	-	70	-	ns
12	tAW	Address Valid to End of Write	45	-	60	-	70	-	ns
13	tAS	Address Set-up Time	0	-	0	-	0	-	ns
14	tWP	Write Pulse Width	40	-	50	-	55	-	ns
15	tWR	Write Recovery Time	0	-	0	-	0	-	ns
16	tWHZ	Write to Output in High Z	0	20	0	25	0	30	ns
17	tDW	Data to Write Time Overlap	25	-	30	-	40	-	ns
18	tDH	Data Hold from Write Time	0	-	0	-	0	-	ns
19	tOW	Output Active from End of Write	5	-	5	-	5	-	ns

AC TEST CONDITIONS

TA = 0°C to 70°C unless otherwise specified

PARAMETER	Value
Input Pulse Level	0.8V to 2.4V
Input Rise and Fall Time	5ns
Input and Output Timing Reference Level	1.5V
Output Load	CL = 100pF + 1TTL Load

AC TEST LOADS

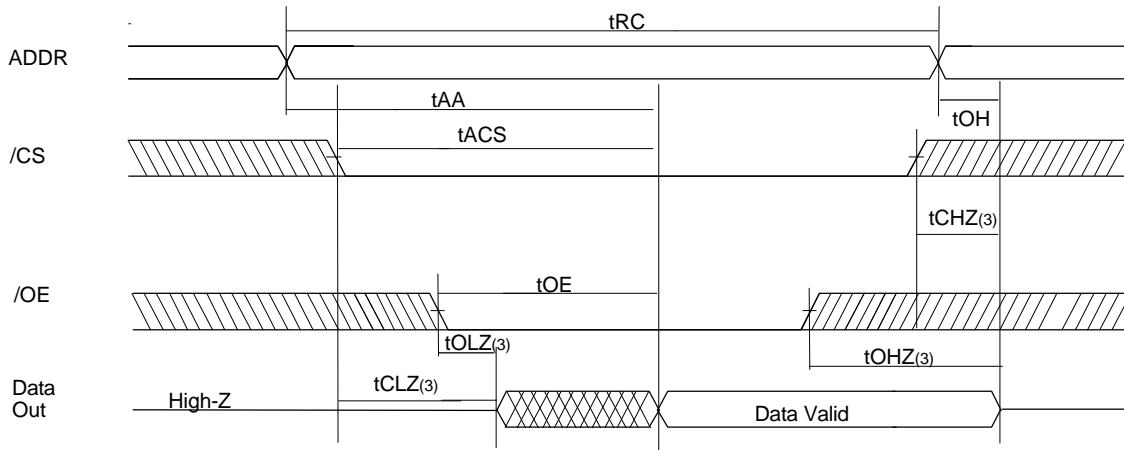


Note

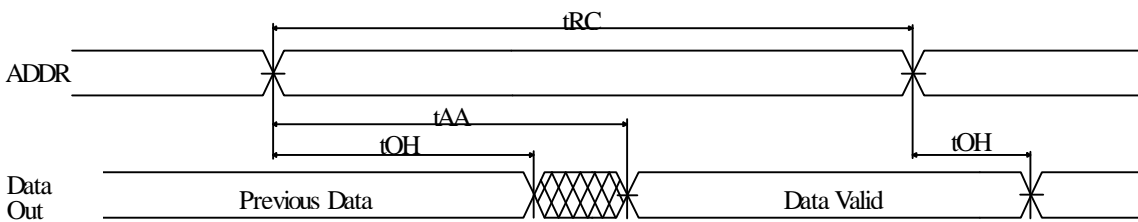
1. Including jig and scope capacitance

TIMING DIAGRAM

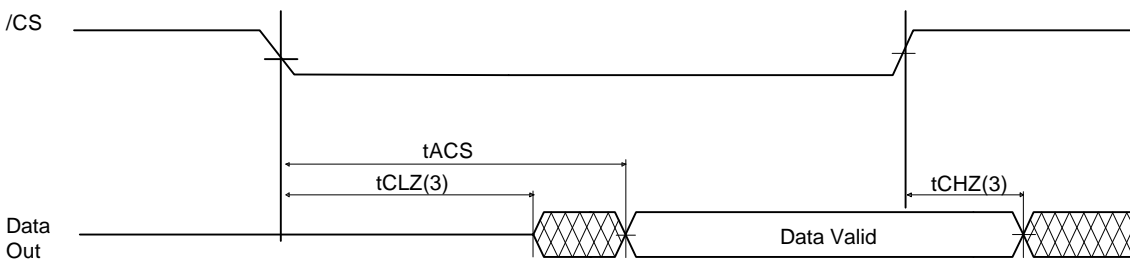
READ CYCLE 1(Note 1,4)



READ CYCLE 2(Note 1,2,4)



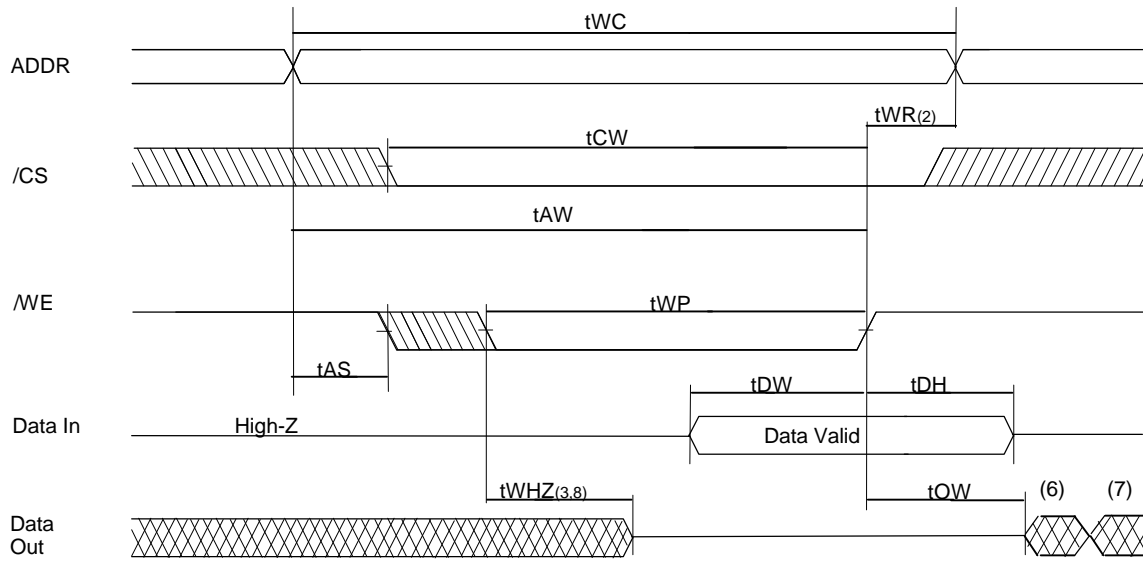
READ CYCLE 3(Note 1,2,4)



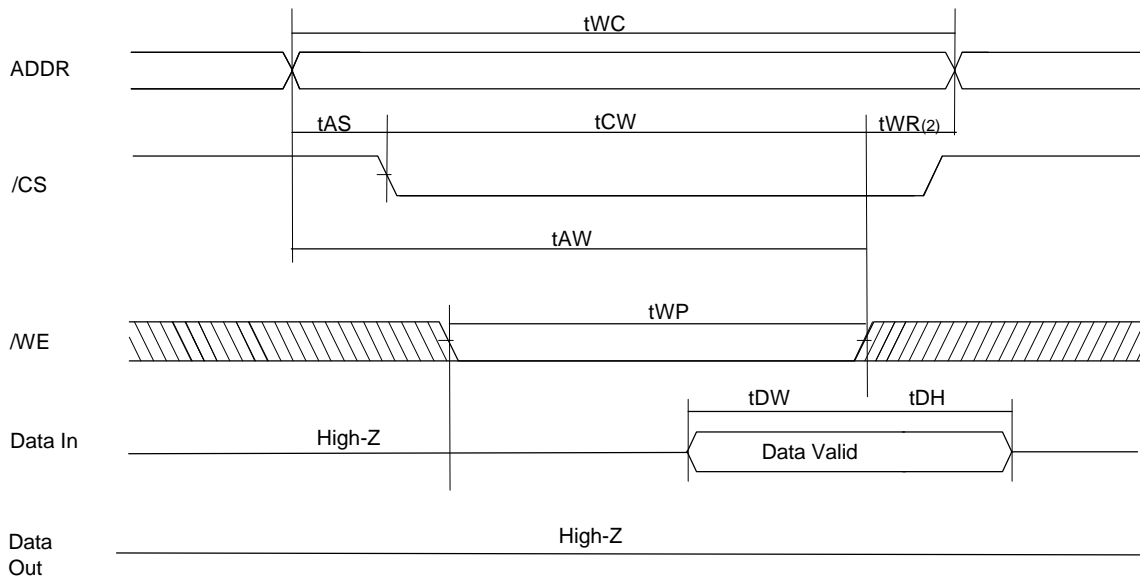
Notes:

1. Read Cycle occurs whenever a high on the /WE and /OE is low, and /CS are in active status.
2. /OE = V_{IL}
3. Transition is measured + 200mV from steady state voltage.
This parameter is sampled and not 100% tested.
4. /CS in high for the standby, low for active

WRITE CYCLE 1(1,4,5,9) (/WE Controlled)



WRITE CYCLE 2 (Note 1,4,5,9) (/CS Controlled)



Notes:

1. A write occurs whenever a low on the /WE and /OE is low while /CS are in active state.
2. tWR is measured from the earlier of /CS or /WE going high to the end of write cycle.
3. During this period, I/O pins are in the output state so that the input signals of opposite phase to the output must not be applied.
4. If the /CS low transition occur simultaneously with the /WE low transition or after the /WE transition, outputs remain in a high impedance state.
5. /OE is continuously low(/OE=V_{IL})
6. Q(data out) is the same phase with the write data of this write cycle.
7. Q(data out) is the read data of the next address.
8. Transition is measured + 200mV from steady state.
This parameter is sampled and not 100% tested.
9. /CS in high for the standby, low for active

DATA RETENTION ELECTRIC CHARACTERISTIC

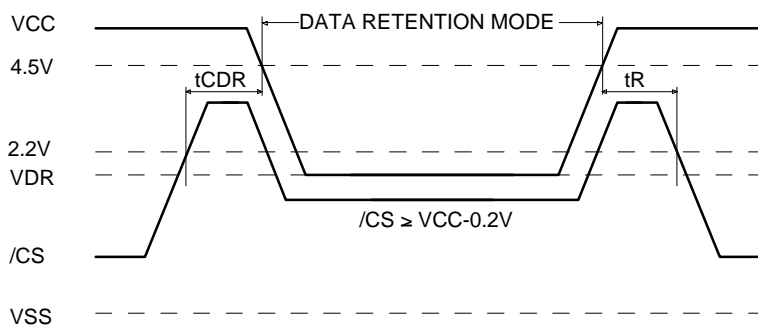
T_A=0°C to 70°C (Normal)

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit	
VDR	V _{cc} for Data Retention	/CS ≥ V _{cc} - 0.2V V _{ss} ≤ V _{IN} ≤ V _{cc}	2.0	-	-	V	
ICCDR	Data Retention Current	V _{cc} = 3.0V, /CS ≥ V _{cc} - 0.2V V _{ss} ≤ V _{IN} ≤ V _{cc}	L	-	-	50	uA
			LL	-	-	15	uA
tCDR	Chip Deselect to Data Retention Time		0	-	-	ns	
tR	Operating Recovery Time		tRC(2)	-	-	ns	

Notes:

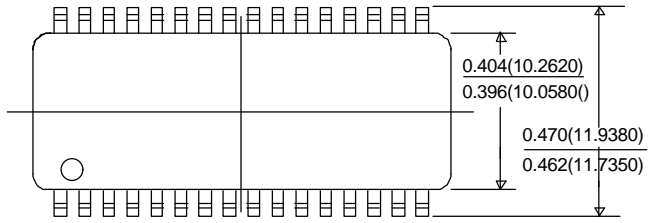
1. Typical values are at the condition of T_A = 25°C.
2. tRC is read cycle time.

DATA RETENTION TIMING DIAGRAM

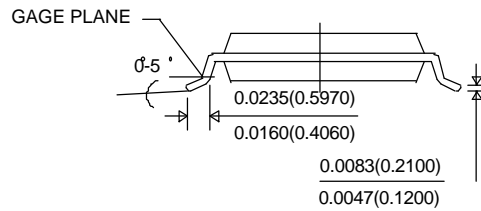
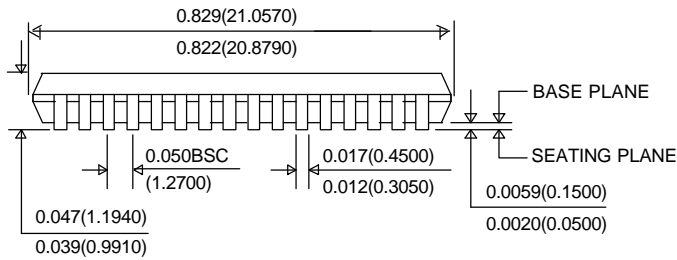


PACKAGE INFORMATION

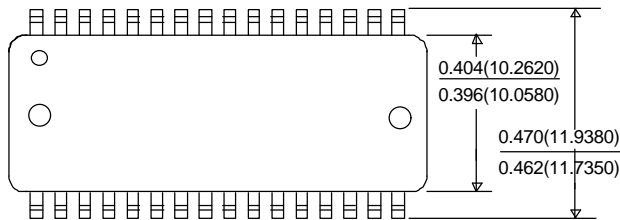
32pin 400mil Thin Small Outline Package Standard(T2)



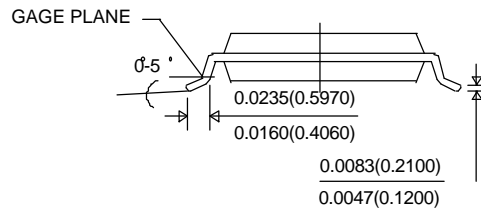
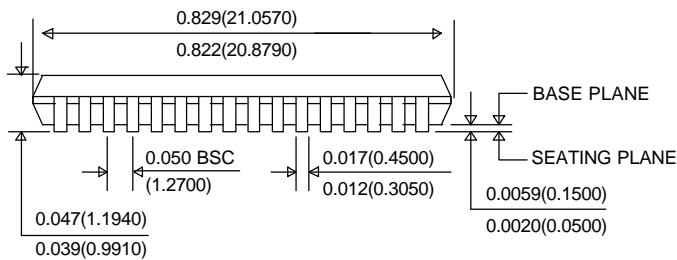
UNIT : INCH(mm) MAX.
MIN.



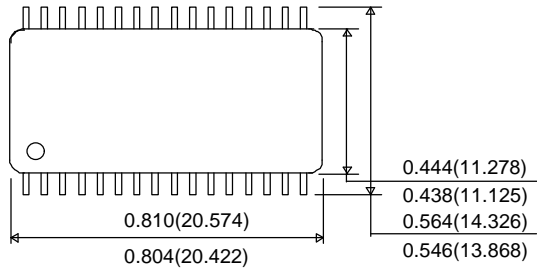
32pin 400mil Thin Small Outline Package Reversed(R2)



UNIT : INCH(mm) MAX.
MIN.



32pin 525mil Small Outline Package(G)



UNIT : INCH(mm)

