Integrated Device Technology, Inc.

8K x 8
4K x 8
CMOS FourPort™ RAM MODULE

PRELIMINARY
IDT7MB1041
IDT7MB1042

FEATURES:

- High-density 64K/32K-bit CMOS FourPort RAM Modules
- 8K x 8 (IDT7MB1041) or 4K x 8 (IDT7MB1042) option
- Fast access times
  - maximum: 35, 40, 45, 55, 65, 80, 100ns
- Fully asynchronous operation from any four ports: P1, P2, P3, P4
- Versatile control for write-inhibit: separate $\overline{BUSY}$ input to control write-inhibit for each of the other 3 ports
- Battery backup operation - 2V data retention (low power version only)
- Surface mounted fine pitch (25 mil) PQFP (Plastic Quad FlatPack) components on a FR-4 120-pin QIP (Quad In-line Package) substrate
- TTL compatible I/Os
- Single 5V (± 10%) power supply
- Multiple ground pins provide maximum noise immunity
- Input/outputs directly TTL compatible

DESCRIPTION:

The IDT7MB1041/1042 are 64/32K-bit high-speed CMOS FourPort RAM modules constructed on a multi-layer FR-4 substrate using 4 IDT7052 (2K x 8) FourPort RAMs or a depopulated version with 2 IDT7052 FourPort RAMs. The IDT7MB1041/1042 modules are designed to be used as stand-alone 64K/32K-bit fourport RAM. Using the IDT FourPort Module in such system applications as multiprocessor or real time data acquisition result in dramatically increased system performance by providing four independent ports with separate control, address, and I/O pins that permit independent and asynchronous access for reads or writes to any location in memory. Upper and lower byte module signals for each port provide the system additional memory control capability.

The IDT7MB1041/1042 modules are packaged in a 120-pin FR-4 QIP (Quad In-line Package) and have maximum access times of 35ns over the commercial temperature range.

PIN NAMES (1, 2)

P1-4A0 - 12	Ports 1-4, Address Inputs
P1-4I/O0 - 7	Port 1-4, Data Inputs/Outputs
R/$\overline{W}$ P1	ReadWrite - Port 1
R/$\overline{W}$ P2	Read/Write - Port 2
R/$\overline{W}$ P3	Read/Write - Port 3
R/$\overline{W}$ P4	Read/Write - Port 4
$\overline{CS}$ P1	Chip Select - Port 1
$\overline{CS}$ P2	Chip Select - Port 2
$\overline{CS}$ P3	Chip Select - Port 3
$\overline{CS}$ P4	Chip Select - Port 4
$\overline{OE}$ P1	Output Enable - Port 1
$\overline{OE}$ P2	Output Enable - Port 2
$\overline{OE}$ P3	Output Enable - Port 3
$\overline{OE}$ P4	Output Enable - Port 4
$\overline{BUSY}$ P1	Port Busy Write Disable - Port 1
$\overline{BUSY}$ P2	Port Busy Write Disable - Port 2
$\overline{BUSY}$ P3	Port Busy Write Disable - Port 3
$\overline{BUSY}$ P4	Port Busy Write Disable - Port 4
Vcc	Power
GND	Ground

2802 tbl 01

PIN CONFIGURATION

Note: Pin configurations for these modules are currently not available, please consult the factory.

Notes:
1. For valid read operation, no other part may write to the same address location at the same time.
2. For the IDT7MB1042 (4K x 8) version, P1A12, P2A12, P3A12, P4A12 must be connected to GND for proper operation of the module.

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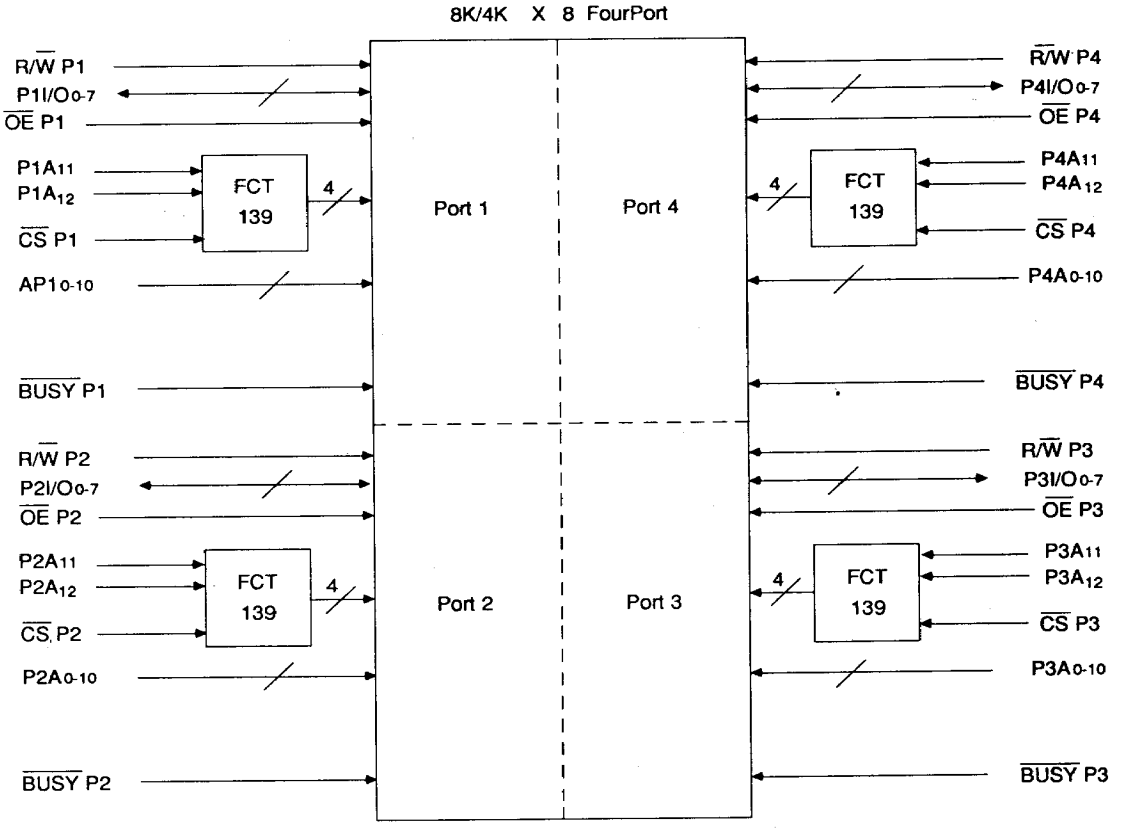
FUNCTIONAL BLOCK DIAGRAM



2802 drw 01

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ABSOLUTE MAXIMUM RATINGS(1)

Symbol	Rating	Commercial	Military	Unit
VTERM	Terminal Voltage with Respect to GND	-0.5 to ± 7.0	-0.5 to ± 7.0	V
TA	Operating Temperature	0 to +70	-55 to + 125	°C
TBIAS	Temperature Under Bias	-55 to + 125	-65 to + 135	°C
TSTG	Storage Temperature	-55 to +125	-65 to +150	°C
IOUT	DC Output Current	50	50	mA

2802 tbl 02

NOTE:

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED OPERATING TEMPERATURE AND SUPPLY VOLTAGE

Grade	Ambient Temperature	GND	Vcc
Commercial	0°C to + 70°C	OV	5.0V± 10%

2801 tbl 03

RECOMMENDED DC OPERATING CONDITIONS

Symbol	Parameter	Min.	Typ.	Max.	Unit
Vcc	Supply Voltage	4.5	5.0	5.5	V
GND	Supply Voltage	0	0	0	V
VIH	Input High Voltage	2.2	—	6.0	V
VIL	Input Low Voltage	-0.5(1)	—	0.8	V

2802 tbl 04

NOTE:

1. VIL (min.) = -3.0V for pulse width less than 20ns.

DC ELECTRICAL CHARACTERISTICS

(Vcc=5.0V ± 10%, TA = 0°C to +70°C)

Symbol	Parameter	Test Conditions	Min.	Max.	Unit
|ILI|	Input Leakage Current	Vcc = 5.5V, VIN = 0V to Vcc	—	40	µA
|ILO|	Output Leakage Current	$\overline{CS}$ = VIH, VOUT = 0V to Vcc	—	40	µA
VOL	Output Low Voltage	IOL = 4mA	—	0.4	V
VOH	Output High Voltage	IOH = -4mA	2.4	—	V

2802 tbl 05

CAPACITANCE(1) (TA= +25°C, F = 1.0 MHz)

Symbol	Parameter	Test Conditions	IDT7MB1041/1042 Max.	Max.	Unit
CIN1	Input Capacitance	VIN = 0V	12	12	pF
CIN2	Input Capacitance (Data, Address, All Other Controls)	VIN = 0V	50	25	pF
COUT	Output Capacitance (Data)	VOUT = 0V	45	25	pF

2802 tbl 06

NOTE:

1. This parameter is guaranteed by design but not tested.

DC ELECTRICAL CHARACTERISTICS

(Vcc=5.0V ± 10%, TA = 0°C to +70°C)

Symbol	Parameter	Test Conditions	IDT7MB1041 Min.	Max.	IDT7MB1042 Min.	Max.	Unit
ICC1	Operating Power Supply Current (All Ports Active)	$\overline{CS}$ ≥ VIL, Outputs Open f = 0	—	550	—	400	mA
ICC2	Dynamic Operating Current	$\overline{CS}$ ≥VIL, Outputs Open f = fMAX	—	600	—	430	mA
ISB	Standby current (All Ports - TTL Level Inputs)	$\overline{CS}$ = VIH, Outputs Open f = fMAX	—	340	—	170	mA
ISB1	Full Standby Current (All Ports - All CMOS Level Inputs)	All Ports $\overline{CS}$ ≥ Vcc -0.2V VIN ≥Vcc -0.2V or VIN ≤ 0.2V, f = 0	—	20	—	10	mA

2802 tbl 07

AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	5ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figures 1 and 2

2802 tbl 08

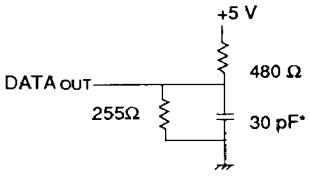


Figure 1. Output Load

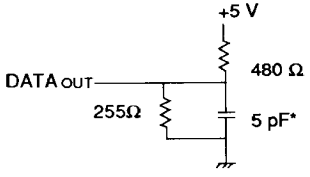


Figure 2. Output Load (for tCLZ, tCHZ, tOLZ, tOHZ, tWHZ, tOW)

*Including scope and jig.

2802 drw 02

AC ELECTRICAL CHARACTERISTICS(1)

(VCC = 5.0V ± 10%, TA = 0°C to +70°C)

Symbol	Parameter	7MB1041S35 7MB1042S35 Min.	Max.	7MB1041S40 7MB1042S40 Min.	Max.	7MB1041S45 7MB1042S45 Min.	Max.	7MB1041S55 7MB1042S55 Min.	Max.	7MB1041S65 7MB1042S65 Min.	Max.	7MB1041S80 7MB1042S80 Min.	Max.	7MB1041S100 7MB1042S100 Min.	Max.	Unit
Read Cycle																
tRC	Read Cycle Time	35	—	40	—	45	—	55	—	65	—	80	—	100	—	ns
tAA	Address Access Time	—	35	—	40	—	45	—	55	—	65	—	80	—	100	ns
tACS	Chip Select Access Time	—	35	—	40	—	45	—	55	—	65	—	80	—	100	ns
tOE	Output Enable Access Time	—	25	—	25	—	30	—	40	—	50	—	65	—	85	ns
tOH	Output Hold From Address Change	0	—	0	—	0	—	0	—	0	—	0	—	0	—	ns
tCLZ(2)	Chip Select to Output in Low Z	3	—	5	—	5	—	5	—	5	—	10	—	10	—	ns
tOLZ(2)	Output Enable to Output in Low Z	3	—	5	—	5	—	5	—	5	—	10	—	10	—	ns
tCHZ(2)	Chip Deselect to Output in High Z	20	—	20	—	25	—	25	—	25	—	30	—	30	—	ns
tOHZ(2)	Output Disable to Output in High Z	20	—	20	—	25	—	25	—	25	—	30	—	30	—	ns
tPU(2)	Chip Enable to Power Up Time	0	—	0	—	0	—	0	—	0	—	0	—	0	—	ns
tPD(2)	Chip Disable to Power Down Time	—	35	—	55	—	55	—	50	—	70	—	70	—	70	ns

2802 tbl 09

NOTES:
1. Transition is measured by ±500mV from low or high impedance voltage with load (Figures 1 and 2).
2. This parameter is guaranteed by design but not tested.

8

AC ELECTRICAL CHARACTERISTICS(1)

(V_{CC} = 5.0V ± 10%, T_A = 0°C to +70°C)

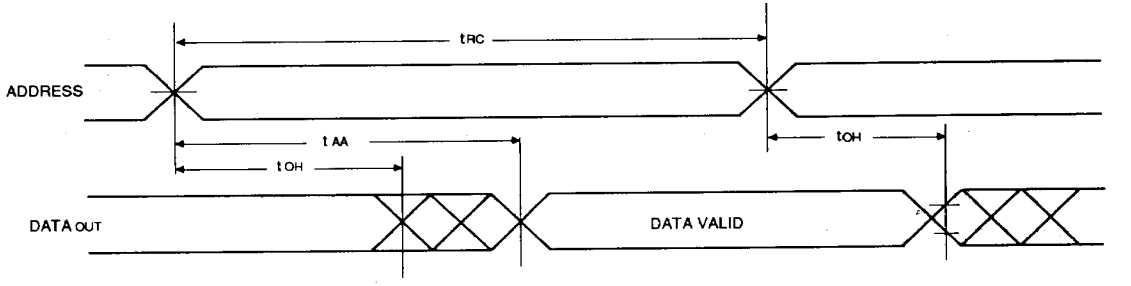
Symbol	Parameter	7MB1041S35 7MB1042S35 Min.	Max.	7MB1041S40 7MB1042S40 Min.	Max.	7MB1041S45 7MB1042S45 Min.	Max.	7MB1041S55 7MB1042S55 Min.	Max.	7MB1041S65 7MB1042S65 Min.	Max.	7MB1041S80 7MB1042S80 Min.	Max.	7MB1041S100 7MB1042S100 Min.	Max.	Unit
Write Cycle																
t_{WC}	Write Cycle Time	35	—	40	—	45	—	55	—	65	—	80	—	100	—	ns
t_{CW}	Chip Select to End of Write	30	—	35	—	35	—	45	—	55	—	70	—	90	—	ns
t_{AW}	Address Valid to End of Write	30	—	35	—	35	—	45	—	55	—	70	—	90	—	ns
t_{AS1}	Address Set-up to $\overline{CS}$ Time	0	—	0	—	0	—	0	—	0	—	0	—	0	—	ns
t_{AS2}	Address Set-up to R/$\overline{W}$ Time	5	—	5	—	5	—	5	—	5	—	5	—	5	—	ns
t_{WP}	Write Pulse Width	25	—	30	—	35	—	45	—	45	—	45	—	45	—	ns
t_{WR}	Write Recovery Time	5	—	5	—	5	—	5	—	5	—	5	—	5	—	ns
t_{DW}	Data Valid to End of Write	20	—	20	—	20	—	20	—	20	—	30	—	30	—	ns
t_{DH}	Data Hold Time	0	—	0	—	0	—	0	—	0	—	0	—	0	—	ns
t_{WHZ}(2)	Write Enabled to Output in High Z	—	18	—	18	—	20	—	20	—	20	—	30	—	30	ns
t_{OW}	Output Active from End of Write	0	—	0	—	0	—	0	—	0	—	0	—	0	—	ns
t_{WDD}	Write Pulse to Data Delay	—	50	—	65	—	70	—	80	—	80	—	90	—	100	ns
t_{DDD}	Write Data Valid to Read Data Delay	—	40	—	45	—	45	—	55	—	65	—	80	—	100	ns
Busy Input Timing																
t_{WB}	Write to $\overline{BUSY}$	0	—	0	—	0	—	0	—	0	—	0	—	0	—	ns
t_{WH}	Write Hold After $\overline{BUSY}$	20	—	20	—	25	—	25	—	25	—	30	—	30	—	ns

NOTES:

2802 tbl 10

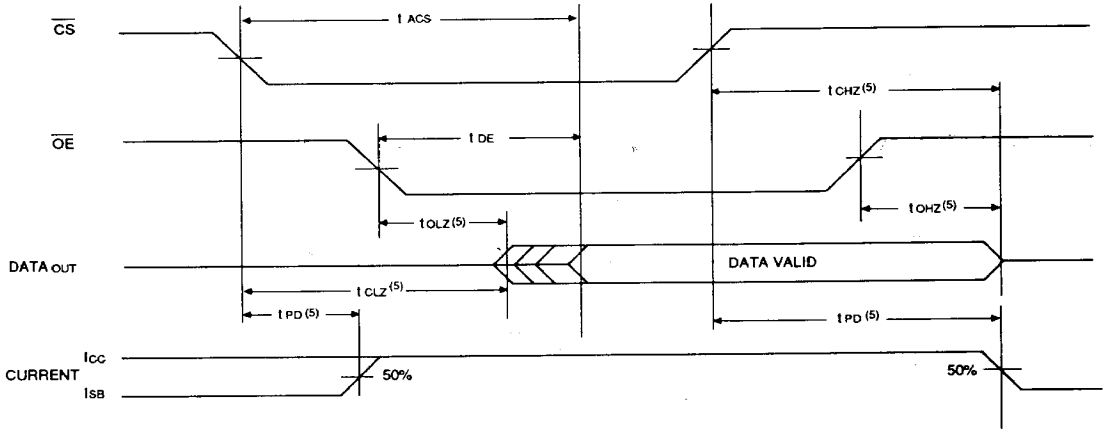
1. Transition is measured by ±500mV from low or high impedance voltage with load (Figures 1 and 2).
2. This parameter is quaranteed by design but not tested.

TIMING WAVEFORM OF READ CYCLE NO. 1, ANY PORT(1,2,4)



2802 drw 03

TIMING WAVEFORM OF READ CYCLE NO. 2, ANY PORT(1,3)

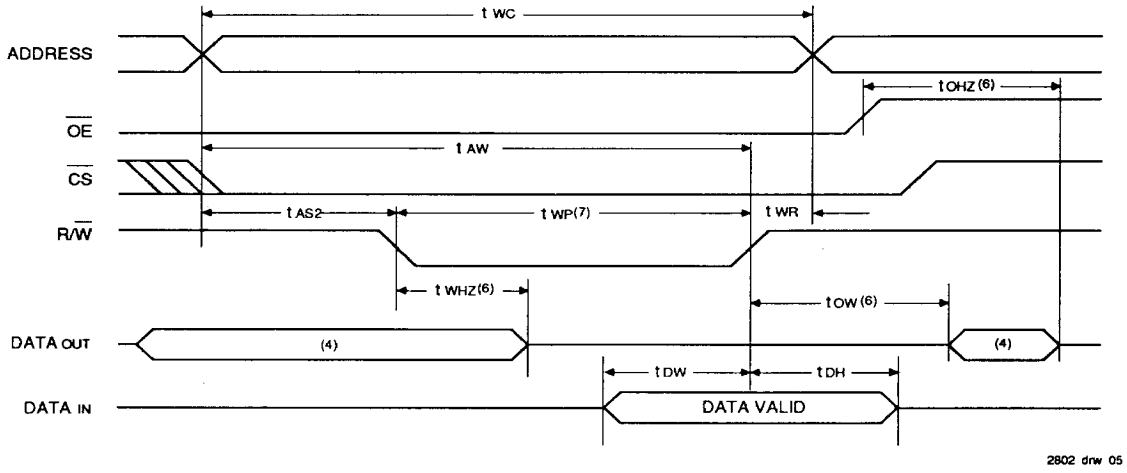


2802 drw 04

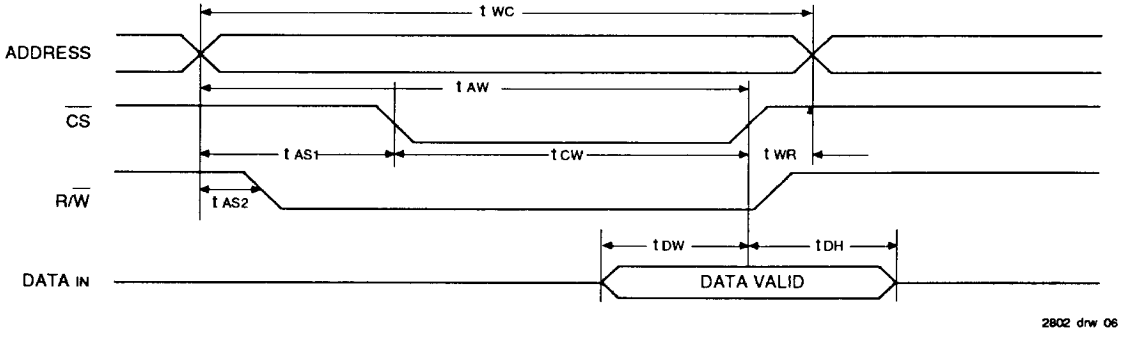
NOTES:
1. R/$\overline{W}$ is high for Read Cycles.
2. Device is continuously enabled. $\overline{CS} \geq V_{IL}$.
3. Addresses valid prior to or coincident with $\overline{CS}$ transition low.
4. $\overline{OE} \geq V_{IL}$.
5. This parameter is guaranteed by design but not tested.

8

TIMING WAVEFORM OF WRITE CYCLE NO. 1, R/$\overline{W}$ CONTROLLED TIMING(1,2,3,7)

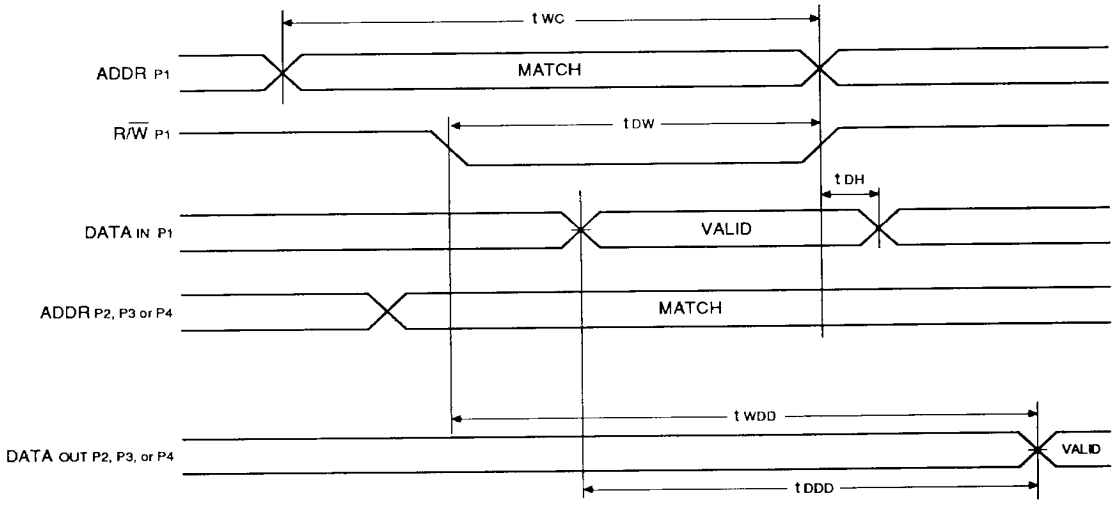


TIMING WAVEFORM OF WRITE CYCLE NO. 2, $\overline{CS}$ CONTROLLED TIMING(1,2,3,5)



NOTES:
1. R/$\overline{W}$ must be high during all address transitions.
2. A write occurs during the overlap (tWP) of a low $\overline{CS}$ and a low R/$\overline{W}$.
3. tWR is measured from the earlier of $\overline{CS}$ or R/$\overline{W}$ going high to the end of the write cycle.
4. During this period, the I/O pins are in the output state, and input signals must not be applied.
5. If the $\overline{CS}$ low transition occurs simultaneously with or after the R/$\overline{W}$ low transition, the ouputs remain in the high impedance state.
6. Transition is measured ±500mV from steady state with a 5pF load (including scope and jig). This parameter is guaranteed by design but not tested.
7. If $\overline{OE}$ is low during a R/$\overline{W}$ controlled write cycle, the write pulse width must be the larger of tWP or (tWZ + tDW) to allow the I/O drivers to turn off data to be placed on the busfor the required tDW. If $\overline{OE}$ is high during a R/$\overline{W}$ controlled write cycle, this requirement does not apply and the write pulse can be as short as the specified tWP.

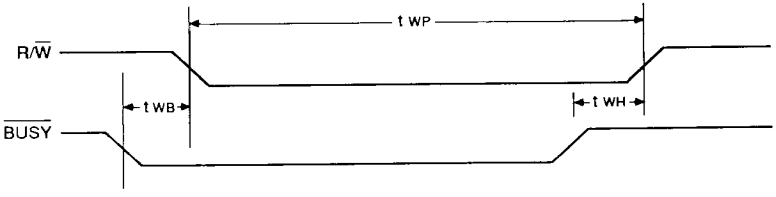
TIMING WAVEFORM OF READ WITH PORT-TO-PORT DELAY(1,2,3)



2802 drw 07

NOTES:
1. Assume $\overline{BUSY}$ input at High and $\overline{CS}$ at Low for the writing port.
2. Write cycle parameters should be adhered to, to ensure proper writing.
3. Device is continuously enabled for any of the reading ports which has its $\overline{OE}$ at Low.

TIMING WAVEFORM OF WRITE WITH $\overline{BUSY}$ INPUT



2802 drw 08

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FUNCTIONAL DESCRIPTION

The IDT7MB1041/1042 provides four ports with separate control, address and I/O pins that permit independent access for reads or writes to any location in memory. These devices have an automatic power down feature controlled by $\overline{CS}$. The $\overline{CS}$ controls on-chip power down circuitry that permits the respective port to go into standby mode when not selected ($\overline{CS}$ high). When a port is enabled, access to the entire memory array is permitted. Each port has its own Output Enable control ($\overline{OE}$). In the read mode, the port's $\overline{OE}$ turns on the output drivers when set LOW. READ/WRITE conditions are illustrated in the table below.

READ/WRITE CONTROL

ANY PORT					
$\overline{CS}$	R/$\overline{W}$	$\overline{OE}$	$\overline{BUSY}$	I/O$_{0-7}$	FUNCTION
H	X	X	X	HI-Z	Port Disabled and in Power Down Mode
L	L	X	H	DATA$_{IN}$	Write Cycle
X	L	X	L	HI-Z	Write is Blocked
L	H	L	X	DATA$_{OUT}$	Read Cycle
X	X	H	X	HI-Z	High Impedance Outputs

2802 drw 11

NOTES:
1. H = High, L - Low, X = Don't Care, Z = High Impedance.
2. If $\overline{BUSY}$ = Low, Data is not written.
3. For valid write operation, no more than one port can write to the same address location at the same time.

ORDERING INFORMATION