SANYO No.2422

LC3518B-10/12/15, LC3518BL-10/12/15

Asynchronous Silicon Gate CMOS LSI

2048 WORDS x 8 BITS CMOS STATIC RAM

General Description

The LC3518B/BL are fully asynchronous silicon gate CMOS static RAMs organized as 2048 words x 8 bits.

The LC3518B/BL have two chip enable inputs: $\overline{CE1}$, $\overline{CE2}$ for low standby current mode being valid at the time of battery backup usage.

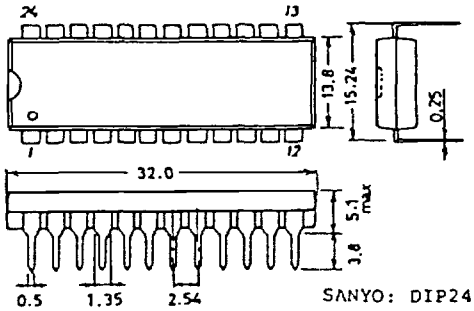
The LC3518B/BL have a full CMOS circuit configuration. Since the current dissipation is low at the data retention mode or standby mode, they are especially suited for use in memory systems whose power dissipation must be minimized and battery-powered portable systems.

The LC3518BL guarantees a maximum standby current of 1uA at 60°C.

Features

- Address access time (t_{AA})
  - 100ns(max): LC3518B-10/BL-10
  - 120ns(max): LC3518B-12/BL-12
  - 150ns(max): LC3518B-15/BL-15
- Low current dissipation
  - Standby mode
    - 0.2uA(max) /Ta=25°C } LC3518BL-10/12/15
    - 1.0uA(max) /Ta=60°C }
    - 5.0uA(max) /Ta=60°C } LC3518B-10/12/15
    - 30uA(max) /Ta=85°C }
  - Operating mode
    - 9mA(max) (at f=1MHz)
- Single 5V supply: 5V±10%
- Data retention supply voltage: 2.0 to 5.5V
- No clock required (Fully static memory)
- Directly TTL compatible: All inputs and outputs
- Common data input and output using 3-state outputs
- 24-pin plastic DIP package

Case Outline 3072-D24NSEC
(unit:mm)



SANYO: DIP24

These specifications are subject to change without notice.

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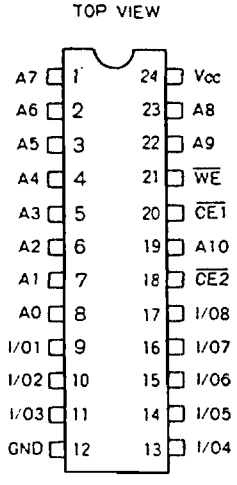
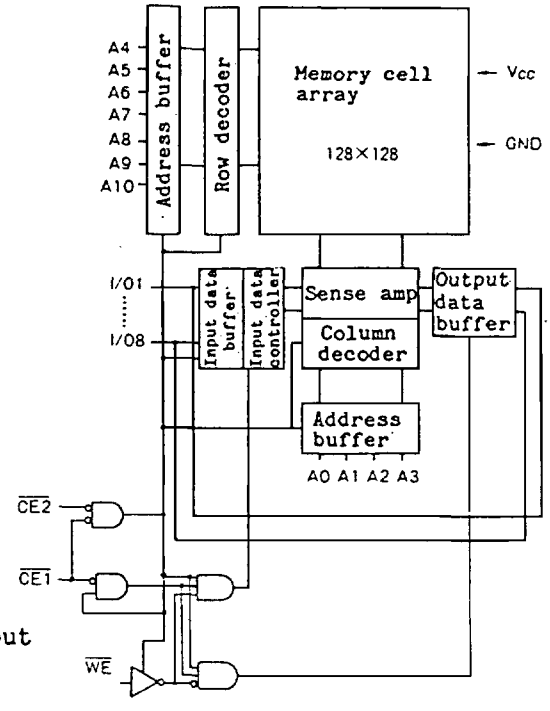
Pin Assignment



Block Diagram



A0 to A10	Address input
$\overline{WE}$	Read/write control input
$\overline{CE1}$	Chip enable input
$\overline{CE2}$	Chip enable input
I/01 to I/08	Data input/output
V_{CC}/GND	Power supply pin

Function Table

Mode	$\overline{CE2}$	$\overline{CE1}$	$\overline{WE}$	I/O	Supply Current
Read Cycle	L	L	H	Data output	I_{CCA}
Write Cycle	L	L	L	Data input	I_{CCA}
Nonselect	X	H	X	High impedance	I_{CCS}
Nonselect	H	X	X	High impedance	I_{CCS}

X:H or L

Absolute Maximum Ratings

Parameter	Symbol	Conditions	Limits	unit
Maximum Supply Voltage	$V_{CC}max$		+7.0	V
Input Pin Voltage	V_{IN}		-0.3 to V_{CC}+0.3	V
I/O Pin Voltage	$V_{I/O}$		-0.3 to V_{CC}+0.3	V
Operating Temperature	Topg		-30 to +85	°C
Storage Temperature	Tstg		-55 to +125	°C

DC Allowable Operating Conditions at Ta=-30 to +85°C

Parameter	Symbol	min	typ	max	unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Input "H"-Level Voltage	V_{IH}	2.2		V_{CC}+0.3	V
Input "L"-Level Voltage	V_{IL}	-0.3		0.8	V

DC Electrical Characteristics at Ta=-30 to 85°C, V_{CC}=5V±10%

Parameter	Symbol	Conditions			min	typ*	max	unit
Input Leak Current	I_{LI}	V_{IN}=0 to V_{CC}			-1.0		1.0	uA
I/O Leak Current	I_{LO}	$V_{\overline{CE1}}$ or $V_{\overline{CE2}}$=V_{IH}, $V_{I/O}$=0 to V_{CC}			-5.0		5.0	uA
Supply Current(DC)	I_{CCA1}	$V_{\overline{CE1}}$=0V, $V_{\overline{CE2}}$=0V, V_{IN}=V_{CC}/GND, $I_{I/O}$=0mA				2	5	mA
	I_{CCA2}	$V_{\overline{CE1}}$=V_{IL}, $V_{\overline{CE2}}$=V_{IL}, V_{IN}=V_{IH}/V_{IL}, $I_{I/O}$=0mA				5	15	mA
Average Supply Current	I_{CCA3}	min cycle, duty=100%, $I_{I/O}$=0mA					50	mA
	I_{CCA4}	Cycle time=1us, $V_{\overline{CE1}}$=0V, $V_{\overline{CE2}}$=0V V_{IN}=V_{CC}/GND, $I_{I/O}$=0mA				4	9	mA
Standby Supply Current	I_{CCS1}	$V_{\overline{CE1}}$=V_{CC}-0.2V or $V_{\overline{CE2}}$=V_{CC}-0.2V V_{IN}=0 to V_{CC}	LC3518B -10/12/15	Ta=60°C			5.0	uA
				Ta=85°C			30	uA
			LC3518BL -10/12/15	Ta=25°C			0.2	uA
				Ta=60°C			1.0	uA
	I_{CCS2}	$V_{\overline{CE1}}$=V_{IH} or $V_{\overline{CE2}}$=V_{IH}, V_{IN}=0 to V_{CC}				1.0	3.0	mA
Output "H"-Level Voltage	V_{OH}	I_{OH}=-1.0mA			2.4			V
Output "L"-Level Voltage	V_{OL}	I_{OL}=2.0mA					0.4	V

* Reference value at V_{CC}=5.0V, Ta=+25°C

Input/Output Capacitance at Ta=+25°C, f=1MHz

Parameter	Symbol	Conditions	min	typ	max	unit
Input/Output Capacitance	$C_{I/O}$	$V_{I/O}$=0V			10	pF
Input Capacitance	C_{IN}	V_{IN}=0V			5	pF

AC Electrical Characteristics at Ta=-30 to +85°C, V_{CC}=5V±10%

AC Test Conditions

Input pulse voltage level: 0.6V, 2.4V

Input rise/fall time: 5ns

Input/output timing level: Input "H" level V_{IH}=2.2V, Output "H" level V_{OH}=2.2V
Input "L" level V_{IL}=0.8V, Output "L" level V_{OL}=0.8V

Output load: 1TTL gate + C_L=100pF
(Including jig capacitance)

Read Cycle

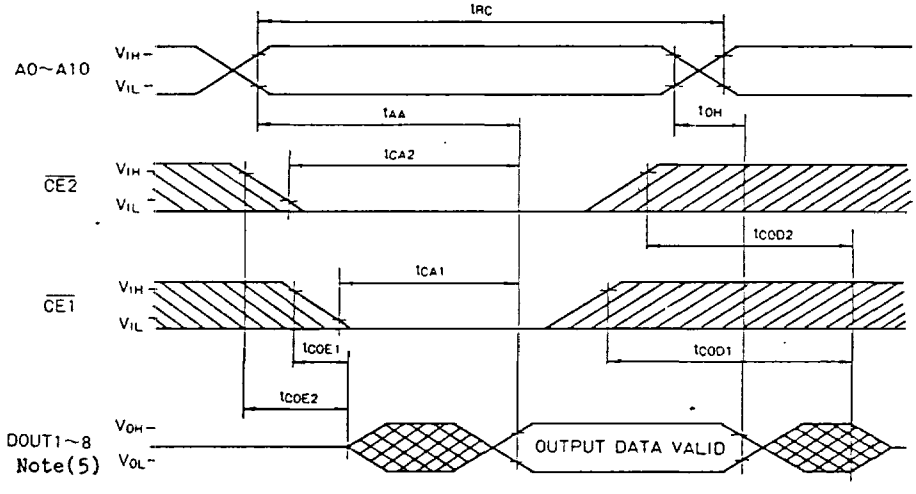
Parameter	Symbol	LC3518B-10 LC3518BL-10		LC3518B-12 LC3518BL-12		LC3518B-15 LC3518BL-15		unit
		min	max	min	max	min	max	
Read Cycle Time	t_{RC}	100		120		150		ns
Address Access Time	t_{AA}		100		120		150	ns
$\overline{CE1}$ Access Time	t_{CA1}		100		120		150	ns
$\overline{CE2}$ Access Time	t_{CA2}		100		120		150	ns
Output Hold Time	t_{OH}	20		20		20		ns
$\overline{CE1}$-Output Enable Time	t_{COE1}	10		10		10		ns
$\overline{CE2}$-Output Enable Time	t_{COE2}	10		10		10		ns
$\overline{CE1}$-Output Disable Time	t_{COD1}		30		40		50	ns
$\overline{CE2}$-Output Disable Time	t_{COD2}		30		40		50	ns

Write Cycle

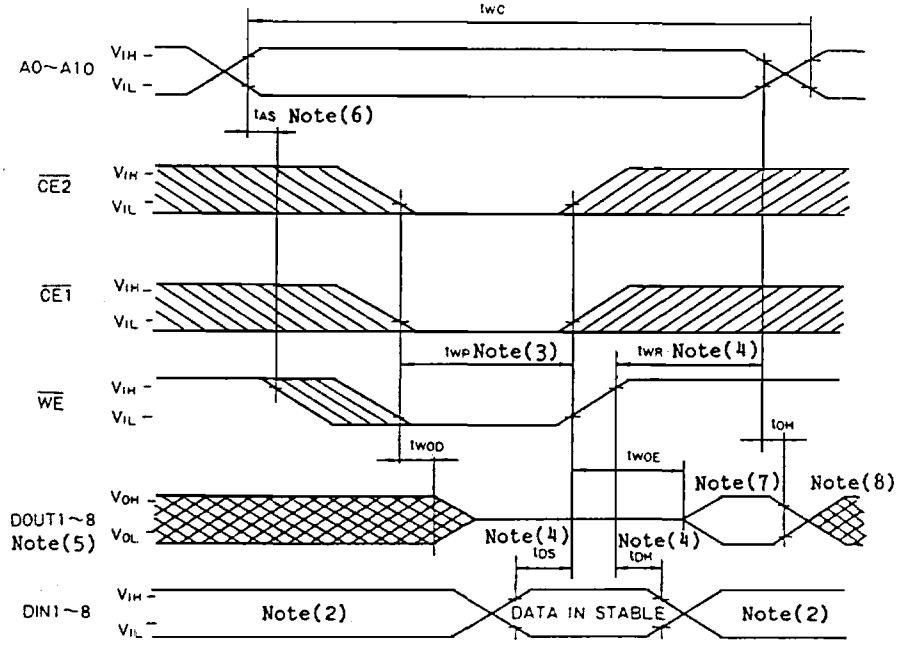
Parameter	Symbol	LC3518B-10 LC3518BL-10		LC3518B-12 LC3518BL-12		LC3518B-15 LC3518BL-15		unit
		min	max	min	max	min	max	
Write Cycle Time	t_{WC}	100		120		150		ns
Address Setup Time	t_{AS}	0		0		0		ns
Write Pulse Width	t_{WP}	80		100		120		ns
Write Recovery Time	t_{WR}	0		0		0		ns
Data Setup Time	t_{DS}	50		60		70		ns
Data Hold Time	t_{DH}	0		0		0		ns
$\overline{WE}$-Output Enable Time	t_{WOE}	5		5		5		ns
$\overline{WE}$-Output Disable Time	t_{WOD}		30		40		50	ns

Timing Chart

[Read Cycle] Note(1)



[Write Cycle 1]



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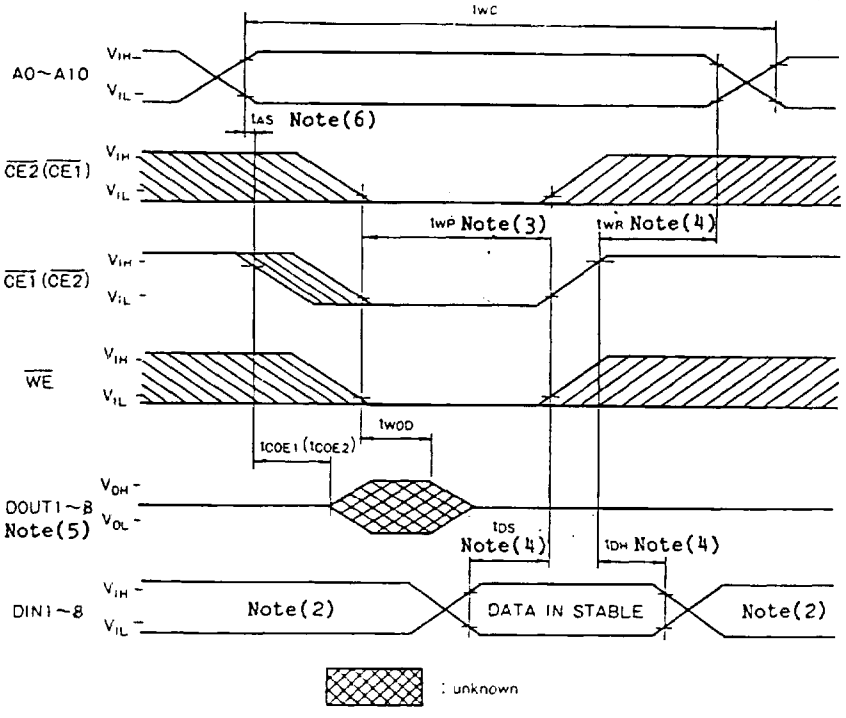
[Write Cycle 2]



Note) (1) $\overline{WE}$ must be high during read cycle.
(2) When D_{OUT} is in the output state, no opposite phase signal must be applied externally.
(3) A write occurs during the overlap of a low $\overline{CE1}$, $\overline{CE2}$ and a low $\overline{WE}$.
(4) t_{WR}, t_{DS}, t_{DH} are referenced to the earliest going high of $\overline{CE1}$, $\overline{CE2}$ or $\overline{WE}$.
(5) D_{OUT} is in a high impedance state when $\overline{CE1}$ is high or $\overline{CE2}$ is high or $\overline{WE}$ is low.
(6) t_{AS} is referenced to the point at which all of $\overline{CE1}$, $\overline{CE2}$, $\overline{WE}$ go low.
(7) D_{OUT} is the same phase as write data of this write cycle.
(8) D_{OUT} is the read-out data of the next address.

Data Retention Characteristics at Ta=-30 to +85°C

Parameter	Symbol	Conditions			min	typ	max	unit
Data Retention Supply Voltage	V_{DR}	$V_{\overline{CE1}}=V_{CC}$ or $V_{\overline{CE2}}=V_{CC}$ V_{IN}=0 to V_{CC}			2.0		5.5	V
Data Retention Supply Current	I_{CCDR}	$V_{\overline{CE1}}=V_{CC}$ or $V_{\overline{CE2}}=V_{CC}$ V_{CC}=3.0V V_{IN}=0 to V_{CC}	LC3518B -10/12/15	Ta=60°C			4.0	uA
				Ta=85°C			20	uA
			LC3518BL -10/12/15	Ta=25°C			0.2	uA
				Ta=60°C			1.0	uA
$\overline{CE}$ Setup Time	t_{CDR}				0			us
$\overline{CE}$ Hold Time	t_R				t_{RC} Note(1)			us

Note) (1) t_{RC}=Read cycle time.