

PCMF2DFN1; PCMF3DFN1

Common-mode EMI filter for differential channels with integrated ESD protection

Rev. 2 — 28 April 2014

Product data sheet

1. Product profile

1.1 General description

The devices are common-mode ElectroMagnetic Interference (EMI) filters with integrated ElectroStatic Discharge (ESD) protection for two and three differential channels. The devices are designed to provide low insertion loss for differential high-speed signals on each channel while unwanted common-mode signals are attenuated.

Each differential channel incorporates two signal lines that are coupled by integrated coils. Diodes provide protection to downstream components from ESD voltages up to ± 15 kV on each signal line.

Table 1. Product overview

Type number	Number of channels	Package		
		Name	Version	
PCMF2DFN1	2	DFN2520-9	SOT1333-1	XSON9
PCMF3DFN1	3	DFN4020-14	SOT1334-1	XSON14

1.2 Features and benefits

- Two and three differential channels common-mode EMI filter with integrated ESD protection
- Superior common-mode suppression over a wide frequency range
- ESD protection up to ± 15 kV contact discharge according to IEC 61000-4-2
- Maximum package height: 0.5 mm

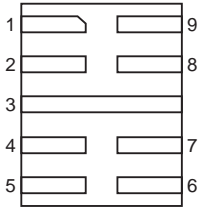
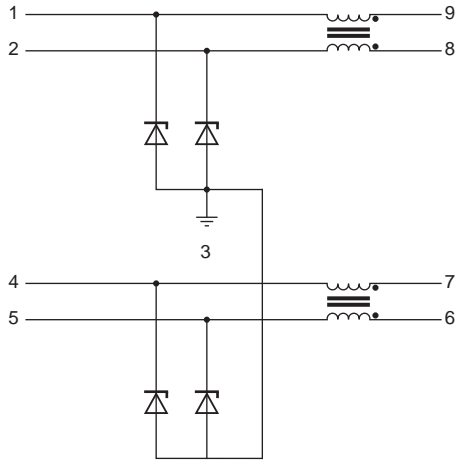
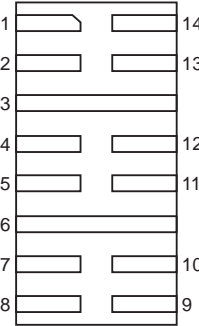
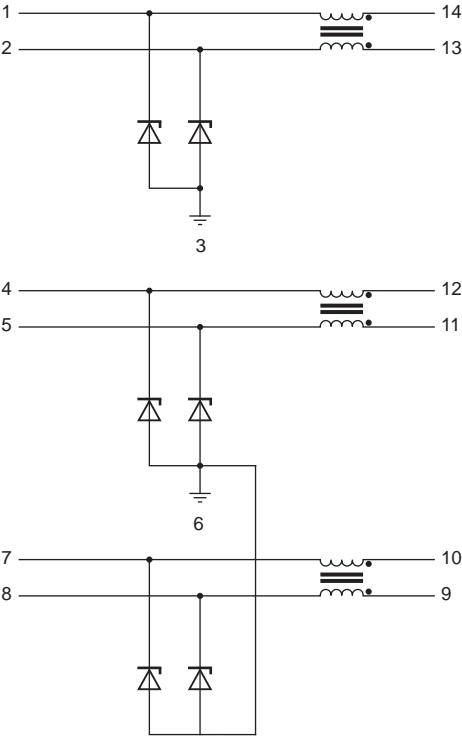
1.3 Applications

- Smartphone, cellular and cordless phone
- MIPI D-PHY as used in Camera Serial Interface (CSI) and Display Serial Interface (DSI)
- General-purpose EMI and Radio-Frequency Interference (RFI) filter and downstream ESD protection
- Tablet PC and Mobile Internet Device (MID)
- High-Definition Multimedia Interface (HDMI)



2. Pinning information

Table 2. Pinning

Pin	Symbol	Description	Simplified outline	Graphic symbol
PCMF2DFN1 (SOT1333-1)				
1	CH1_IN+	input channel 1	 <p>Transparent top view DFN2520-9</p>	 <p>aaa-007385</p>
2	CH1_IN-	input channel 1		
3	GND	ground		
4	CH2_IN+	input channel 2		
5	CH2_IN-	input channel 2		
6	CH2_OUT-	output channel 2		
7	CH2_OUT+	output channel 2		
8	CH1_OUT-	output channel 1		
9	CH1_OUT+	output channel 1		
PCMF3DFN1 (SOT1334-1)				
1	CH1_IN+	input channel 1	 <p>Transparent top view DFN4020-14</p>	 <p>aaa-007384</p>
2	CH1_IN-	input channel 1		
3	GND_1	ground 1		
4	CH2_IN+	input channel 2		
5	CH2_IN-	input channel 2		
6	GND_2	ground 2		
7	CH3_IN+	input channel 3		
8	CH3_IN-	input channel 3		
9	CH3_OUT-	output channel 3		
10	CH3_OUT+	output channel 3		
11	CH2_OUT-	output channel 2		
12	CH2_OUT+	output channel 2		
13	CH1_OUT-	output channel 1		
14	CH1_OUT+	output channel 1		

3. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
PCMF2DFN1	DFN2520-9	plastic extremely thin small outline package; no leads; 9 terminals; body 2 × 2.5 × 0.5 mm	SOT1333-1
PCMF3DFN1	DFN4020-14	plastic extremely thin small outline package; no leads; 14 terminals; body 2 × 4 × 0.5 mm	SOT1334-1

4. Marking

Table 4. Marking codes

Type number	Marking code
PCMF2DFN1	MP1
PCMF3DFN1	CMFMP1

5. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_I	input voltage		-0.5	5	V
V_{ESD}	electrostatic discharge voltage	IEC 61000-4-2, level 4; all input pins to ground			
		contact discharge	-15	15	kV
		air discharge	-15	15	kV
		IEC 61000-4-2, level 4; all output pins to ground			
		contact discharge	-2	2	kV
		air discharge	-2	2	kV
T_{stg}	storage temperature		-55	+125	°C
T_{amb}	ambient temperature		-40	+85	°C

6. Characteristics

6.1 Channel characteristics

Table 6. Channel characteristics

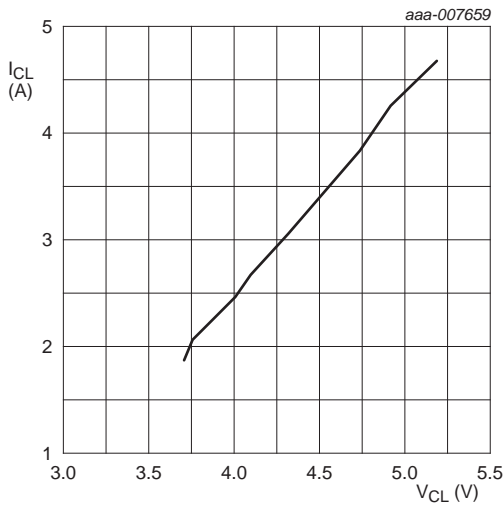
$T_{amb} = 25\text{ }^{\circ}\text{C}$ unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{s(ch)}$	channel series resistance	single line; input to output	-	5	-	Ω
C_d	diode capacitance	$f = 1\text{ MHz}$; $V_I = 2.5\text{ V}$ [1]	-	0.6	0.75	pF
I_{RM}	reverse leakage current	per line; $V_I = 5\text{ V}$	-	-	100	nA
V_{BR}	breakdown voltage	$I_R = 10\text{ mA}$	6	-	9	V
V_F	forward voltage	$I_F = 10\text{ mA}$	0.6	-	1.1	V
R_{dyn}	dynamic resistance	TLP [2]				
		positive transient	-	0.6	-	Ω
		negative transient	-	0.6	-	Ω
		surge [3]				
		positive transient	-	0.6	-	Ω
		negative transient	-	0.6	-	Ω
V_{CL}	clamping voltage	positive transient; $I_{PP} = 4\text{ A}$ [3]	-	4.8	-	V
		negative transient; $I_{PP} = -5\text{ A}$ [3]	-	-3.6	-	V
		TLP; $I_{CL} = 8\text{ A}$	-	8	-	V
		TLP; $I_{CL} = 12\text{ A}$	-	10.5	-	V
		TLP; $I_{CL} = 16\text{ A}$	-	13.4	-	V
		TLP; $I_{CL} = -8\text{ A}$	-	-6	-	V
		TLP; $I_{CL} = -12\text{ A}$	-	-8.4	-	V
		TLP; $I_{CL} = -16\text{ A}$	-	-10.7	-	V

[1] This parameter is guaranteed by design.

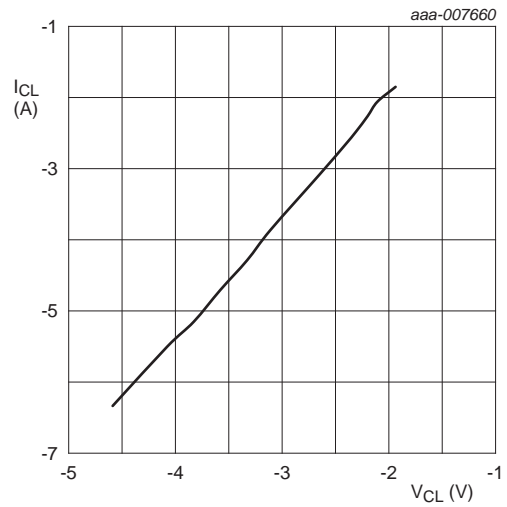
[2] 100 ns Transmission Line Pulse (TLP); 50 Ω ; pulser at 70 to 90 ns.

[3] According to IEC 61000-4-5 (8/20 μs).



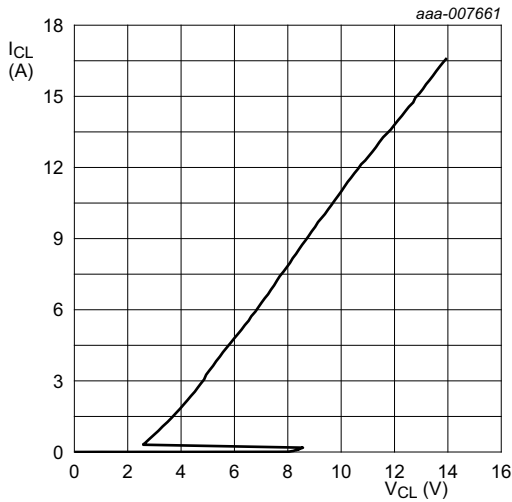
IEC 61000-4-5; $t_p = 8/20 \mu s$; positive pulse

Fig 1. Dynamic resistance with positive clamping; typical values



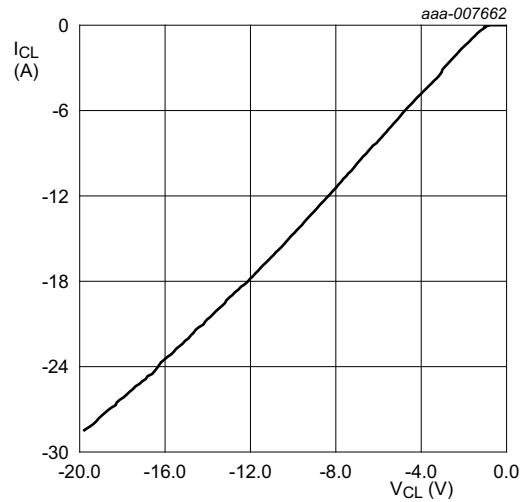
IEC 61000-4-5; $t_p = 8/20 \mu s$; negative pulse

Fig 2. Dynamic resistance with negative clamping; typical values



$t_p = 100 ns$; Transmission Line Pulse (TLP)

Fig 3. Dynamic resistance with positive clamping; typical values



$t_p = 100 ns$; Transmission Line Pulse (TLP)

Fig 4. Dynamic resistance with negative clamping; typical values

The device uses an advanced clamping structure showing a negative dynamic resistance. This snap-back behavior strongly reduces the clamping voltage to the system behind the ESD protection during an ESD event. Do not connect unlimited DC current sources to the data lines to avoid keeping the ESD protection device in snap-back state after exceeding breakdown voltage (due to an ESD pulse for instance).

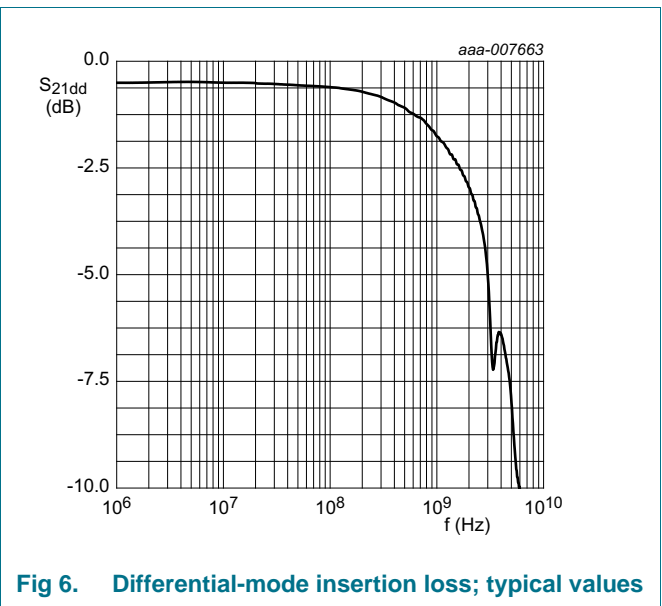
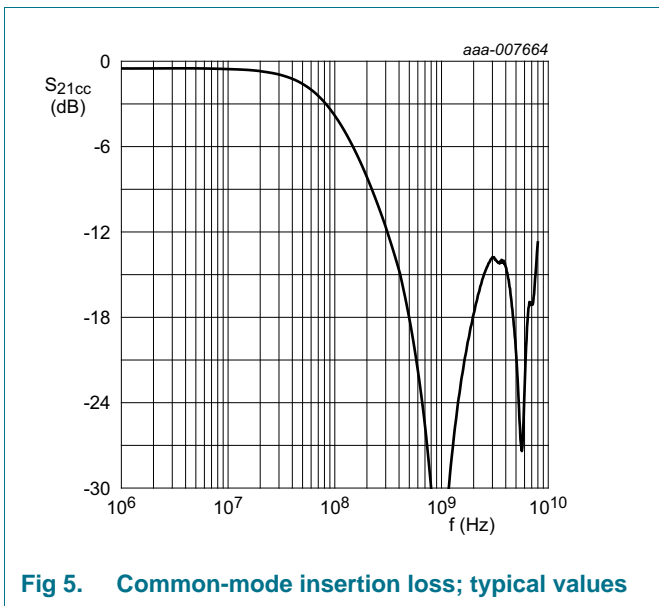
6.2 Frequency characteristics

Table 7. Frequency characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Common mode: S_{21cc}						
α_{il}	insertion loss		[1]			
		$f = 400 \text{ MHz}$	-	15	-	dB
		$f = 800 \text{ MHz}$	-	30	-	dB
		$f = 5 \text{ GHz}$	-	21	-	dB
Differential mode: S_{21dd}						
α_{il}	insertion loss	$f = 1 \text{ MHz}$	[1]	0.6	-	dB
f_{-3dB}	cut-off frequency		[1][2]	2.2	-	GHz

[1] Measured with 4-port network analyzer; $R_{gen} = 50 \Omega$; $R_L = 50 \Omega$.

[2] Normalized to attenuation at 1 MHz.



7. Application information

7.1 Application diagram

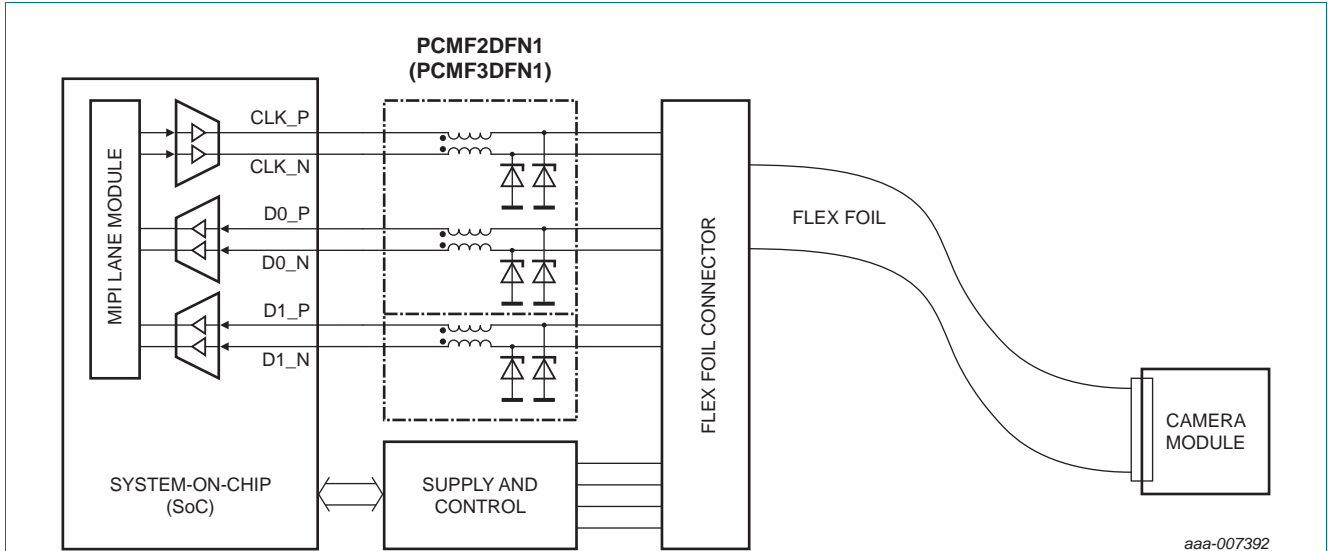


Fig 7. Application diagram for MIPI D-PHY CSI

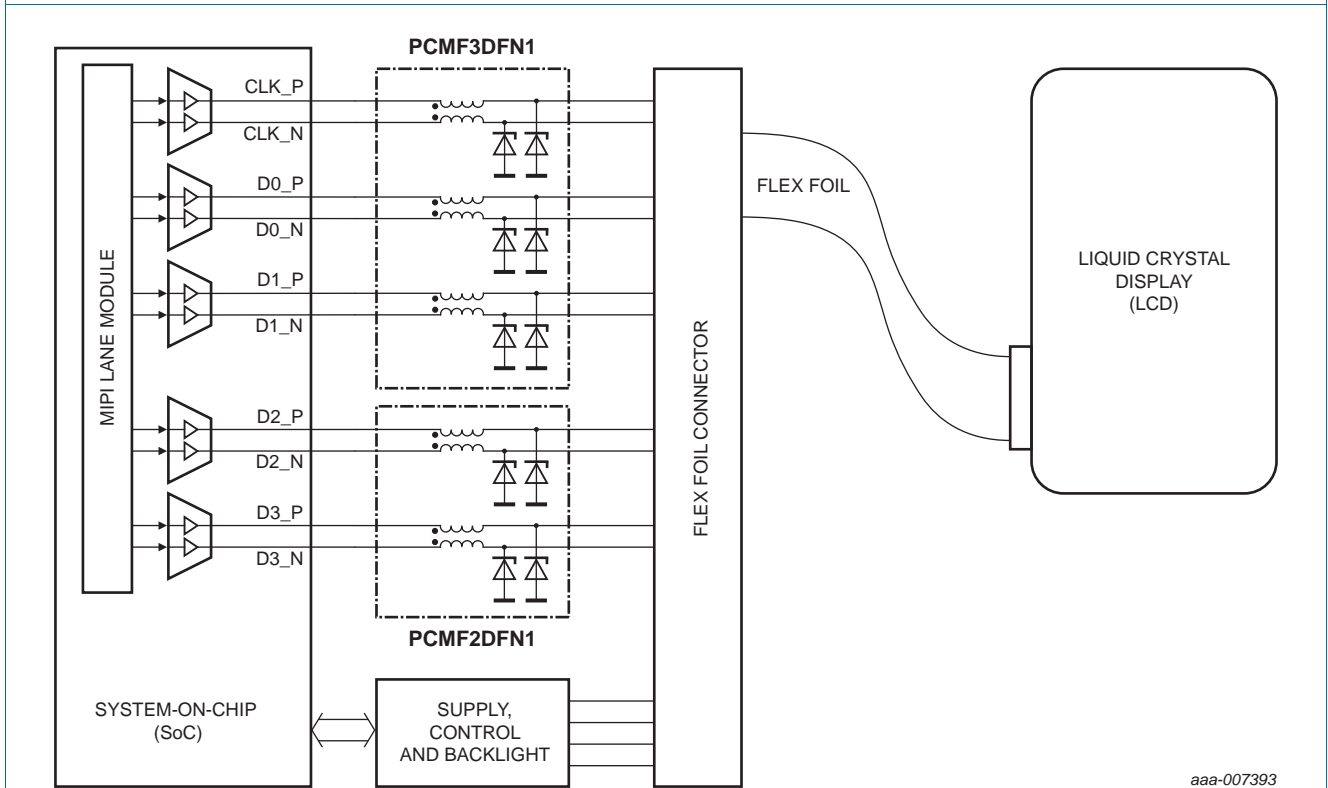
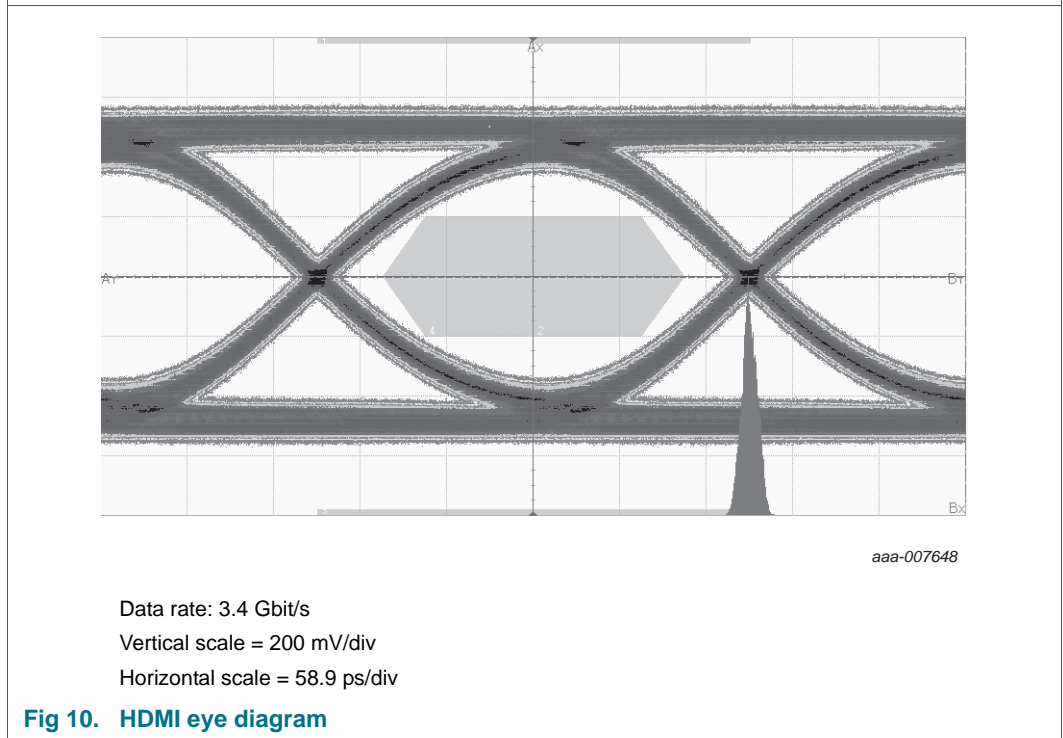
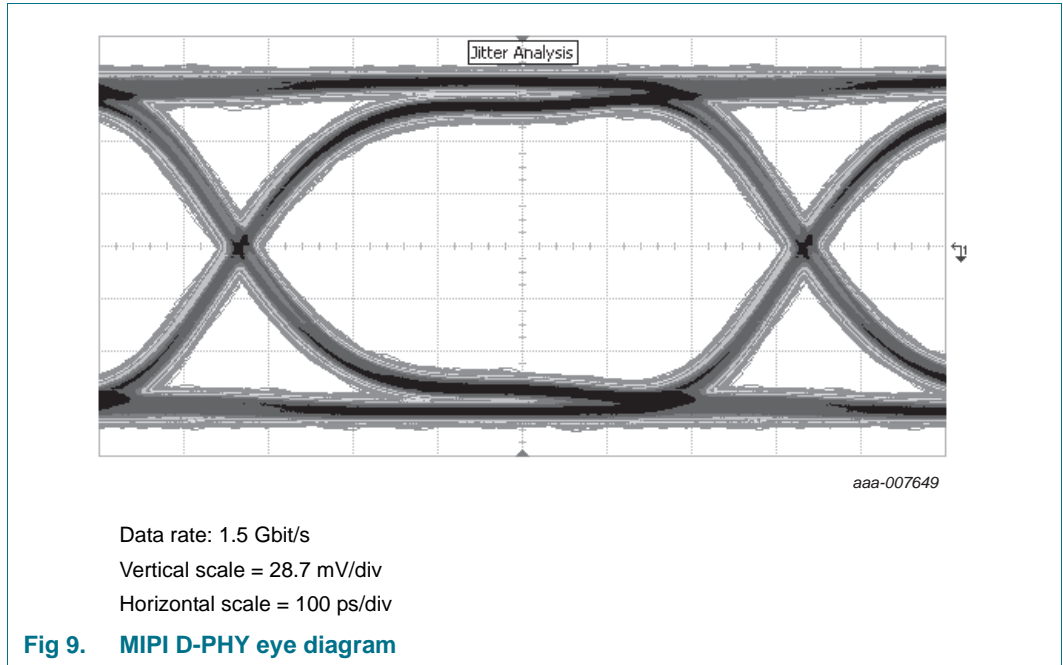


Fig 8. Application diagram for MIPI D-PHY DSI

7.2 Eye diagram



8. Package outline

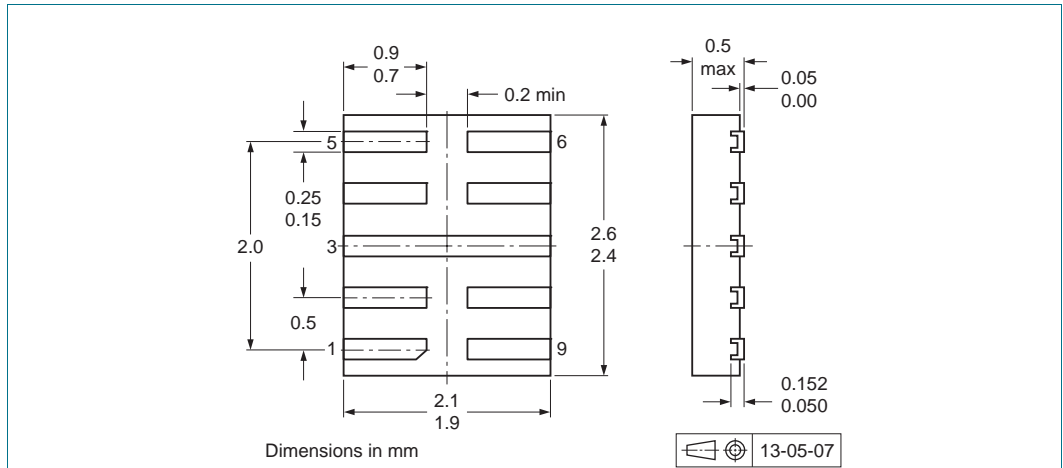


Fig 11. Package outline DFN2520-9 (SOT1333-1)

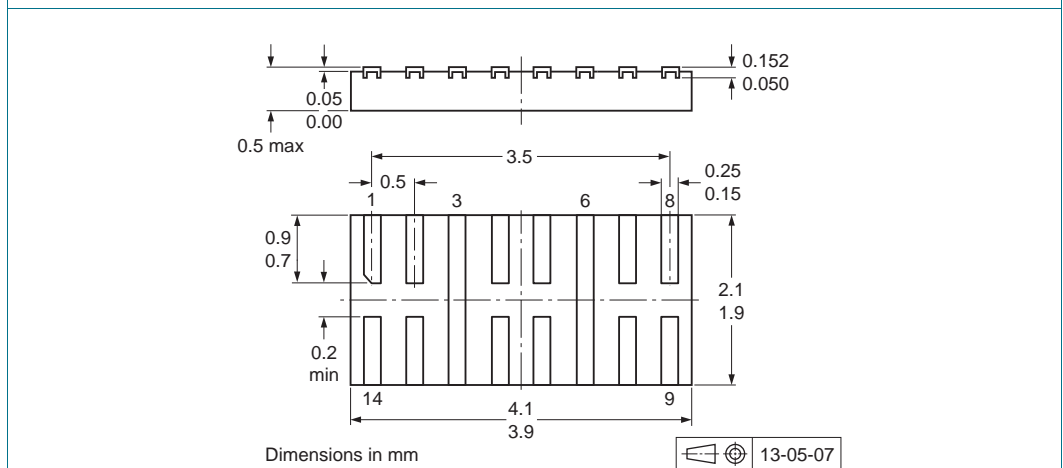


Fig 12. Package outline DFN4020-14 (SOT1334-1)

9. Soldering

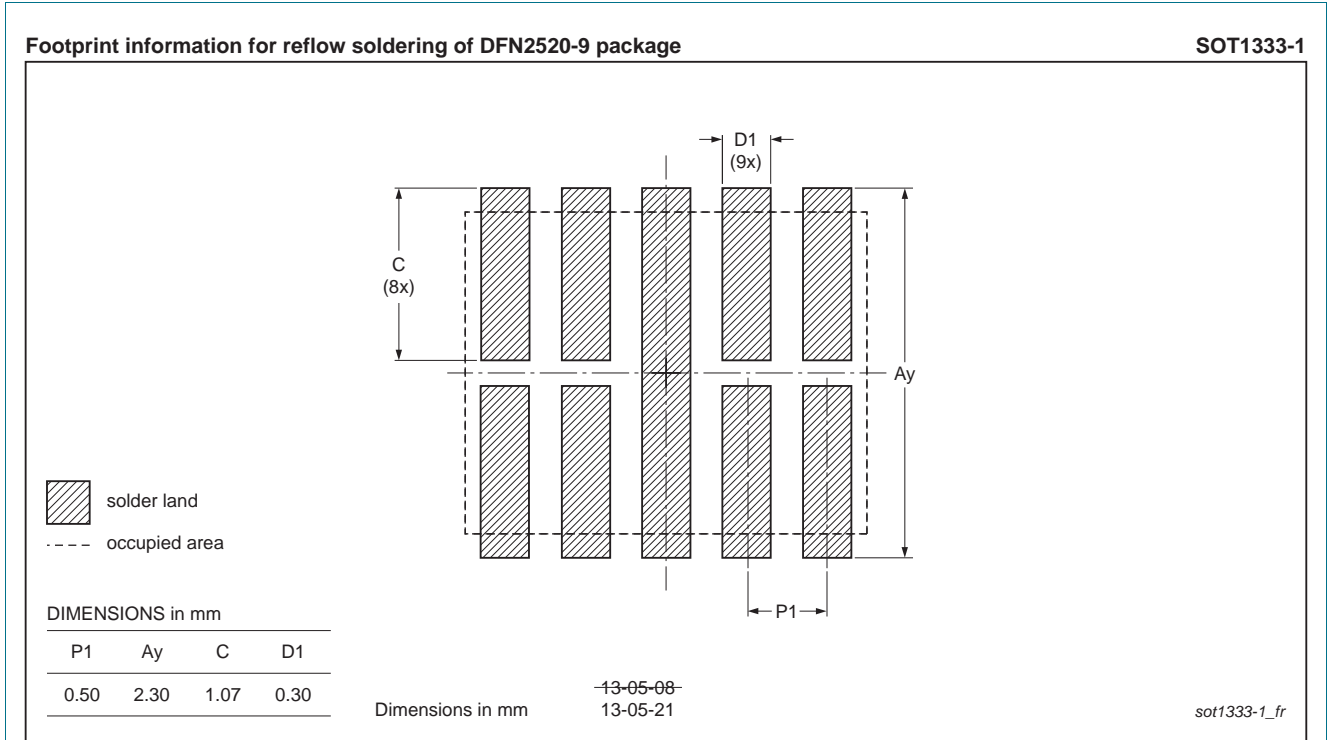


Fig 13. Reflow soldering footprint DFN2520-9 (SOT1333-1)

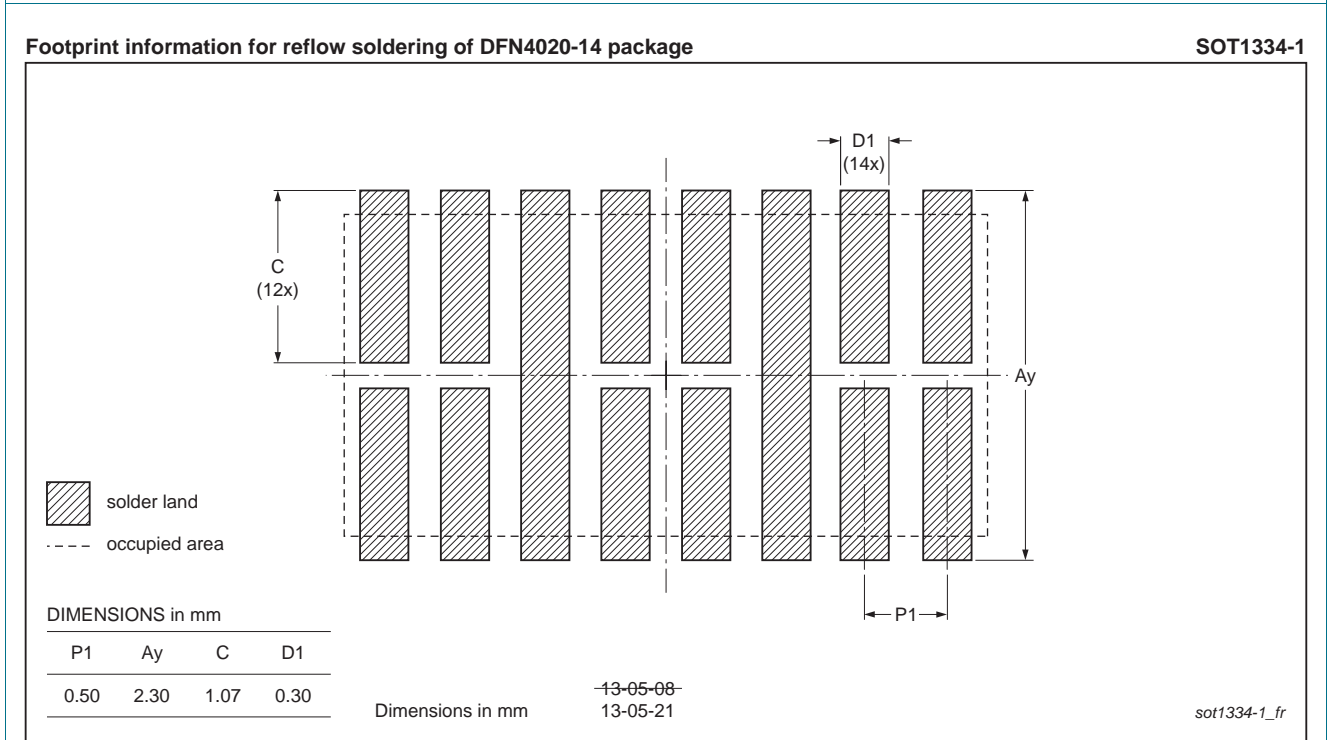


Fig 14. Reflow soldering footprint DFN4020-14 (SOT1334-1)

10. Revision history

Table 8. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
PCMF2DFN1_PCMF3DFN1 v.2	20140428	Product data sheet	-	PCMF2DFN1_PCMF3DFN1 v.1
Modification:	• Surge rating adapted			
PCMF2DFN1_PCMF3DFN1 v.1	20130606	Product data sheet	-	-

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Document status ^{[1][2]}	Product status ^[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
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[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

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