SH69P48A

OTP 4K 4-bit Micro-controller with 10-bit SAR A/D Converter

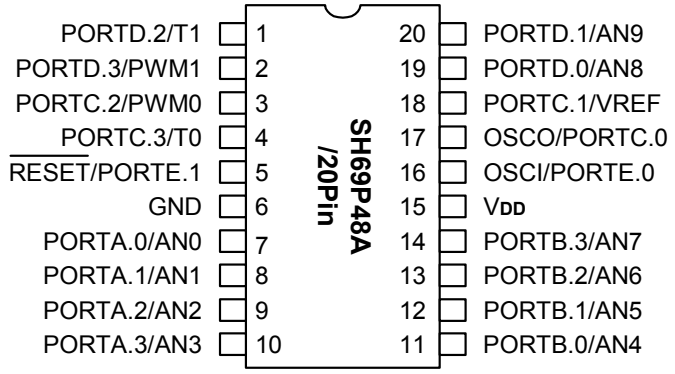
Features

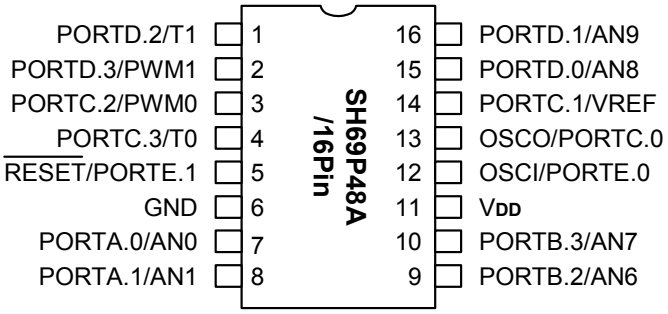
- SH6610D-based single-chip 4-bit micro-controller with 10-bit SAR A/D converter
- OTPROM: 4K X 16bits
- RAM: 253 X 4bits
  - 61 System control registers
  - 192 Data memory
- Operation voltage:
  - **fosc** = 30kHz - 4MHz, V_{DD} = 2.4V - 5.5V
  - **fosc** = 4MHz - 10MHz, V_{DD} = 4.5V - 5.5V
- 17 CMOS bi-directional I/O ports plus 1 CMOS open drain output port (PORTE.1)
- 8-level stack (including interrupts)
- Two 8-bit auto re-loaded timer/counter
  One can switch to external clock source
- Warm-up timer
- Powerful interrupt sources:
  - A/D interrupt
  - Internal interrupt (Timer1, Timer0)
  - External interrupts: PORTB/D (Falling edge)
- Oscillator (code option)
  - Crystal oscillator: 32.768kHz, 400kHz - 10MHz
  - Ceramic resonator: 400kHz - 10MHz
  - External RC oscillator: 400kHz - 10MHz
  - Internal RC oscillator: 4MHz ± 5%
  - External clock: 30kHz - 10MHz
- Instruction cycle time (4/**fosc**)
- Two low power operation modes: HALT and STOP
- Reset
  - Built-in watchdog timer (code option)
  - Built-in power-on reset (POR)
  - Built-in low voltage reset (LVR)
- Two-level low voltage reset (LVR) (code option)
- 10 channels 10-bit resolution analog/digital converter (ADC)
- Read ROM table function
- 2 channels (8 + 2) bits PWM output
- OTP type/code protection
- 20-pin DIP/SOP, 16-pin SOP package

General Description

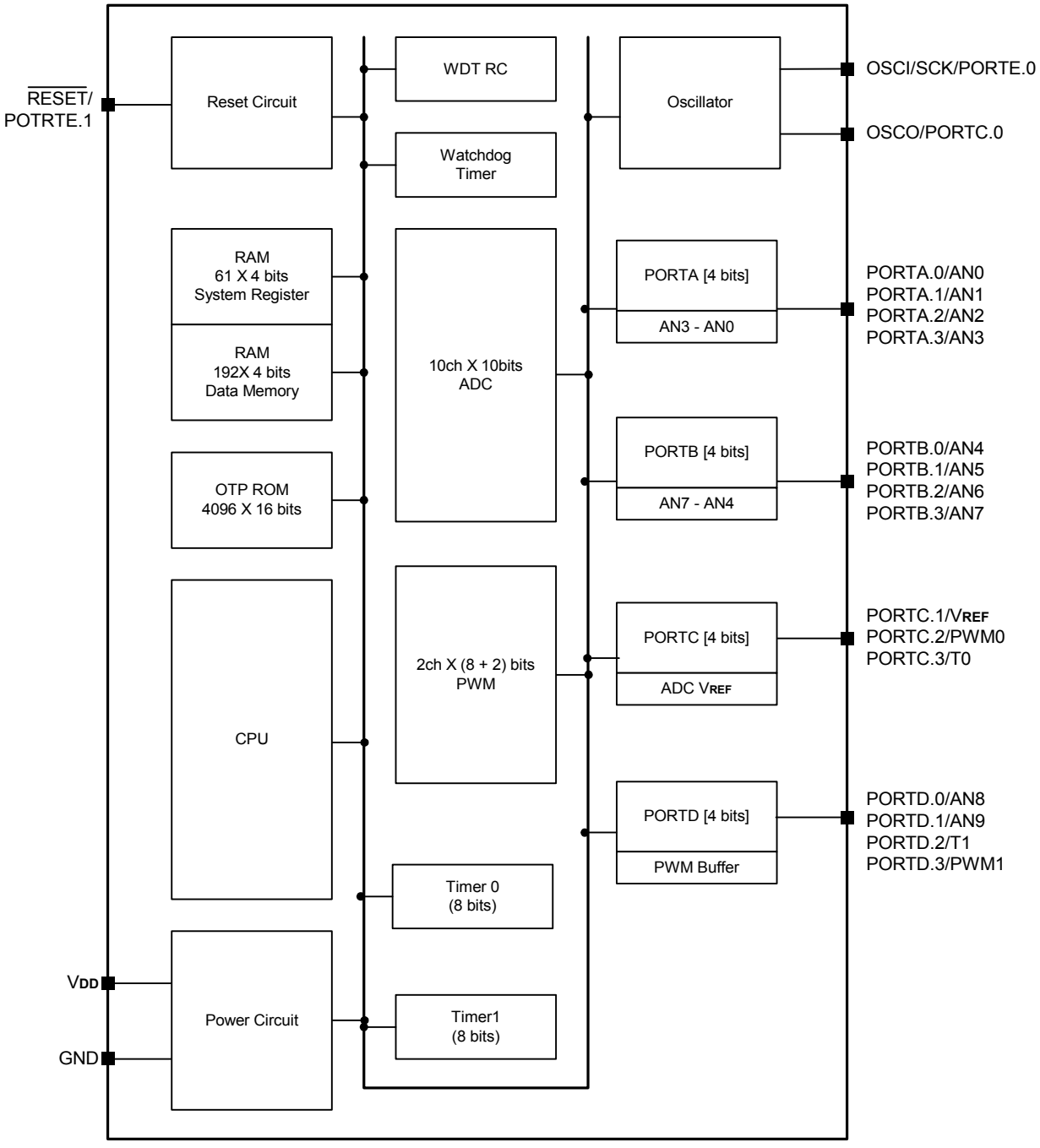
SH69P48A is a single-chip 4-bit micro-controller, that integrates a SH6610D CPU core, 253 nibbles of RAM, 4K words of OTP ROM, two 8-bit timer/counter, 10 channels 10-bit ADC, 2 channels (8 + 2) bits high speed PWM output, on-chip oscillator clock circuitry, on-chip watchdog timer, low voltage reset function and support power saving modes to reduce power consumption. The SH69P48A is ideal for charger applications.

Pin Configuration





Block Diagram



Pin Descriptions:

Pin No.		Designation	I/O	Description
20 pin	16 pin			
1	1	PORTD.2 - /T1	I/O I I	Bit programmable bi-directional I/O port Vector port interrupt. (falling edge active) Shared with Timer1 Input Capture
2	2	PORTD.3 - /PWM1	I/O I O	Bit programmable bi-directional I/O port Vector port interrupt. (falling edge active) Shared with PWM1 output
3	3	PORTC.2 /PWM0	I/O O	Bit programmable bi-directional I/O port Shared with PWM0 output
4	4	PORTC.3 /T0	I/O I	Bit programmable bi-directional I/O port Shared with Timer0 external clock input
5	5	$\overline{\text{RESET}}$ /PORTE.1	I O	Reset pin input, (low active) Open drain output port (selected by code option)
6	6	GND	P	Ground pin
7	7	PORTA.0 /AN0	I/O I	Bit programmable bi-directional I/O port Shared with ADC input channel AN0
8	8	PORTA.1 /AN1	I/O I	Bit programmable bi-directional I/O port Shared with ADC input channel AN1
9	-	PORTA.2 /AN2	I/O I	Bit programmable bi-directional I/O port Shared with ADC input channel AN2
10	-	PORTA.3 /AN3	I/O I	Bit programmable bi-directional I/O port Shared with ADC input channel AN3
11	-	PORTB.0 - /AN4	I/O I I	Bit programmable bi-directional I/O port Vector port interrupt. (falling edge active) Shared with ADC input channel AN4
12	-	PORTB.1 - /AN5	I/O I I	Bit programmable bi-directional I/O port Vector port interrupt. (falling edge active) Shared with ADC input channel AN5
13	9	PORTB.2 - /AN6	I/O I I	Bit programmable bi-directional I/O port Vector port interrupt. (falling edge active) Shared with ADC input channel AN6
14	10	PORTB.3 - /AN7	I/O I I	Bit programmable bi-directional I/O port Vector port interrupt. (falling edge active) Shared with ADC input channel AN7
15	11	V_{DD}	P	Power supply pin
16	12	OSCI /PORTE.0	I I/O	Oscillator input pin, connect to crystal/ceramic oscillator or external resistor of external RC oscillator. Bi-directional I/O port in the internal RC mode
17	13	OSCO /PORTC.0	O I/O	Oscillator output pin, connect to crystal/ceramic oscillator. Bi-directional I/O port in the RC oscillator mode

Pin Descriptions: (continued)

Pin No.		Designation	I/O	Description
20 pin	16 pin			
18	14	PORTC.1 /V_{REF}	I/O I	Bit programmable bi-directional I/O port Shared with external ADC V_{REF} input
19	15	PORTD.0 - /AN8	I/O I I	Bit programmable bi-directional I/O port Vector port interrupt (falling edge active) Shared with ADC input channel AN8
20	16	PORTD.1 - /AN9	I/O I I	Bit programmable bi-directional I/O port Vector port interrupt (falling edge active) Shared with ADC input channel AN9

OTP Programming Pin Description (OTP Program Mode)

Pin No.		Symbol	I/O	Shared by	Description
20 pin	16 pin				
15	11	V_{DD}	P	V_{DD}	Programming power supply (+5.5V)
5	5	V_{PP}	P	$\overline{\text{RESET}}$	Programming high voltage power supply (+11V)
6	6	GND	P	GND	Ground
16	12	SCK	I	OSCI/PORTE.0	Programming clock input pin
7	7	SDA	I/O	PORTA.0/AN0	Programming data pin

Functional Description

1. CPU

The CPU contains the following functional blocks: Program Counter (PC), Arithmetic Logic Unit (ALU), Carry Flag (CY), Accumulator, Table Branch Register, Data Pointer (INX, DPH, DPM, and DPL) and Stacks.

1.1. PC

The PC is used for ROM addressing consisting of 12-bit:
Page Register (PC11), and Ripple Carry Counter (PC10, PC9, PC8, PC7, PC6, PC5, PC4, PC3, PC2, PC1, PC0).
The program counter is loaded with data corresponding to each instruction. The unconditional jump instruction (JMP) can be set at 1-bit page register for higher than 2K.
The program counter cans only 4K program ROM address. (Refer to the ROM description).

1.2. ALU and CY

The ALU performs arithmetic and logic operations. The ALU provides the following functions:
Binary addition/subtraction (ADC, SBC, ADD, SUB, ADI, SBI)
Decimal adjustments for addition/subtraction (DAA, DAS)
Logic operations (AND, EOR, OR, ANDIM, EORIM, ORIM)
Decisions (BA0, BA1, BA2, BA3, BAZ, BNZ, BC, BNC)
Logic Shift (SHR)
The Carry Flag (CY) holds the ALU overflow that the arithmetic operation generates. During an interrupt service or CALL instruction, the carry flag is pushed into the stack and recovered from the stack by the RTNI instruction. It is unaffected by the RTNW instruction.

1.3. Accumulator (AC)

The accumulator is a 4-bit register holding the results of the arithmetic logic unit. In conjunction with the ALU, data is transferred between the accumulator and system register, or data memory can be performed.

1.4. Table Branch Register (TBR)

Table Data can be stored in program memory and can be referenced by using Table Branch (TJMP) and Return Constant (RTNW) instructions. The TBR and AC are placed by an offset address in program ROM. TJMP instruction branch into address ((PC11 - PC8) X (2^8) + (TBR, AC)). The address is determined by RTNW to return look-up value into (TBR, AC). ROM code bit7-bit4 is placed into TBR and bit3-bit0 into AC.

1.5. Data Pointer

The Data Pointer can indirectly address data memory. Pointer address is located in register DPH (3-bit), DPM (3-bit) and DPL (4-bit). The addressing range can have 3FFH locations. Pseudo index address (INX) is used to read or write Data memory, then RAM address bit9 - bit0 which comes from DPH, DPM and DPL.

1.6. Stack

The stack is a group of registers used to save the contents of CY & PC (11-0) sequentially with each subroutine call or interrupt. The MSB is saved for CY and it is organized into 13 bits X 8 levels. The stack is operated on a first-in, last-out basis and returned sequentially to the PC with the return instructions (RTNI/RTNW).

Note:

The stack nesting includes both subroutine calls and interrupts requests. The maximum allowed for subroutine calls and interrupts are 8 levels. If the number of calls and interrupt requests exceeds 8, then the bottom of stack will be shifted out, that program execution may enter an abnormal state.

2. RAM

Built-in RAM contains general-purpose data memory and system register. Because of its static nature, the RAM can keep data after the CPU enters STOP or HALT.

2.1. RAM Addressing

Data memory and system register can be accessed in one instruction by direct addressing. The following is the memory allocation map:
System register and I/O: $000 - $02F, $380 - $38C
Data memory: $030 - $0EF

2.2. Configuration of System Register:

Address	Bit 3	Bit 2	Bit 1	Bit 0	R/W	Remarks
$00	IEAD	IET0	IET1	IEP	R/W	Interrupt enable flags
$01	IRQAD	IRQT0	IRQT1	IRQP	R/W	Interrupt request flags
$02	T0S	T0M.2	T0M.1	T0M.0	R/W	Bit2 - 0: Timer0 mode register Bit3: T0 signal source
$03	T1E	T1M.2	T1M.1	T1M.0	R/W	Bit2 - 0: Timer1 mode register Bit3: T1 external signal edge select
$04	T0L.3	T0L.2	T0L.1	T0L.0	R/W	Timer0 load/counter register (low nibble)
$05	T0H.3	T0H.2	T0H.1	T0H.0	R/W	Timer0 load/counter register (high nibble)
$06	T1L.3	T1L.2	T1L.1	T1L.0	R/W	Timer1 load/counter register (low nibble)

2.2. Configuration of System Register: (continued)

Address	Bit 3	Bit 2	Bit 1	Bit 0	R/W	Remarks
$07	T1H.3	T1H.2	T1H.2	T1H.0	R/W	Timer1 load/counter register (high nibble)
$08	PA.3	PA.2	PA.1	PA.0	R/W	PORTA In 16 pin mode, bit2 - 3 are reserved; always keep it to “0” in the user’s program Refer to I/O notice
$09	PB.3	PB.2	PB.1	PB.0	R/W	PORTB In 16 pin mode, bit0 - 1 are reserved, always keep it to “0” in the user’s program Refer to I/O notice
$0A	PC.3	PC.2	PC.1	PC.0	R/W	PORTC
$0B	PD.3	PD.2	PD.1	PD.0	R/W	PORTD
$0C	-	-	PE.1	PE.0	R/W	PORTE
$0D	-	-	-	-	-	Reserved
$0E	TBR.3	TBR.2	TBR.1	TBR.0	R/W	Table branch register
$0F	INX.3	INX.2	INX.1	INX.0	R/W	Pseudo index register
$10	DPL.3	DPL.2	DPL.1	DPL.0	R/W	Data pointer for INX low nibble
$11	-	DPM.2	DPM.1	DPM.0	R/W	Data pointer for INX middle nibble
$12	-	DPH.2	DPH.1	DPH.0	R/W	Data pointer for INX high nibble
$13	T1GO	DEC	-	TM1S0	R/W	Bit0: Set Timer1 mode Bit2: Select directive edge active enable Bit3: Set Timer1 function start
$14	VREFS	-	-	ADCON	R/W	Bit0: Set ADC module operate Bit3: Select internal/external reference voltage
$15	$\overline{\text{GO/DONE}}$	TADC1	TADC0	ADCS	R/W	Bit0: Set ADC conversion time Bit2, Bit1: Select ADC clock period Bit3: ADC status flag
$16	ACR3	ACR2	ACR1	ACR0	R/W	Bit3 - 0: ADC port configuration control
$17	CH3	CH2	CH1	CH0	R/W	Bit3 - 0: Select ADC channel
$18	PACR.3	PACR.2	PACR.1	PACR.0	R/W	PORTA input/output control In 16 pin mode, bit2 - 3 are reserved, always keep it to “1” in the user’s program Refer to I/O notice
$19	PBCR.3	PBCR.2	PBCR.1	PBCR.0	R/W	PORTB input/output control In 16 pin mode, bit0 - 1 are reserved, always keep it to “1” in the user’s program Refer to I/O notice

2.2. Configuration of System Register: (continued)

Address	Bit 3	Bit 2	Bit 1	Bit 0	R/W	Remarks
$1A	PCCR.3	PCCR.2	PCCR.1	PCCR.0	R/W	PORTC input/output control
$1B	PDCR.3	PDCR.2	PDCR.1	PDCR.0	R/W	PORTD input/output control
$1C	-	-	-	PECR.0	R/W	PORTE input/output control
$1D	-	-	-	-	-	Reserved
$1E	- WDT	WDT.2 -	WDT.1 -	WDT.0 -	R/W R	Bit2 - 0: Watchdog timer control Bit3: Watchdog timer overflow flag (Read only)
$1F	-	-	-	-	-	Reserved
$20	PWM0S	T0CK1	T0CK0	PWM0_EN	R/W	Bit0: PWM0 output enable Bit2, Bit1: Select PWM0 clock Bit3: Set PWM0 output mode of duty cycle
$21	PWM1S	T1CK1	T1CK0	PWM1_EN	R/W	Bit0: PWM1 output enable Bit2, Bit1: Select PWM1 clock Bit3: Set PWM1 output mode of duty cycle
$22	PP0.3	PP0.2	PP0.1	PP0.0	R/W	PWM0 period low nibble
$23	PP0.7	PP0.6	PP0.5	PP0.4	R/W	PWM0 period high nibble
$24	-	-	PDF0.1	PDF0.0	R/W	PWM0 duty fine tune nibble
$25	PD0.3	PD0.2	PD0.1	PD0.0	R/W	PWM0 duty low nibble
$26	PD0.7	PD0.6	PD0.5	PD0.4	R/W	PWM0 duty high nibble
$27	PP1.3	PP1.2	PP1.1	PP1.0	R/W	PWM1 period low nibble
$28	PP1.7	PP1.6	PP1.5	PP1.4	R/W	PWM1 period high nibble
$29	-	-	PDF1.1	PDF1.0	R/W	PWM1 duty fine tune nibble
$2A	PD1.3	PD1.2	PD1.1	PD1.0	R/W	PWM1 duty low nibble
$2B	PD1.7	PD1.6	PD1.5	PD1.4	R/W	PWM1 duty high nibble
$2C	-	-	-	-	-	Reserved
$2D	-	-	A1	A0	R	ADC data low nibble (Read only)
$2E	A5	A4	A3	A2	R	ADC data medium nibble (Read only)
$2F	A9	A8	A7	A6	R	ADC data high nibble (Read only)
$380	RDT.3	RDT.2	RDT.1	RDT.0	R/W	ROM data table address/data register
$381	RDT.7	RDT.6	RDT.5	RDT.4	R/W	ROM data table address/data register
$382	RDT.11	RDT.10	RDT.9	RDT.8	R/W	ROM data table address/data register
$383	RDT.15	RDT.14	RDT.13	RDT.12	R/W	ROM data table address/data register
$384	PDIEN.3	PDIEN.2	PDIEN.1	PDIEN.0	R/W	PORTD interrupt enable flags
$385	PDIF.3	PDIF.2	PDIF.1	PDIF.0	R/W	PORTD interrupt request flags
$386	PBIEN.3	PBIEN.2	PBIEN.1	PBIEN.0	R/W	PORTB interrupt enable flags
$387	PBIF.3	PBIF.2	PBIF.1	PBIF.0	R/W	PORTB interrupt request flags
$388	PPACR.3	PPACR.2	PPACR.1	PPACR.0	R/W	PORTA pull-high control
$389	PPBCR.3	PPBCR.2	PPBCR.1	PPBCR.0	R/W	PORTB pull-high control
$38A	PPCCR.3	PPCCR.2	PPCCR.1	PPCCR.0	R/W	PORTC pull-high control
$38B	PPDCR.3	PPDCR.2	PPDCR.1	PPDCR.0	R/W	PORTD pull-high control
$38C	-	-	-	PPECR.0	R/W	PORTE pull-high control

3. ROM

The ROM can address 4096 X 16 bits of program area from $0000 to $0FFF.

3.1. Vector Address Area ($000 to $004)

The program is sequentially executed. There is an area address $000 through $004 that is reserved for a special interrupt service routine such as starting vector address

Address	Instruction	Remarks
$000	JMP*	Jump to Reset service routine
$001	JMP*	Jump to ADC interrupt service routine
$002	JMP*	Jump to Timer0 interrupt service routine
$003	JMP*	Jump to Timer1 interrupt service routine
$004	JMP*	Jump to PORTB/D interrupt service routine

*JMP instruction can be replaced by any instruction.

3.2. ROM Data Table

System Register:

Address	Bit 3	Bit 2	Bit 1	Bit 0	R/W	Remarks
$380	RDT.3	RDT.2	RDT.1	RDT.0	R/W	ROM data table address/data register
$381	RDT.7	RDT.6	RDT.5	RDT.4	R/W	ROM data table address/data register
$382	RDT.11	RDT.10	RDT.9	RDT.8	R/W	ROM data table address/data register
$383	RDT.15	RDT.14	RDT.13	RDT.12	R/W	ROM data table address/data register

The RDT register consists of a 12-bit write-only PC address load register (RDT.11 - RDT.0) and a 16-bit read-only ROM table data read-out register (RDT.15 - RDT.0).

To read out the ROM table data, users should write the ROM table address to the RDT register first (high nibble first then low nibble), then, after one instruction, the right data will be put into the RDT register automatically (write the lowest nibble of address into the register will start the data read-out action).

4. Initial State

4.1. System Register State:

Address	Bit 3	Bit 2	Bit 1	Bit 0	Power-On Reset /Pin Reset /Low Voltage Reset	WDT Reset
$00	IEAD	IET0	IET1	IEP	0000	0000
$01	IRQAD	IRQT0	IRQT1	IRQP	0000	0000
$02	T0S	T0M.2	T0M.1	T0M.0	0000	uuuu
$03	T1E	T1M.2	T1M.1	T1M.0	0000	uuuu
$04	T0L.3	T0L.2	T0L.1	T0L.0	xxxx	xxxx
$05	T0H.3	T0H.2	T0H.1	T0H.0	xxxx	xxxx
$06	T1L.3	T1L.2	T1L.1	T1L.0	xxxx	xxxx
$07	T1H.3	T1H.2	T1H.1	T1H.0	xxxx	xxxx
$08	PA.3	PA.2	PA.1	PA.0	0000	0000
$09	PB.3	PB.2	PB.1	PB.0	0000	0000
$0A	PC.3	PC.2	PC.1	PC.0	0000	0000
$0B	PD.3	PD.2	PD.1	PD.0	0000	0000
$0C	-	-	PE.1	PE.0	--10	--10
$0D	-	-	-	-	----	----
$0E	TBR.3	TBR.2	TBR.1	TBR.0	xxxx	uuuu
$0F	INX.3	INX.2	INX.1	INX.0	xxxx	uuuu
$10	DPL.3	DPL.2	DPL.1	DPL.0	xxxx	uuuu
$11	-	DPM.2	DPM.1	DPM.0	-xxx	-uuu
$12	-	DPH.2	DPH.1	DPH.0	-xxx	-uuu
$13	T1GO	DEC	-	TM1S0	00-0	0u-u
$14	VREFS	-	-	ADCON	0—0	u—0
$15	GO/$\overline{\text{DONE}}$	TADC1	TADC0	ADCS	0000	0uuu
$16	ACR3	ACR2	ACR1	ACR0	0000	uuuu
$17	CH3	CH2	CH1	CH0	0000	uuuu
$18	PACR.3	PACR.2	PACR.1	PACR.0	0000	0000
$19	PBCR.3	PBCR.2	PBCR.1	PBCR.0	0000	0000
$1A	PCCR.3	PCCR.2	PCCR.1	PCCR.0	0000	0000
$1B	PDCR.3	PDCR.2	PDCR.1	PDCR.0	0000	0000
$1C	-	-	-	PECR.0	---0	---0
$1D	-	-	-	-	----	----
$1E	WDT	WDT.2	WDT.1	WDT.0	0000	1000
$1F	-	-	-	-	----	----
$20	PWM0S	T0CK1	T0CK0	PWM0_EN	0000	uuu0

Legend: x = unknown, u = unchanged, - = unimplemented read as '0'.

System Register State: (continued)

Address	Bit 3	Bit 2	Bit 1	Bit 0	Power-On Reset /Pin Reset /Low Voltage Reset	WDT Reset
$21	PWM1S	T1CK1	T1CK0	PWM1_EN	0000	uuu0
$22	PP0.3	PP0.2	PP0.1	PP0.0	xxxx	uuuu
$23	PP0.7	PP0.6	PP0.5	PP0.4	xxxx	uuuu
$24	-	-	PDF0.1	PDF0.0	--xx	--uu
$25	PD0.3	PD0.2	PD0.1	PD0.0	xxxx	uuuu
$26	PD0.7	PD0.6	PD0.5	PD0.4	xxxx	uuuu
$27	PP1.3	PP1.2	PP1.1	PP1.0	xxxx	uuuu
$28	PP1.7	PP1.6	PP1.5	PP1.4	xxxx	uuuu
$29	-	-	PDF1.1	PDF1.0	--xx	--uu
$2A	PD1.3	PD1.2	PD1.1	PD1.0	xxxx	uuuu
$2B	PD1.7	PD1.6	PD1.5	PD1.4	xxxx	uuuu
$2C	-	-	-	-	----	----
$2D	-	-	A1	A0	--xx	--uu
$2E	A5	A4	A3	A2	xxxx	uuuu
$2F	A9	A8	A7	A6	xxxx	uuuu
$380	RDT.3	RDT.2	RDT.1	RDT.0	xxxx	uuuu
$381	RDT.7	RDT.6	RDT.5	RDT.4	xxxx	uuuu
$382	RDT.11	RDT.10	RDT.9	RDT.8	xxxx	uuuu
$383	RDT.15	RDT.14	RDT.13	RDT.12	xxxx	uuuu
$384	PDIEN.3	PDIEN.2	PDIEN.1	PDIEN.0	0000	0000
$385	PDIF.3	PDIF.2	PDIF.1	PDIF.0	0000	0000
$386	PBIEN.3	PBIEN.2	PBIEN.1	PBIEN.0	0000	0000
$387	PBIF.3	PBIF.2	PBIF.1	PBIF.0	0000	0000
$388	PPACR.3	PPACR.2	PPACR.1	PPACR.0	0000	0000
$389	PPBCR.3	PPBCR.2	PPBCR.1	PPBCR.0	0000	0000
$38A	PPCCR.3	PPCCR.2	PPCCR.1	PPCCR.0	0000	0000
$38B	PPDCR.3	PPDCR.2	PPDCR.1	PPDCR.0	0000	0000
$38C	-	-	-	PPECR.0	---0	---0

Legend: x = unknown, u = unchanged, - = unimplemented read as '0'.

4.2. Others Initial States:

Others	After any Reset
Program Counter (PC)	$000
CY	Undefined
Accumulator (AC)	Undefined
Data Memory	Undefined

5. System Clock and Oscillator

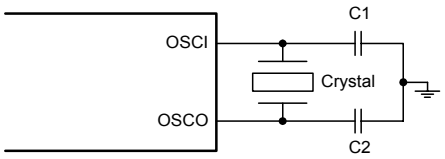
The oscillator generates the basic clock pulses that provide the system clock to supply CPU and on-chip peripherals.
System clock = f**osc**/4

5.1. Instruction Cycle Time:

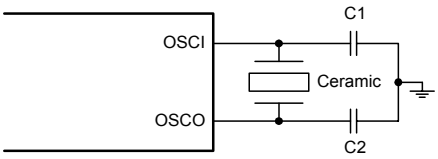
(1) 4/32.768kHz (≈ 122.1μs) for 32.768kHz oscillator.
(2) 4/10MHz (= 0.4μs) for 10MHz oscillator.

5.2. Oscillator Type

(1) Crystal oscillator: 32.768kHz or 400kHz - 10MHz



(2) Ceramic resonator: 400kHz - 10MHz



Capacitor Selection for Oscillator

Ceramic Resonators			Recommend Type	Manufacturer
Frequency	**C1**	**C2**		
455kHz	47 - 100pF	47 - 100pF	ZT 455E	JingBo Electronic Shenzhen
3.58MHz	-	-	ZT 3.58M*	JingBo Electronic Shenzhen
4MHz	-	-	ZT 4M*	JingBo Electronic Shenzhen

*- The specified ceramic resonator has internal built-in load capacity

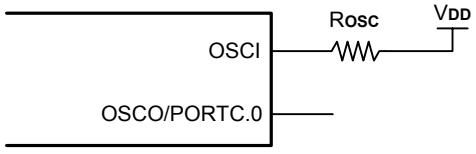
Crystal Oscillator			Recommend Type	Manufacturer
Frequency	**C1**	**C2**		
32.768kHz	5 - 12.5pF	5 - 12.5pF	DT 38 (Φ 3 X 8)	KDS
4MHz	8 - 15pF	8 - 15pF	49S-4.000M-F16E	JingBo Electronic Shenzhen
8MHz	8 - 15pF	8 - 15pF	49S-8.000M-F16E	JingBo Electronic Shenzhen

Notes:

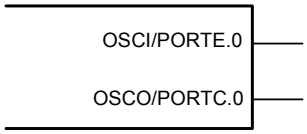
1. **Capacitor values are used for design guidance only!**
2. These capacitors were tested with the crystals listed above for basic start-up and operation. **They are not optimized.**
3. Be careful for the stray capacitance on PCB board, the user should test the performance of the oscillator over the expected
   V**DD** and the temperature range for the application.

Before selecting crystal/ceramic, the user should consult the crystal/ceramic manufacturer for appropriate value of external component to get best performance, visit http://www.sinowealth.com for more recommended manufactures.

(3) RC oscillator: 400kHz - 10MHz

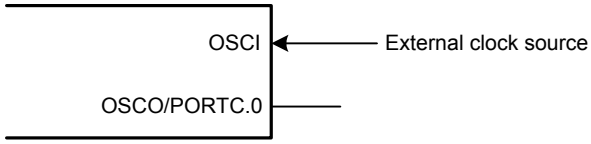


External RC oscillator



Internal RC oscillator (f**osc** = 4MHz ± 5%)

(4) External input clock: 30kHz - 10MHz



Note:

- If the RC oscillator or the external input clock is selected, OSCO pin will be used as the I/O port (PORTC.0).
- If the internal RC oscillator is selected, OSCO pin will be used as the I/O port (PORTC.0), and OSCI pin will be used as the PORTE.0.

6. I/O Ports

- The MCU provides 17 bi-directional I/O ports plus 1 CMOS open drain output port (PORTE.1). The PORT data put in register ($08 - $0C). The PORT control register ($18 - $1C) controls the PORT as input or output. Each I/O port (excluding those open drain output ports) contains a pull-high resistor, which is controlled by the value of the corresponding bit in the port pull-high control register ($388 - $38C), independently.
- When the port is selected as an input port, it can turn on the pull-high resistor by writing “1”, and turn off the pull-high resistor by writing “0”, to the relevant bit in the port pull-high control register ($388 - $38C).
- When the port is selected as an output port, the pull-high resistor will be turned off automatically, regardless the value of the corresponding bit in the port pull-high control register ($388 - $38C).
- When PORTB/D is selected as the digital input direction, it can activate port interrupt by falling edge (if port interrupt is enabled).

System Register $08 - $0C:Port Data Register

Address	Bit 3	Bit 2	Bit 1	Bit 0	R/W	Remarks
$08	PA.3	PA.2	PA.1	PA.0	R/W	PORTA
$09	PB.3	PB.2	PB.1	PB.0	R/W	PORTB
$0A	PC.3	PC.2	PC.1	PC.0	R/W	PORTC
$0B	PD.3	PD.2	PD.1	PD.0	R/W	PORTD
$0C	-	-	PE.1	PE.0	R/W	PORTE

Note:

In 16 pin mode, bit2 - 3 of the $08 RAM and bit0 - 1 of the $09 RAM are reserved; always keep it “0” in the user’s program.

System Register $18 - $1C: Port Control Register

Address	Bit 3	Bit 2	Bit 1	Bit 0	R/W	Remarks
$18	PACR.3	PACR.2	PACR.1	PACR.0	R/W	PORTA input/output control
$19	PBCR.3	PBCR.2	PBCR.1	PBCR.0	R/W	PORTB input/output control
$1A	PCCR.3	PCCR.2	PCCR.1	PCCR.0	R/W	PORTC input/output control
$1B	PDCR.3	PDCR.2	PDCR.1	PDCR.0	R/W	PORTD input/output control
$1C	-	-	-	PECR.0	R/W	PORTE input/output control

Note: In 16 pin mode, bit2 - 3 of the $18 RAM and bit0 - 1 of the $19 RAM are reserved, always keep it “1” in the user’s program.

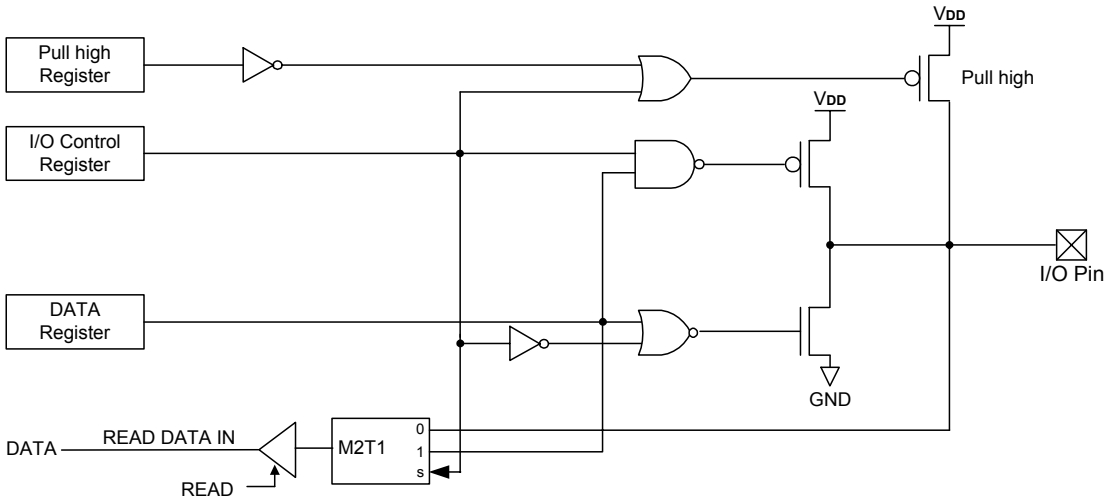
PA (/B/C/D/E) CR.n, (n = 0, 1, 2, 3)
0: Set I/O as an input direction. (Default)
1: Set I/O as an output direction.

System Register $388 - $38C: Port Pull-high Control Register

Address	Bit 3	Bit 2	Bit 1	Bit 0	R/W	Remarks
$388	PPACR.3	PPACR.2	PPACR.1	PPACR.0	R/W	PORTA pull-high control
$389	PPBCR.3	PPBCR.2	PPBCR.1	PPBCR.0	R/W	PORTB pull-high control
$38A	PPCCR.3	PPCCR.2	PPCCR.1	PPCCR.0	R/W	PORTC pull-high control
$38B	PPDCR.3	PPDCR.2	PPDCR.1	PPDCR.0	R/W	PORTD pull-high control
$38C	-	-	-	PPECR.0	R/W	PORTE pull-high control

PPA (/B/C/D/E) CR.n, (n = 0, 1, 2, 3)
0: Disable internal pull-high resistor. (Default)
1: Enable internal pull-high resistor.

Equivalent Circuit for a Single I/O Pin



- In SH69P48A, each output port contains a latch, which can hold the output data. Writing the port data register (PDR) under the output mode can directly transfer data to the corresponding pad.

  All input ports do not have latches, so the external input data should be held externally until the input data is read from outside or reading the port data register (PDR) is read under the input mode.

  When a digital I/O port is selected as an output, the reading of the associated port bit actually represents the value of the output data latch, not the voltage on the pad. When a digital I/O port is selected as an input, the reading of the associated port bit represents the status on the corresponding pad.
- PORTA.0 - 3 can be shared with ADC input channel (AN0 - 3).
- PORTB.0 - 3 can be shared with ADC input channel (AN4 - 7).
- PORTD.0 - 1 can be shared with ADC AN8-9 input channel (AN8 - 9).
- The OSCO pin can be shared with PORTC.0, if the SH69P48A uses the External clock or the RC oscillator as the system oscillation. (Refer to the Code option (OP_OSC [2:0]).)
- The OSCI pin can be shared with PORTE.0, if the SH69P48A uses the internal RC oscillator as the system oscillation. (Refer to the Code option (OP_OSC [2:0]).)
- The RESET pin can be shared with PORTE.1 for open drain output. (Refer to the OTP option (OP_RST).)

Port Interrupt

The PORTB and PORTD are used as external port interrupt sources. Since PORTB and PORTD are bit programmable I/Os, only the voltage transition from V**DD** to GND applying to the digital input port can generate a port interrupt. The analog input cannot generate any interrupt request.

The interrupt control flags are mapped on $385, $387 of the system register. They can be accessed or tested by the read/write operation. Those flags are cleared to “0” at the initialization by the chip reset.

Port Interrupts (including other external interrupt sources) can be used to wake up the CPU from the HALT or the STOP mode.

System Register $384, $386: Port Interrupt Enable Flags Register

Address	Bit 3	Bit 2	Bit 1	Bit 0	R/W	Remarks
$384	PDIEN.3	PDIEN.2	PDIEN.1	PDIEN.0	R/W	PORTD interrupt enable flags
$386	PBIEN.3	PBIEN.2	PBIEN.1	PBIEN.0	R/W	PORTB interrupt enable flags

PDIEN.n, PBIEN.n (n = 0, 1, 2, 3)
0: Disable port interrupt. (Default)
1: Enable port interrupt.

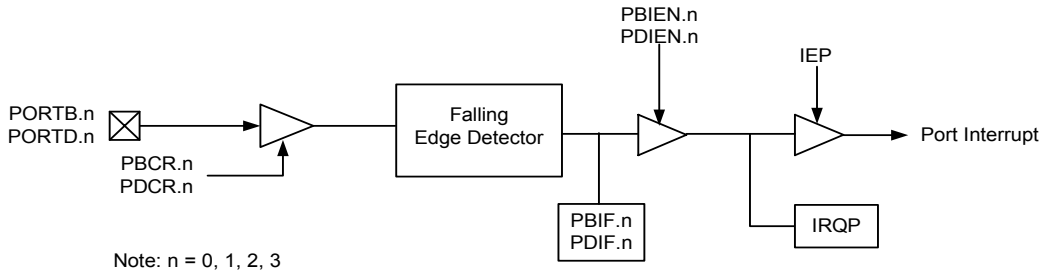
System Register $385, $387: Port Interrupt Request Flags Register

Address	Bit 3	Bit 2	Bit 1	Bit 0	R/W	Remarks
$385	PDIF.3	PDIF.2	PDIF.1	PDIF.0	R/W	PORTD interrupt request flags
$387	PBIF.3	PBIF.2	PBIF.1	PBIF.0	R/W	PORTB interrupt request flags

PDIF.n, PBIF.n (n = 0, 1, 2, 3)
0: Port interrupt is not present. (Default)
1: Port interrupt is present.

Only writing these bits to 0 is available.

Following is the port interrupt function block-diagram for reference.



Port Interrupt Function Block-Diagram

Port Interrupt Programming Notes:

When the Port falling edge is active, any I/O input pin transition from V_{DD} to GND will set PIF.n to “1”. Meanwhile, if the PIEN.n = 1, the port will generate an interrupt request (IRQP = 1).

Port Interrupt can wake the CPU from the HALT or STOP mode.

ADC Converter Enable Register $14:

Address	Bit 3	Bit 2	Bit 1	Bit 0	R/W	Remarks
$14	VREFS	-	-	ADCON	R/W	Bit0: Set ADC module operate Bit3: Select Internal/External reference voltage
	X	-	-	0	R/W	Disable the ADC converter module. (Default)
	X	-	-	1	R/W	Enable the ADC converter module.

When an ADC converter is disabled, PORTA.0-3, PORTB.0-3 and PORTD.0-1 are used as normal I/O ports. When an ADC converter is enabled, set the ADC port configuration register ($16) to select anyone of PORTA.0-3, PORTB.0-3 and PORTD.0-1 as a normal I/O port or ADC port. For detail, refer to ADC converter description.

PORTC.1 can be shared with the reference voltage input (VREF).
ADC Port Configuration Control Register $14:

Address	Bit 3	Bit 2	Bit 1	Bit 0	R/W	Remarks
$14	VREFS	-	-	ADCON	R/W	Bit0: Set ADC module operate Bit3: Select Internal/External reference voltage
	0	-	-	X	R/W	Set PORTC.1 as a normal I/O port (Default)
	1	-	-	X	R/W	Set PORTC.1 as the external reference voltage input

PORTC.2 can be shared with the PWM0 output (PWM0).
PWM0 Control Register $20:

Address	Bit 3	Bit 2	Bit 1	Bit 0	R/W	Remarks
$20	PWM0S	T0CK1	T0CK0	PWM0_EN	R/W	Bit0: PWM0 output enable Bit2, Bit1: Select PWM0 clock Bit3: Set PWM0 output mode of duty cycle
	X	X	X	0	R/W	Set PORTC.2 as a normal I/O port and disable PWM0 (Default)
	X	X	X	1	R/W	Set PORTC.2 as PWM0 output and enable PWM0

PORTC.3 can be shared with the Timer0 external input (T0).

Timer0 Mode Register $02:

Address	Bit 3	Bit 2	Bit 1	Bit 0	R/W	Remarks
$02	T0S	T0M.2	T0M.1	T0M.0	R/W	Bit2-0: Timer0 mode register Bit3: T0 signal source
	0	X	X	X	R/W	Set PORTC.3 as a normal I/O port (Default)
	1	X	X	X	R/W	Set PORTC.3 as T0 input (falling edge active)

PORTD.2 can be shared with the Timer1 input capture. (T1)

Timer1 Control Register $13:

Address	Bit 3	Bit 2	Bit 1	Bit 0	R/W	Remarks
$13	T1GO	DEC	-	TM1S0	R/W	Bit1-0: Timer1 mode select
	X	X	-	0	R/W	Set PORTD.2 as a normal I/O port (Default)
	X	X	-	1	R/W	Set PORTD.2 as T1 input

PORTD.3 can be shared with the PWM1 output (PWM1).

PWM1 Control Register $21:

Address	Bit 3	Bit 2	Bit 1	Bit 0	R/W	Remarks
$21	PWM1S	T1CK1	T1CK0	PWM1_EN	R/W	Bit0: PWM1 output enable Bit2, Bit1: Select PWM1 clock Bit3: Set PWM1 output mode of duty cycle
	X	X	X	0	R/W	Set PORTD.3 as a normal I/O port and disable PWM1 (Default)
	X	X	X	1	R/W	Set PORTD.3 as PWM1 output and enable PWM1

7. Timer

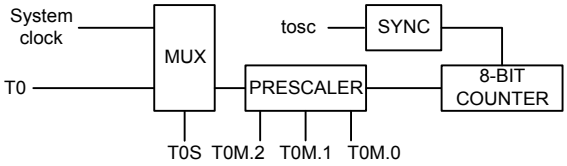
7.1. Timer0

SH69P48A has two 8-bit timers.

The Timer0 has the following features:

- 8-bit up-counting timer/counter.
- Automatic re-loads counter.
- 8-level pre-scale.
- Interrupt on overflow from $FF to $00.

The following is a simplified Timer0 block diagram.



The Timer0 provides the following functions:

- Programmable interval timer function.
- Read counter value.

7.1.1. Timer0 Configuration and Operation

The Timer0 consist of an 8-bit write-only timer load register (TL0L, TL0H) and an 8-bit read-only timer counter (TC0L, TC0H). Each of them has low order digits and high order digits. Writing data into the timer load register (TL0L, TL0H) can initialize the timer counter.

The low-order digit should be written first, and then the high-order digit. The timer counter is automatically loaded with the contents of the load register when the high order digit is written or counter counts overflow from $FF to $00.

Timer Load Register: Since the register H controls the physical READ and WRITE operations.

Please follow these steps:

Write Operation:

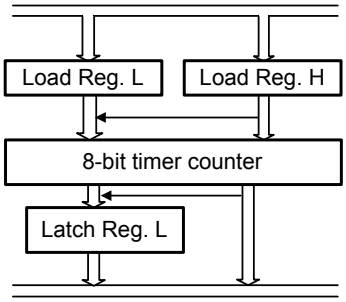
Low nibble first

High nibble to update the counter

Read Operation:

High nibble first

Low nibble followed.



7.1.2. Timer0 Mode Register

The Timer0 can be programmed in several different prescalers by setting the Timer0 Mode register (TM0).

The 8-bit counter prescaler overflow output pulses. The Timer0 Mode register is a 3-bit register used for the timer control as shown bellow. These mode registers select the input pulse sources into the timer.

Timer0 Mode Register: $02

TM0.2	TM0.1	TM0.0	Prescaler Divide Ratio	Clock Source
0	0	0	$/2^{11}$	System clock/T0
0	0	1	$/2^{9}$	System clock/T0
0	1	0	$/2^{7}$	System clock/T0
0	1	1	$/2^{5}$	System clock/T0
1	0	0	$/2^{3}$	System clock/T0
1	0	1	$/2^{2}$	System clock/T0
1	1	0	$/2^{1}$	System clock/T0
1	1	1	$/2^{0}$	System clock/T0

External Clock/Event T0 as Timer0 Source

When external clock/event T0 input as Timer0 source, it is synchronized with the CPU system clock. The external source must follow certain constraints. The system clock samples it in instruction frame cycle. Therefore it is necessary to be high (at least 2 t**osc**) and low (at least 2 t**osc**). When the pre-scale ratio selects /2^0, it is the same as the system clock input.

The requirement is as follows:

T0H (T0 high time) $\geq$ 2 * t**osc** + ΔT

T0L (T0 low time) $\geq$ 2 * t**osc** + ΔT; ΔT = 20ns

When another pre-scale ratio is selected, the TM0 is scaled by the asynchronous ripple counter and so the pre-scale output is symmetrical. Then:

$$\text{T0 high time} = \text{T0 low time} = \frac{N * T0}{2}$$

Where: T0 = Timer0 input period

N = pre-scale value

The requirement is:

$$\frac{N * T0}{2} \geq 2 * tosc + \Delta T \quad \text{or} \quad T0 \geq \frac{4 * tosc + 2 * \Delta T}{N}$$

So, the limitation is applied for the T0 period time only. The pulse width is not limited by this equation. It is summarized as follows:

$$T0 = \text{Timer0 period} \geq \frac{4 * tosc + 2 * \Delta T}{N}$$

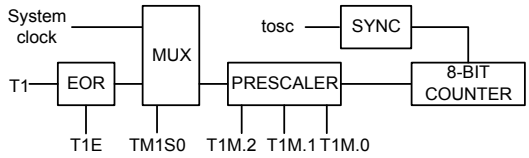
Timer0 Mode Register: $02

Address	Bit 3	Bit 2	Bit 1	Bit 0	R/W	Remarks
$02	T0S	T0M.2	T0M.1	T0M.0	R/W	Bit3: T0 signal source
	0	X	X	X	R/W	Shared with PORTC.3, Timer0 source is system clock (Default)
	1	X	X	X	R/W	Shared with T0 input, Timer0 source is T0 input clock (Falling edge active)

7.2. Timer1

The Timer1 has the following features:
- 8-bit up-counting timer/counter.
- Automatic re-loads counter.
- 8-level pre-scale.
- Interrupt on overflow from $FF to $00.

The following is a simplified Timer1 block diagram.



The Timer1 provides the following functions:
- Programmable interval timer function.
- Read counter value.

7.2.1. Timer1 Configuration and Operation

Timer1 consists of a 8-bit write-only timer load register (TL1L, TL1H) and a 8-bit read-only timer counter (TC1L, TC1H). Each of them has low order digits and high order digits. Writing data into the timer load register (TL1L, TL1H) can initialize the timer counter.

The low-order digit should be written first, and then the high-order digit. The timer counter is automatically loaded with the contents of the load register when the high order digit is written or the counter counts overflow from $FF to $00.

Timer Load Register: Since the register H controls the physical READ and WRITE operations.

Please follow these steps:

Write Operation:

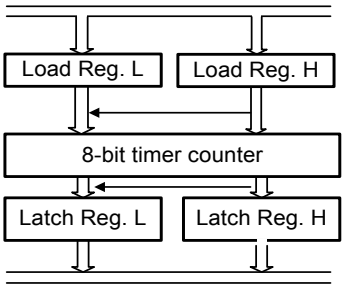
Low nibble first

High nibble to update the counter

Read Operation:

High Nibble first

Low nibble followed.



7.2.2. Timer1 Control Register

The Timer1 can be programmed in two modes: timer and pulse width measurement.

Timer1 Control Register: $13

Address	Bit 3	Bit 2	Bit 1	Bit 0	R/W	Remarks
$13	T1GO	DEC	-	TM1S0	R/W	Bit0: Timer1 control register
	X	X	-	0	R/W	Timer with internal system clock
	X	X	-	1	R/W	Pulse width measurement (T1 pin input)
	0	X	-	X	R/W	Timer/counter stops (Read: status; Write: command) (default)
	1	X	-	X	R/W	Timer/counter starts (Read: status; Write: command)

(a) Timer Mode

In this mode, Timer1 is performed using the internal clock. The contents of the Timer1 counter register ($06 - $07) are loaded into the up-counter while the highest nibble ($07) has been written. The up counter will start counting if the T1GO (bit3) in the Timer1 control register ($13) is set to 1. The Timer1 interrupt will be issued when the up counter overflows from $FF to $00 if the Interrupt enable register ($00) bit1 (IET1) is set to 1.

After the T1GO (bit3) in the Timer1 control register ($13) has been set to 1, writing the Timer1 counter register ($06 - $07) can't affect the up counter operating anymore. Only when the T1GO (bit3) in the Timer1 control register ($13) has been reset to 0, will the revised contents of the Timer1 counter register ($06 - $07) be loaded into the up-counter while the highest nibble ($07) is written.

Timer1 Mode Register: $03

Address	Bit 3	Bit 2	Bit 1	Bit 0	R/W	Remarks
$03	T1E	T1M.2	T1M.1	T1M.0	R/W	Bit2-0: Timer1 mode register Bit3: T1 external signal edge select
	X	0	0	0	R/W	Timer clock: System clock/2^{11}
	X	0	0	1	R/W	Timer clock: System clock/2^{9}
	X	0	1	0	R/W	Timer clock: System clock/2^{7}
	X	0	1	1	R/W	Timer clock: System clock/2^{5}
	X	1	0	0	R/W	Timer clock: System clock/2^{3}
	X	1	0	1	R/W	Timer clock: System clock/2^{2}
	X	1	1	0	R/W	Timer clock: System clock/2^{1}
	X	1	1	1	R/W	Timer clock: System clock/2^{0}
	0	X	X	X	R/W	T1 input falling edge active (Default)
	1	X	X	X	R/W	T1 input rising edge active

(b) Pulse width Measurement Mode

In this mode, Timer1 is performed using a special function under the timer mode in which counting is started on an edge of the pulse waveform that is input to the T1 pin. It is possible to measure the width of the pulse waveform by reading the up-counter values on state transitions of the input to the T1 pin. The rising or falling edge of the T1 pin input is selected by setting the T1E (bit3) in the Timer1 mode register ($03). But the source clock of the up counter is an internal clock selected by properly setting the T1M (bit2-0) in the Timer1 mode register ($03). When the T1GO (bit3) in the Timer1 control register ($13) is set to “1”, the contents of the up counter must reset to “00H”, automatically. Then a rising (falling) edge signal on the T1 input pin triggers the up counter to start counting. At the next falling (rising) edge, the counter value is loaded to the Timer1 counter register ($06 - $07), individually. Simultaneously, the Timer1 interrupt will be generated if the Interrupt enable register ($00) bit1 (IET1) is set to 1.

When DEC (bit2) in the Timer1 control register ($13) is 0, the Timer1 is in the one-edge capture operation. If the rising edge is selected as the counter-trigging signal, at the next falling edge, the Timer1 interrupt request will be generated. At the same time, the contents of the up-counter must be loaded to the Timer1 counter register ($06 - $07) at first and then will be cleared again and the counter will halted. When the next rising edge applies to the T1 input pin, the up counter will start counting for another measurement cycle.

When DEC (bit2) in the Timer1 control register ($13) is 1, the Timer1 is in the double-edge capture operation. If the rising edge is selected as the counter- trigging signal, at the next falling edge, the Timer1 interrupt request will be generated. At the same time, the contents of the up-counter must be loaded to the Timer1 counter register ($06 - $07) at first and then the counter will continue counting. When the next rising edge applies to the T1 input pin, the Timer1 interrupt request is also generated. At this time, the contents of the up-counter must be loaded to the Timer1 counter register ($06 - $07) again, then the counter must be cleared and can be continued to start counting following measurement cycles.

In this mode, writing the Timer1 counter register ($06 ~ $07) at any time can’t affect the up counter operating anymore.

In this mode, the T1 pin input signal must follow certain constraints. So, the limitation is applied for the T1 period time described as follows:

T1 (period time) $\geq 1 * t_{\text{Timer clock}} + 2 * \Delta T$; ΔT= 20ns

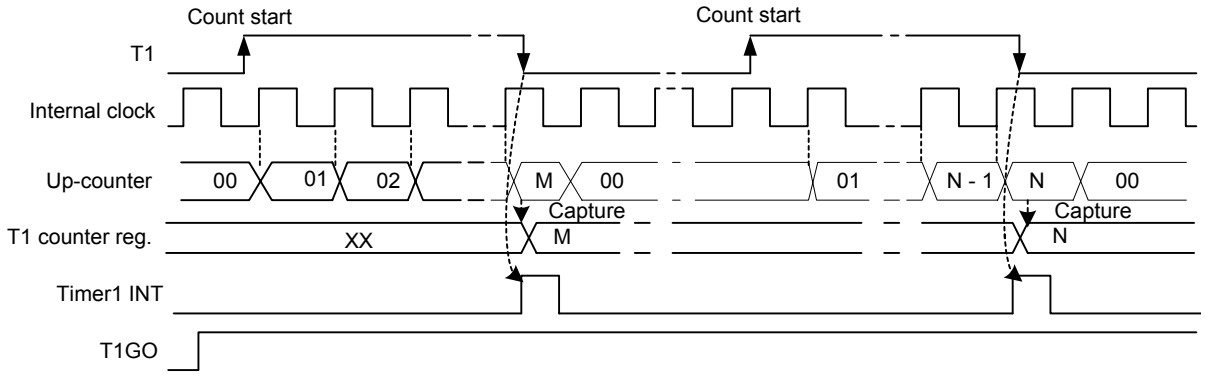
T1 (period time) $\geq (M * t_{OSC}) + 2 * \Delta T$

Where M (pre-scale value for Timer1 internal clock) =2^0, 2^1, 2^2, 2^3, 2^5, 2^7, 2^9or 2^{11}

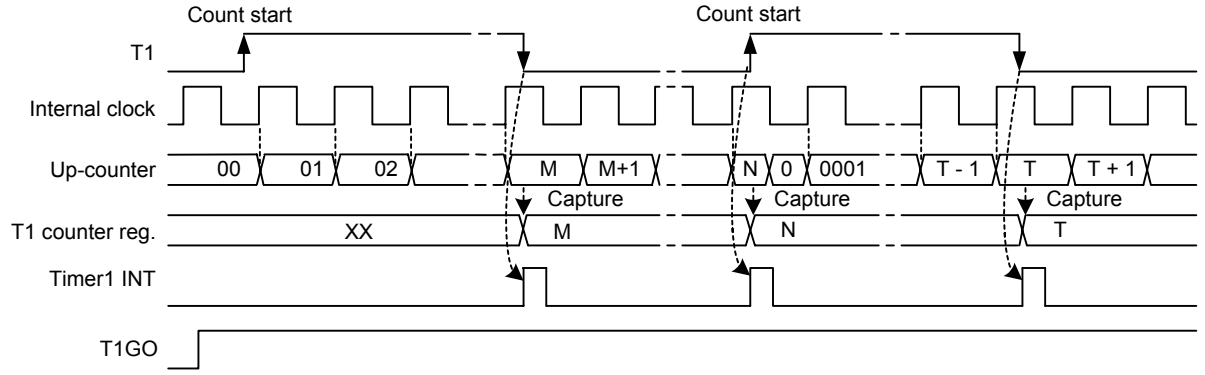
But, in order to correctly get the pulse measurement value in programming, a sufficient “wait time” is required for the relevant Timer1 interrupt subroutine program.

Timer1 Counter Register: $06 - $07

Address	Bit 3	Bit 2	Bit 1	Bit 0	R/W	Remarks
$06	T1L.3	T1L.2	T1L.1	T1L.0	R/W	Timer1 load/counter register (low nibble)
$07	T1H.3	T1H.2	T1H.2	T1H.0	R/W	Timer1 load/counter register (high nibble)



One edge capture (DEC = 0)



Double edge capture (DEC = 1)

Timer1 Control Register: $13 (under the pulse width measurement mode)

Address	Bit 3	Bit 2	Bit 1	Bit 0	R/W	Remarks
$13	T1GO	DEC	-	TM1S0	R/W	Bit0: Timer1 mode select
	X	0	-	1	R/W	Bit2: One edge capture
	X	1	-	1	R/W	Bit2: Double edge capture

8. Interrupt

Four interrupt sources are available on SH69P48A:
- ADC interrupt
- Timer0 interrupt
- Timer1 interrupt
- PORTB/D interrupts (Falling edge)

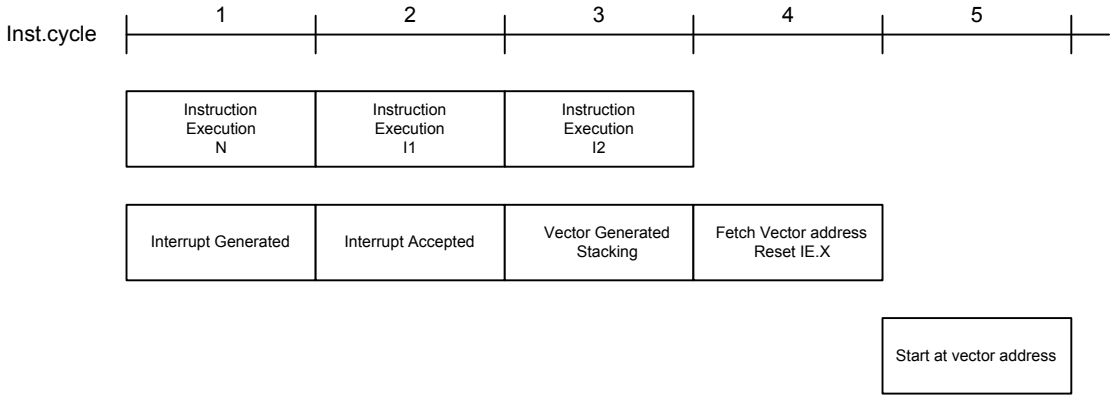
Interrupt Control Bits and Interrupt Service

The interrupt control flags are mapped on $00 and $01 of the system register. They can be accessed or tested by the program. Those flags are clear to “0” at initialization by the chip reset.

System Register:

Address	Bit 3	Bit 2	Bit 1	Bit 0	R/W	Remarks
$00	IEAD	IET0	IET1	IEP	R/W	Interrupt enable flags
$01	IRQAD	IRQT0	IRQT1	IRQP	R/W	Interrupt request flags

When IEx is set to “1” and the interrupt request is generated (IRQx is 1), the interrupt will be activated and vector address will be generated from the priority PLA corresponding to the interrupt sources. When an interrupt occurs, the PC and CY flag will be saved into stack memory and jump to interrupt service vector address. After the interrupt occurs, all interrupt enable flags (IEx) are clear to “0” automatically, so when IRQx is 1 and IEx is set to “1” again, the interrupt will be activated and vector address will be generated from the priority PLA corresponding to the interrupt sources.



Interrupt Servicing Sequence Diagram

Interrupt Nesting:

During the CPU interrupt service, the user can enable any interrupt enable flag before returning from the interrupt. The servicing sequence diagram shows the next interrupt and the next nesting interrupt occurrences. If the interrupt request is ready and the instruction of execution N is IE enabled, then the interrupt will start immediately after the next two instruction executions. However, if instruction I1 or instruction I2 disables the interrupt request or enable flag, then the interrupt service will be terminated.

ADC Interrupt

Bit3 (IEAD) of system register $00 is the ADC interrupt enable flag. When the ADC conversion is complete, it will generate an interrupt request (IRQAD = 1), if the ADC interrupt is enabled (IEAD = 1), an ADC interrupt service routine will start. The ADC interrupt can be used to wake the CPU from HALT mode.

Timer (Timer0, Timer1) Interrupt

The input clock of Timer0 and Timer1 are based on system clock or external clock/event T0 input as Timer0 source. The timer overflow from $FF to $00 will generate an internal interrupt request (IRQT0 or IRQT1 = 1), If the interrupt enable flag is enabled (IET0 or IET1 = 1), a timer interrupt service routine will start. Timer interrupt can also be used to wake the CPU from HALT mode.

Port Falling Edge Interrupt

Only the digital input port can generate a port interrupt. The analog input cannot generate any interrupt request.
Port Interrupt can be used to wake the CPU from the HALT or STOP mode.

Port Interrupts by Bit

Only the digital input port can generate a port interrupt. The analog input cannot generate any interrupt request.

System Register $384, $386: Port Interrupt Enable Flags Register

Address	Bit 3	Bit 2	Bit 1	Bit 0	R/W	Remarks
$384	PDIEN.3	PDIEN.2	PDIEN.1	PDIEN.0	R/W	PORTD interrupt enable flags
$386	PBIEN.3	PBIEN.2	PBIEN.1	PBIEN.0	R/W	PORTB interrupt enable flags

System Register $385, $387: Port Interrupt Request Flags Register

Address	Bit 3	Bit 2	Bit 1	Bit 0	R/W	Remarks
$385	PDIF.3	PDIF.2	PDIF.1	PDIF.0	R/W	PORTD interrupt request flags
$387	PBIF.3	PBIF.2	PBIF.1	PBIF.0	R/W	PORTB interrupt request flags

9. Analog/Digital Converter (ADC)

The 10 channels and the 10-bit resolution ADC converter are implemented in this micro-controller.

The ADC converter control registers can be used to define the ADC channel number, select analog channel, reference voltage and conversion clock, start ADC conversion, and set the end of ADC conversion flags. The ADC conversion result register byte is read-only.

The approach for ADC conversion:

- Set analog channel and select reference voltage. (When using the external reference voltage, keep in mind that any analog input voltage must not exceed V_{REF})
- Operating ADC converter module and select the converted analog channels.
- Set ADC conversion clock source.
- GO/$\overline{\text{DONE}}$ = 1, start ADC conversion.

Systems Register $14

Address	Bit 3	Bit 2	Bit 1	Bit 0	R/W	Remarks
$14	VREFS	-	-	ADCON	R/W	Bit0: Set ADC module operate Bit3: Select Internal/External reference voltage
	X	-	-	0	R/W	ADC converter module not operating
	X	-	-	1	R/W	ADC converter module operating
	0	-	-	X	R/W	Internal reference voltage (V_{REF} = V_{DD})
	1	-	-	X	R/W	External reference voltage

Systems Register $16

Address	Bit 3	Bit 2	Bit 1	Bit 0	R/W	Remarks
$16	ACR3	ACR2	ACR1	ACR0	R/W	Bit3-0: ADC port configuration control
	0	0	0	0	R/W	See the following table

Set Analog Channels

ACR3	ACR2	ACR1	ACR0	9	8	7	6	5	4	3	2	1	0
0	0	0	0	PD.1	PD.0	PB3	PB.2	PB.1	PB.0	PA.3	PA.2	PA.1	PA.0
0	0	0	1	PD.1	PD.0	PB.3	PB.2	PB.1	PB.0	PA.3	PA.2	PA.1	AN0
0	0	1	0	PD.1	PD.0	PB.3	PB.2	PB.1	PB.0	PA.3	PA.2	AN1	AN0
0	0	1	1	PD.1	PD.0	PB.3	PB.2	PB.1	PB.0	PA.3	AN2	AN1	AN0
0	1	0	0	PD.1	PD.0	PB.3	PB.2	PB.1	PB.0	AN3	AN2	AN1	AN0
0	1	0	1	PD.1	PD.0	PB.3	PB.2	PB.1	AN4	AN3	AN2	AN1	AN0
0	1	1	0	PD.1	PD.0	PB.3	PB.2	AN5	AN4	AN3	AN2	AN1	AN0
0	1	1	1	PD.1	PD.0	PB.3	AN6	AN5	AN4	AN3	AN2	AN1	AN0
1	X	0	0	PD.1	PD.0	AN7	AN6	AN5	AN4	AN3	AN2	AN1	AN0
1	X	0	1	PD.1	AN8	AN7	AN6	AN5	AN4	AN3	AN2	AN1	AN0
1	X	1	X	AN9	AN8	AN7	AN6	AN5	AN4	AN3	AN2	AN1	AN0

System Register $17 for ADC Channel Selection

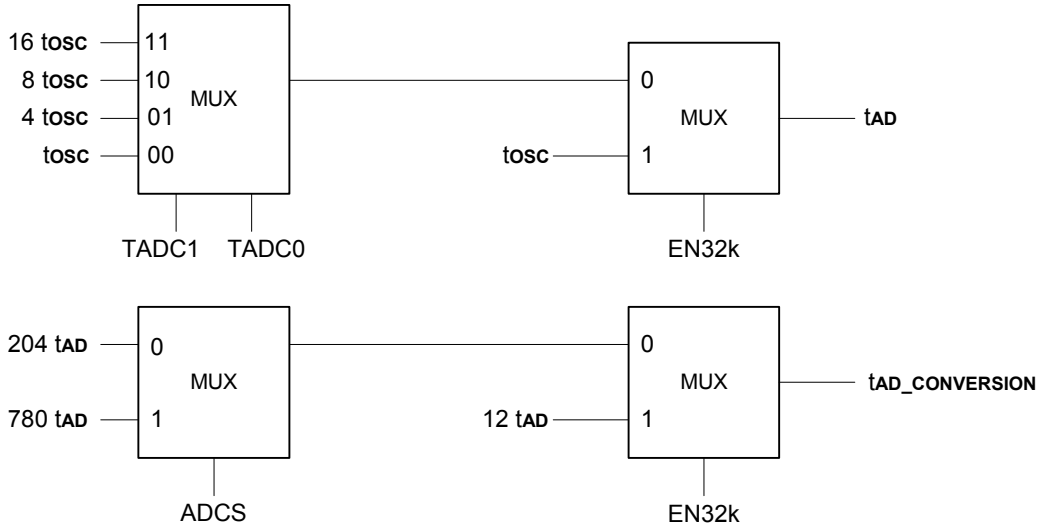
Address	Bit 3	Bit 2	Bit 1	Bit 0	R/W	Remarks
$17	CH3	CH2	CH1	CH0	R/W	Bit3-0: Select ADC channel
	0	0	0	0	R/W	ADC channel AN0
	0	0	0	1	R/W	ADC channel AN1
	0	0	1	0	R/W	ADC channel AN2
	0	0	1	1	R/W	ADC channel AN3
	0	1	0	0	R/W	ADC channel AN4
	0	1	0	1	R/W	ADC channel AN5
	0	1	1	0	R/W	ADC channel AN6
	0	1	1	1	R/W	ADC channel AN7
	1	X	X	0	R/W	ADC channel AN8
	1	X	X	1	R/W	ADC channel AN9

System Register $2D - $2F for ADC Data

Address	Bit 3	Bit 2	Bit 1	Bit 0	R/W	Remarks
$2D	X	X	A1	A0	R	ADC data low nibble (Read only)
$2E	A5	A4	A3	A2	R	ADC data medium nibble (Read only)
$2F	A9	A8	A7	A6	R	ADC data high nibble (Read only)

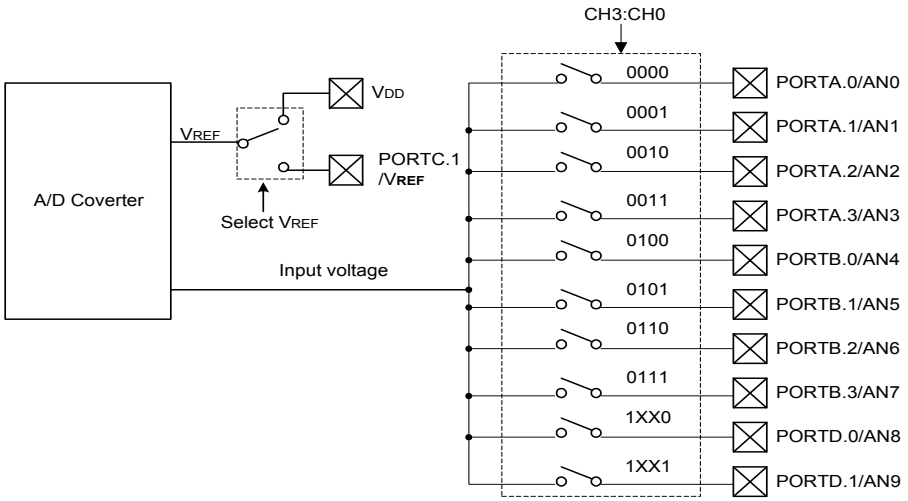
Systems Register $15

Address	Bit 3	Bit 2	Bit 1	Bit 0	R/W	Remarks	
$15	GO/$\overline{\text{DONE}}$	TADC1	TADC0	ADCS	R/W	Bit0: Set ADC conversion time Bit2-1: Select ADC clock period Bit3: ADC status flag	
	X	X	X	0	R/W	ADC conversion time = 204 t_{AD}	When oscillator type is not selected as 32.768kHz crystal oscillator in code option selection.
	X	X	X	1	R/W	ADC conversion time = 780 t_{AD}	
	X	0	0	X	R/W	ADC clock period t_{AD} = t_{OSC}	
	X	0	1	X	R/W	ADC clock period t_{AD} = 4t_{OSC}	
	X	1	0	X	R/W	ADC clock period t_{AD} = 8t_{OSC}	
	X	1	1	X	R/W	ADC clock period t_{AD} = 16t_{OSC}	
	X	Any Value			R/W	ADC conversion time = 12 t_{AD}, ADC clock period t_{AD} = t_{OSC}	When oscillator type is selected as 32.768kHz crystal oscillator in code option selection.
	0	X	X	X	R/W	ADC conversion not in progress	
	1	X	X	X	R/W	ADC conversion in progress, when ADCON = 1	



ADC Conversion Time Diagram

In the above diagram, EN32k equals to 1 when the 32.768kHz crystal oscillator is selected as oscillator type in code option; EN32k equals to 0 when the 32.768kHz crystal oscillator is not selected as oscillator type in code option.



ADC Converter Block Diagram

Notes:

- Select ADC clock period t_{AD}, make sure that $1\mu s \leq t_{AD} \leq 33.4\ \mu s$.
- When the ADC conversion is complete, an ADC converter interrupt occurs (if the ADC converter interrupt is enabled).
- The analog input channels must have their corresponding PXCR (X = A, B, D) bits selected as inputs.
- If an I/O port is selected as analog input, the I/O functions and pull-high resistor will be disabled.
- Bit GO/$\overline{\text{DONE}}$ is automatically cleared by hardware when the ADC conversion is complete.
- Clearing the GO/$\overline{\text{DONE}}$ bit during a conversion will abort the current conversion.
- The ADC result register will NOT be updated with the partially completed ADC conversion sample.
- 4t_{OSC} wait is required before the next acquisition is started.
- ADC converter can keep on working in the HALT mode, and would stop automatic while enabling a “STOP” instruction.
- ADC converter can wake-up the device from the HALT mode (if the ADC converter interrupt is enabled).

10. Pulse Width Modulation (PWM)

The SH69P48A consists of two 8+2 PWM modules. The PWM module can provide the pulse width modulation waveform with the period and the duty being controlled, individually. The PWMC is used to control the PWM module operation with proper clocks. The PWMP is used to control the period cycle of the PWM module output. And the PWMD is used to control the duty in the waveform of the PWM module output.

System Register $20, $21: PWM Control Register (PWMC)

Address	Bit 3	Bit 2	Bit 1	Bit 0	R/W	Remarks
$20, $21	PWMnS	TnCK1	TnCK0	PWMn_EN	R/W	Bit0: PWMn output enable Bit2, Bit1: Select PWMn clock Bit3: Set PWMn output mode of duty cycle
	X	X	X	0	R/W	Shared with I/O port (Default)
	X	X	X	1	R/W	Shared with PWMn, n = 0 or 1
	X	0	0	X	R/W	PWMn clock = t**osc** (Default)
	X	0	1	X	R/W	PWMn clock = 2t**osc**
	X	1	0	X	R/W	PWMn clock = 4t**osc**
	X	1	1	X	R/W	PWMn clock = 8t**osc**
	0	X	X	X	R/W	PWMn output normal mode of duty cycle (high active) (Default)
	1	X	X	X	R/W	PWMn output negative mode of duty cycle (low active)

n = 0 or 1
The PWM0 output pin is shared with PORTC.2.
The PWM1 output pin is shared with PORTD.3.

System Register $22 - $23, $27 - $28: PWM Period Control Register (PWMP)

Address	Bit 3	Bit 2	Bit 1	Bit 0	R/W	Remarks
$22, $27	PPn.3	PPn.2	PPn.1	PPn.0	R/W	PWMn period low nibble
$23, $28	PPn.7	PPn.6	PPn.5	PPn.4	R/W	PWMn period high nibble

n = 0 or 1
PWM output period cycle = [PPn.7, PPn.0] X PWMn clock.
When [PPn.7, PPn.0] = 00H, PWMn will output GND if the PWMnS bit is set to “0”.
When [PPn.7, PPn.0] = 00H, PWMn will output high level if the PWMnS bit is set to “1”.

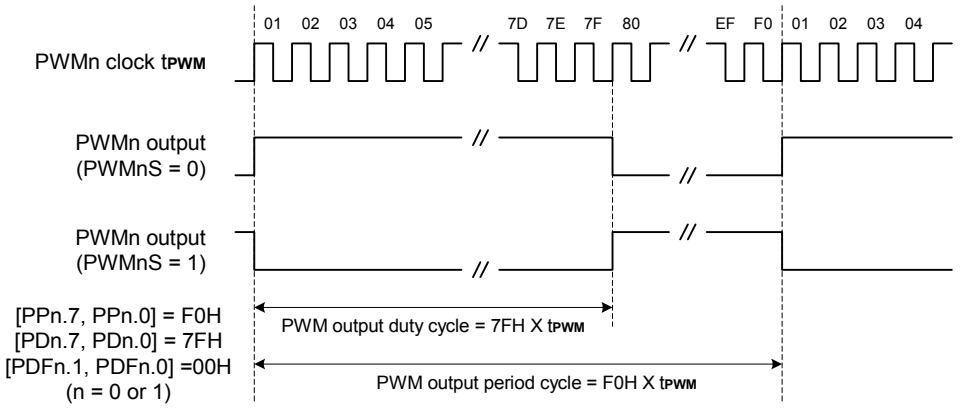
System Register $24 - $26, $29 - $2B: PWM Duty Control Register (PWMD)

Address	Bit 3	Bit 2	Bit 1	Bit 0	R/W	Remarks
$24	-	-	PDF0.1	PDF0.0	R/W	PWM0 duty fine tune nibble
$25	PD0.3	PD0.2	PD0.1	PD0.0	R/W	PWM0 duty low nibble
$26	PD0.7	PD0.6	PD0.5	PD0.4	R/W	PWM0 duty high nibble
$29	-	-	PDF1.1	PDF1.0	R/W	PWM1 duty fine tune nibble
$2A	PD1.3	PD1.2	PD1.1	PD1.0	R/W	PWM1 duty low nibble
$2B	PD1.7	PD1.6	PD1.5	PD1.4	R/W	PWM1 duty high nibble

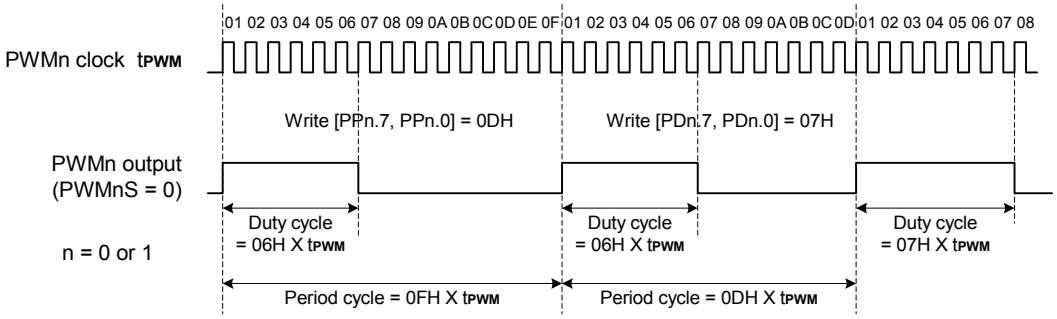
n = 0 or 1
Average PWMn output duty cycle = ([PDn.7, PDn.0] + [PDFn.1, PDFn.0]/4) X PWMn clock.
If [PPn.7, PPn.0] ≤ [PDn.7, PDn.0], PWMn outputs high when the PWMnS bit is set to “0”.
If [PPn.7, PPn.0] ≤ [PDn.7, PDn.0], PWMn outputs GND level when the PWMnS bit is set to “1”.

Note:

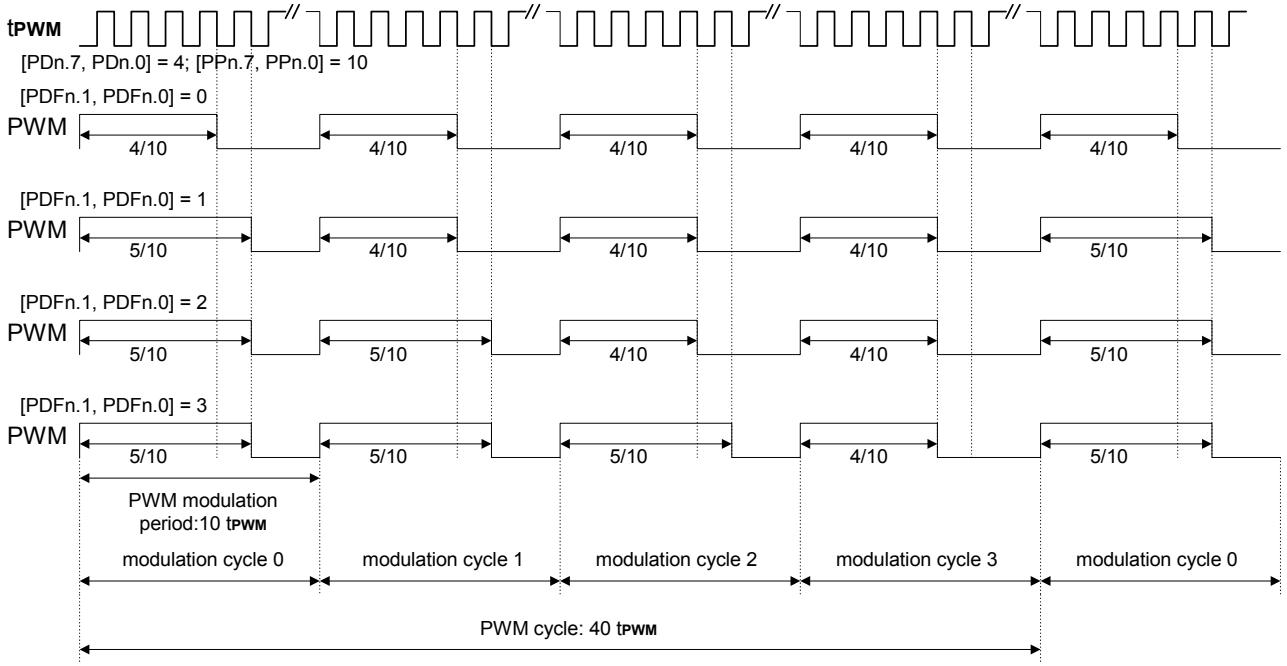
- If the I/O port is selected as the PWM output, the I/O functions and pull-high resistor will be disabled.
- The writing flow of the PWMn duty control register is described as follows. First set the fine tune nibble, and then the low nibble, and set the high nibble at last.
- The writing flow of the PWMn period control register is described as follows. First set the low nibble, and then set the high nibble.
- After the high nibble of the PWMn period or duty control register is written, the data are loaded into the re-load counter and start counting in the next period.
- The reading flow of the PWMn period or duty control register is at the reverse direction with that described above. First read the high nibble, and then read the low nibble.
- PWM can keep on working in the HALT mode, and will stop automatic when the "STOP" instruction is enabled.



PWM Output Example



PWM Output Period or Duty Cycle Changing Example



(8+2) bits PWM Waveform

In the (8+2) bits PWM waveform, A PWM cycle is divided into 4 modulation cycles (cycle 0 - cycle 3), each modulation cycle has certain period decided by period cycle registers (PWMP). The contents of duty cycle register (PWMD) are divided into two parts. The basic part of PWMD is PDn.7 - PDn.0. The extended part is PDFn.1 - PDFn.0. In a PWM cycle, the duty cycle of each modulation cycle is shown in the table.

Parameter	[PDFn.1, PDFn.0] (0-3)	Duty Cycle
Modulation Cycle I (I = 0 - 3)	I < [PDFn.1, PDFn.0]	([PDn.7, PDn.0] + 1)/[PPn.7, PPn.0]
	I ≥ [PDFn.1, PDFn.0]	[PDn.7, PDn.0]/[PPn.7, PPn.0]

The modulation period, cycle period and cycle duty of the PWM output signal are summarized in the following table.

PWM modulation period	PWM cycle period	PWM cycle duty
[PPn.7, PPn.0] X t_{PWM}	4*[PPn.7, PPn.0] X t_{PWM}	(4 X [PDn.7, PDn.0] + [PDFn.1, PDFn.0])/(4 X [PPn.7, PPn.0])

11. Low Voltage Reset (LVR)

The LVR function is to monitor the supply voltage and generate an internal reset in the device. It is typically used in AC line applications or large battery where heavy loads may be switched in and cause the device voltage to temporarily fall below the specified operating minimum.

The LVR function is selected by the Code option.

The LVR circuit will feature the following functions when the LVR function is enabled:

- Generates a system reset when $V_{DD} \leq V_{LVR}$.
- Cancels the system reset when $V_{DD} > V_{LVR}$.

12. Watchdog Timer (WDT)

The watchdog timer is a count-down counter, and its clock source is an independent built-in RC oscillator, so that it will always run even in the STOP mode. The watchdog timer will automatically generate a device reset when it overflows. It can be enabled or disabled permanently by using the code option.

The watchdog timer control bits ($1E bit2 - bit0) are used to select different overflow frequencies. The watchdog timer overflow flag ($1E bit3) will be automatically set to “1” by hardware when the watchdog timer overflows. By reading or writing the system register $1E, the watchdog timer should re-count before the overflow happens.

System Register $1E: Watchdog Timer (WDT)

Address	Bit 3	Bit 2	Bit 1	Bit 0	R/W	Remarks
$1E	- WDT	WDT.2 -	WDT.1 -	WDT.0 -	R/W R	Bit2-0: Watchdog timer control Bit3: Watchdog timer overflow flag (Read only)
	X	0	0	0	R/W	Watchdog timer-out period = 4096ms
	X	0	0	1	R/W	Watchdog timer-out period = 1024ms
	X	0	1	0	R/W	Watchdog timer-out period = 256ms
	X	0	1	1	R/W	Watchdog timer-out period = 128ms
	X	1	0	0	R/W	Watchdog timer-out period = 64ms
	X	1	0	1	R/W	Watchdog timer-out period = 16ms
	X	1	1	0	R/W	Watchdog timer-out period = 4ms
	X	1	1	1	R/W	Watchdog timer-out period = 1ms
	0	X	X	X	R	No watchdog timer overflow reset
	1	X	X	X	R	Watchdog timer overflow, WDT reset happens

Note:
Watchdog timer-out period valid for V_{DD} = 5V.

13. HALT and STOP Mode

After the execution of HALT instruction, SH69P48A will enter the HALT mode. In the HALT mode, CPU will STOP operating. But peripheral circuit (Timer0, Timer1, ADC and watchdog timer) will keep status.

After the execution of STOP instruction, SH69P48A will enter the STOP mode. The whole chip (including oscillator) will STOP operating. But watchdog is still enabled.

In the HALT mode, SH69P48A can be waked up if any interrupt occurs.

In the STOP mode, SH69P48A can be waked up if port interrupt occurs or watchdog timer overflow (WDT is enabled).

When CPU is awaked from the HALT/STOP by any interrupt source, it will execute the relevant interrupt serve subroutine at first. Then the instruction next to HALT/STOP is executed.

14. Warm-up Timer

The device has a built-in warm-up timer to eliminate unstable state of initial oscillation when oscillator starts oscillating in the following conditions:

Power-on Reset

Warm-up time interval:
(1) When oscillator range is 30kHz - 2MHz, the warm-up counter prescaler divide ratio is 2^{12} (4096)
(2) When oscillator range is 2MHz -10MHz, the warm-up counter prescaler divide ratio is 2^{14} (16384).

Wake up from Stop Mode

Warm-up time interval:
(1) In RC oscillator or external clock mode, the warm-up counter prescaler divide ratio is 2^7 (128).
(2) In Crystal oscillator or Ceramic resonator mode, the warm-up counter prescaler divide ratio is 2^{12} (4096).

15. Code Option

Oscillator Type:

OP_OSC [2:0]:

000 = External clock (Select OSCO pin as PORTC.0 for a normal I/O port) (Default)
001 = Internal R**osc** RC oscillator (4MHz) (Select OSCO pin as PORTC.0 and OSCI pin as PORTE.0 for normal I/O ports)
010 = Internal R**osc** RC oscillator (4MHz) (Select OSCO pin as PORTC.0 and OSCI pin as PORTE.0 for normal I/O ports)
011 = Internal R**osc** RC oscillator (4MHz) (Select OSCO pin as PORTC.0 and OSCI pin as PORTE.0 for normal I/O ports)
100 = External R**osc** RC oscillator (400kHz - 10MHz) (Select OSCO pin as PORTC.0 for a normal I/O port)
101 = Ceramic resonator (400kHz - 10MHz)
110= Crystal oscillator (400kHz - 10MHz)
111 = 32.768kHz Crystal oscillator

Oscillator Range:

OP_OSC 3:
0 = 2MHz - 10MHz (Default)
1 = 30kHz - 2MHz

Watchdog Timer:

OP_WDT:
0 = Enable (Default)
1 = Disable

Low Voltage Reset:

OP_LVR:
0 = Disable (Default)
1 = Enable

LVR Voltage Range:

OP_LVR0:
0 = High LVR voltage (Default)
1 = Low LVR voltage

Chip pin Reset:

OP_RST:

0 = Enable chip pin reset (Default)

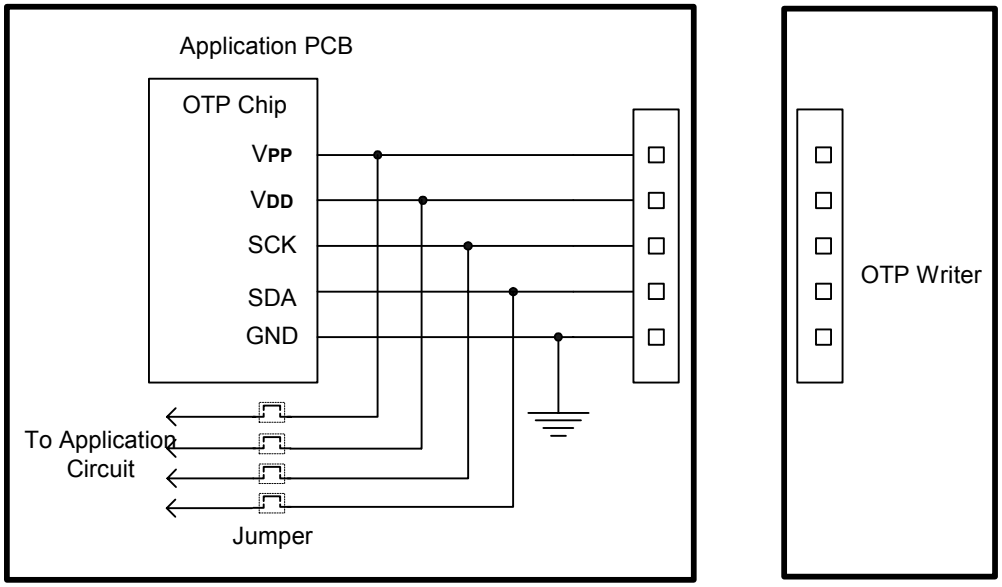
1 = Disable chip pin reset (Select RESET pin as PORTE.1 for an open drain output)

In System Programming Notice for OTP

The In System Programming technology is valid for OTP chip.

The Programming Interface of the OTP chip must be set on user's application PCB, and users can assemble all components including the OTP chip in the application PCB before programming the OTP chip. Of course, it's accessible bonding OTP chip only first, and then programming code and finally assembling other components.

Since the programming timing of Programming Interface is very sensitive, therefore four jumpers are needed (V_{DD}, V_{PP}, SDA, SCK) to separate the programming pins from the application circuit as shown in the following diagram.



The recommended steps are the followings:

(1) The jumpers are open to separate the programming pins from the application circuit before programming the chip.

(2) Connect the programming interface with OTP writer and begin programming.

(3) Disconnect OTP writer and shorten these jumpers when programming is completed.

For more detail information, please refer to the OTP writer user manual.

Instruction Set

All instructions are one cycle and one-word instructions. The characteristic is memory-oriented operation.

1. Arithmetic and Logical Instruction

1.1. Accumulator Type

Mnemonic	Instruction Code	Function	Flag Change
ADC X (, B)	00000 0bbb xxx xxxx	AC <- Mx + AC + CY	CY
ADCM X (, B)	00000 1bbb xxx xxxx	AC, Mx <- Mx + AC + CY	CY
ADD X (, B)	00001 0bbb xxx xxxx	AC <- Mx + AC	CY
ADDM X (, B)	00001 1bbb xxx xxxx	AC, Mx <- Mx + AC	CY
SBC X (, B)	00010 0bbb xxx xxxx	AC <- Mx + -AC + CY	CY
SBCM X (, B)	00010 1bbb xxx xxxx	AC, Mx <- Mx + -AC + CY	CY
SUB X (, B)	00011 0bbb xxx xxxx	AC <- Mx + -AC +1	CY
SUBM X (, B)	00011 1bbb xxx xxxx	AC, Mx <- Mx + -AC +1	CY
EOR X (, B)	00100 0bbb xxx xxxx	AC <- Mx ⊕ AC	
EORM X (, B)	00100 1bbb xxx xxxx	AC, Mx <- Mx ⊕ AC	
OR X (, B)	00101 0bbb xxx xxxx	AC <- Mx | AC	
ORM X (, B)	00101 1bbb xxx xxxx	AC, Mx <- Mx | AC	
AND X (, B)	00110 0bbb xxx xxxx	AC <- Mx & AC	
ANDM X (, B)	00110 1bbb xxx xxxx	AC, Mx <- Mx & AC	
SHR	11110 0000 000 0000	0 -> AC [3], AC[0] -> CY; AC shift right one bit	CY

1.2. Immediate Type

Mnemonic	Instruction Code	Function	Flag Change
ADI X, I	01000 iiii xxx xxxx	AC <- Mx + I	CY
ADIM X, I	01001 iiii xxx xxxx	AC, Mx <- Mx + I	CY
SBI X, I	01010 iiii xxx xxxx	AC <- Mx + -I +1	CY
SBIM X, I	01011 iiii xxx xxxx	AC, Mx <- Mx + -I +1	CY
EORIM X, I	01100 iiii xxx xxxx	AC, Mx <- Mx ⊕ I	
ORIM X, I	01101 iiii xxx xxxx	AC, Mx <- Mx | I	
ANDIM X, I	01110 iiii xxx xxxx	AC, Mx <- Mx & I	

1.3. Decimal Adjustment

Mnemonic	Instruction Code	Function	Flag Change
DAA X	11001 0110 xxx xxxx	AC, Mx <- Decimal adjust for add.	CY
DAS X	11001 1010 xxx xxxx	AC, Mx <- Decimal adjust for sub.	CY

2. Transfer Instruction

Mnemonic	Instruction Code	Function	Flag Change
LDA X (, B)	00111 0bbb xxx xxxx	AC <- Mx	
STA X (, B)	00111 1bbb xxx xxxx	Mx <- AC	
LDI X, I	01111 iiii xxx xxxx	AC, Mx <- I	

3. Control Instruction

Mnemonic	Instruction Code	Function	Flag Change
BAZ X	10010 xxxx xxx xxxx	PC <- X, if AC = 0	
BNZ X	10000 xxxx xxx xxxx	PC <- X, if AC $\neq$ 0	
BC X	10011 xxxx xxx xxxx	PC <- X, if CY = 1	
BNC X	10001 xxxx xxx xxxx	PC <- X, if CY $\neq$ 1	
BA0 X	10100 xxxx xxx xxxx	PC <- X, if AC (0) = 1	
BA1 X	10101 xxxx xxx xxxx	PC <- X, if AC (1) = 1	
BA2 X	10110 xxxx xxx xxxx	PC <- X, if AC (2) = 1	
BA3 X	10111 xxxx xxx xxxx	PC <- X, if AC (3) = 1	
CALL X	11000 xxxx xxx xxxx	ST <- CY, PC +1 PC <- X (Not include p)	
RTNW H, L	11010 000h hhh llll	PC <- ST; TBR <- hhhh, AC <- llll	
RTNI	11010 1000 000 0000	CY, PC <- ST	CY
HALT	11011 0000 000 0000		
STOP	11011 1000 000 0000		
JMP X	1110p xxxx xxx xxxx	PC <- X (Include p)	
TJMP	11110 1111 111 1111	PC <- (PC11-PC8) (TBR) (AC)	
NOP	11111 1111 111 1111	No Operation	

Where,

PC	Program counter	I	Immediate data
AC	Accumulator	$\oplus$	Logical exclusive OR
-AC	Complement of accumulator	|	Logical OR
CY	Carry flag	&	Logical AND
Mx	Data memory	bbb	RAM bank
P	ROM page		
ST	Stack	TBR	Table Branch Register

Electrical Characteristics

Absolute Maximum Ratings*

DC Supply Voltage . . . . . -0.3V to +7.0V

Input/Output Voltage . . . . . GND-0.3V to V_{DD} + 0.3V

Operating Ambient Temperature . . . . . -40℃ to +85℃

Storage Temperature . . . . . -55℃ to +125℃

***Comments**

Stresses exceed those listed under "**Absolute Maximum Ratings**" may cause permanent damage to this device. These are stress ratings only. Functional operation of this device at these or any other conditions above those indicated in the operational sections of this specification is not implied or intended. Exposure to the absolute maximum rating conditions for extended periods may affect device reliability.

DC Electrical Characteristics (V_{DD} = 2.4 - 5.5V, GND = 0V, T_A = 25℃, unless otherwise specified)

Parameter	Symbol	Min.	Typ. *	Max.	Unit	Condition
Operating Voltage	V_{DD}	4.5	5.0	5.5	V	30kHz ≤ f_{OSC} ≤ 10MHz
Operating Voltage	V_{DD}	2.4	5.0	5.5	V	30kHz ≤ f_{OSC} ≤ 4MHz
Operating Current	I_{OP}	-	3	4.5	mA	f_{OSC} = 10MHz All output pins unload, execute NOP instruction, WDT off, ADC disable, LVR off. V_{DD} = 5.0V
		-	2	3	mA	f_{OSC} = 4MHz All output pins unload, execute NOP instruction, WDT off, ADC disable, LVR off. V_{DD} = 5.0V
Stand by Current (HALT)	I_{SB1}	-	-	1.5	mA	f_{OSC} = 10MHz All output pins unload (HALT mode), WDT off, ADC disable, LVR off. V_{DD} = 5.0V
		-	-	1	mA	f_{OSC} = 4MHz All output pins unload (HALT mode), WDT off, ADC disable, LVR off. V_{DD} = 5.0V
Stand by Current (STOP)	I_{SB2}	-	-	1	μA	All output pins unload (STOP mode), WDT off, ADC disable, LVR off. V_{DD} = 5.0V
WDT Current	I_{WDT}	-	-	20	μA	All output pins unload (STOP mode), WDT on, ADC disable, LVR off, V_{DD} = 5.0V
Input Low Voltage	V_{IL1}	GND	-	0.3 X V_{DD}	V	I/O Ports
Input Low Voltage	V_{IL2}	GND	-	0.2 X V_{DD}	V	$\overline{\text{RESET}}$, T0, T1, OSCI
Input High Voltage	V_{IH1}	0.7 X V_{DD}	-	V_{DD}	V	I/O Ports
Input High Voltage	V_{IH2}	0.8 X V_{DD}	-	V_{DD}	V	$\overline{\text{RESET}}$, T0, T1, OSCI
Input Leakage Current	I_{IL}	-1	-	1	μA	Input pad, V_{IN} = V_{DD} or GND
Pull-high Resistor	R_{PH}	10	30	50	kΩ	V_{DD} = 5.0V, V_{IN} = GND
Output Leakage Current	I_{OL}	-1	-	1	μA	Open drain output, V_{DD} = 5.0V V_{OUT} = V_{DD} or GND
Output High Voltage	V_{OH}	V_{DD} - 0.7	-	-	V	I/O Ports, PWM0 & 1, I_{OH} = -10mA, V_{DD} = 5.0V
Output Low Voltage	V_{OL}	-	-	GND + 0.6	V	I/O Ports, PWM0 & 1, I_{OL} = 20mA, V_{DD} = 5.0V

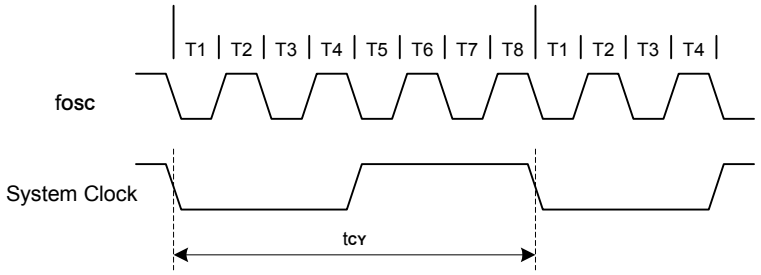
*: Data in "Typ." column is at 5.0V, 25℃, unless otherwise specified.
Maximum value of the supply current to V_{DD} is 100mA.
Maximum value of the output current from GND is 150mA.

AC Electrical Characteristics (V_{DD} = 2.4V - 5.5V, GND = 0V, T_A = 25°C, f_{OSC} = 30kHz - 10MHz, unless otherwise specified.)

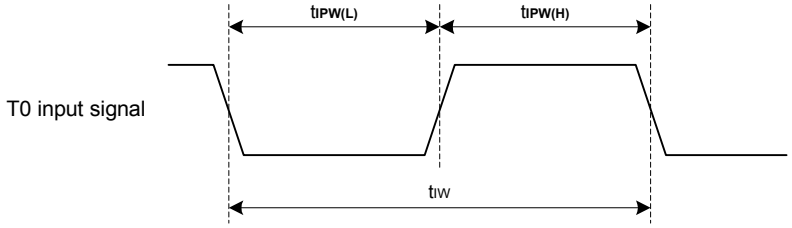
Parameter	Symbol	Min.	Typ.	Max.	Unit	Condition
RESET pulse width	t_{RESET}	10	-	-	μs	V_{DD} = 5.0V
WDT Period	t_{WDT}	1	-	-	ms	V_{DD} = 5.0V
Frequency Variation	|ΔF|/F	-	-	15	%	External RC Oscillator |F(5.0V) - F(2.4V)|/F(5.0V)
Internal RC Frequency Variation	f_{OSC}	3.80	4.00	4.20	MHz	V_{DD} =5V, T_A = 5°C - 45°C
Instruction cycle time	t_{CY}	0.4	-	133.4	μs	f_{OSC} = 30kHz - 10MHz
T0 input width	t_{IW}	(t_{CY} + 40)/N	-	-	ns	N = Prescaler divide ratio
Input pulse width	t_{IPW}	t_{IW}/2	-	-	ns	

Timing Waveform

(a) System Clock Timing Waveform



(b) T0 Input Waveform



ADC Converter Electrical Characteristics

(V_{DD} = 2.4V - 5.5V, GND = 0V, T_A = 25℃, f_{OSC} = 30kHz - 10MHz, unless otherwise specified.)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Condition
Resolution	NR	-	-	10	bit	GND ≤ V_{AIN} ≤ V_{REF}
Reference Voltage	V_{REF}	2.4	-	V_{DD}	V	
ADC Input Voltage	V_{AIN}	GND	-	V_{REF}	V	
ADC Input Resistor	R_{AIN}	2000	-	-	kΩ	V_{IN} = 5.0V
ADC conversion current	I_{AD}	-	500	1000	μA	ADC converter module operating, V_{DD} = 5.0V
Nonlinear Error	E_{NL}	-	-	±2	LSB	V_{REF} = V_{DD} = 5.0V
Full scale error	E_F	-	-	±1	LSB	V_{REF} = V_{DD} = 5.0V
Offset error	E_Z	-	-	±1	LSB	V_{REF} = V_{DD} = 5.0V
Total Absolute error	E_{AD}	-	±1	±2	LSB	V_{REF} = V_{DD} = 5.0V
ADC Clock Period	t_{AD}	1	-	33.4	μs	f_{OSC} = 30kHz - 10MHz
ADC Conversion Time	t_{CNV1}	-	204	-	t_{AD}	Set ADCS = 0
ADC Conversion Time	t_{CNV2}	-	780	-	t_{AD}	Set ADCS = 1

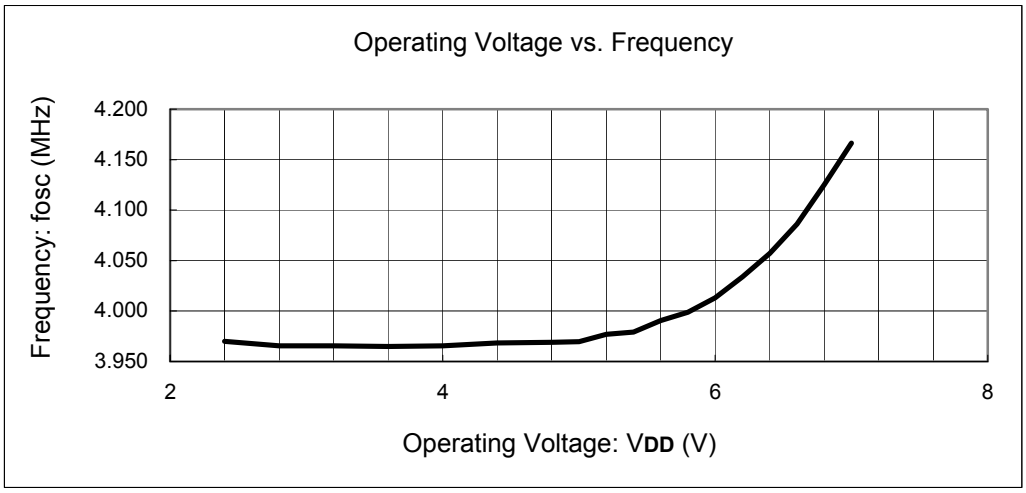
Low Voltage Reset Electrical Characteristics

(GND = 0V, T_A = 25℃, f_{OSC} = 32.768kHz - 10MHz, unless otherwise specified.)

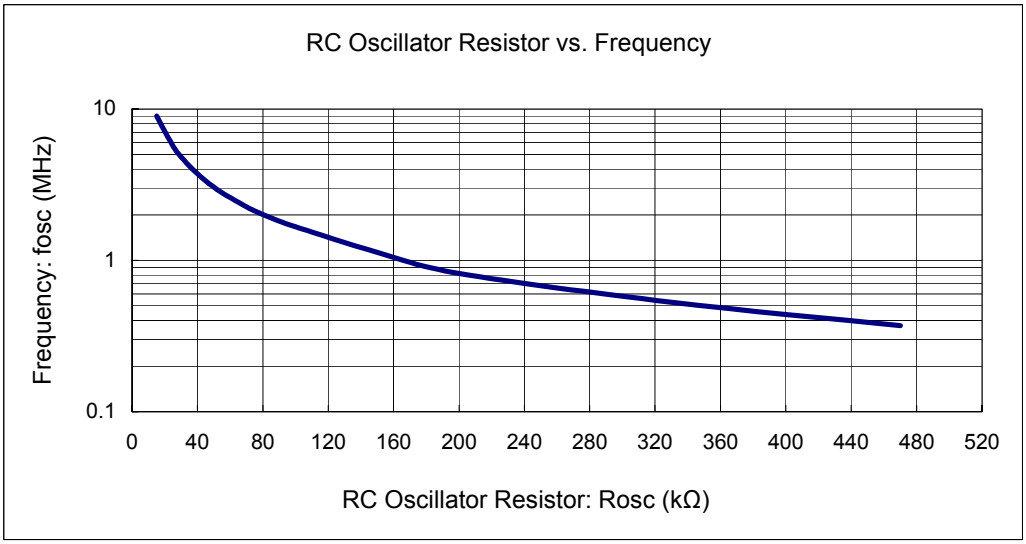
Parameter	Symbol	Min.	Typ.	Max.	Unit	Condition
LVR Voltage (1)	V_{LVR1}	3.8	-	4.2	V	LVR enable
LVR Voltage (2)	V_{LVR2}	2.3	-	2.7	V	LVR enable
LVR Voltage Pulse Width	t_{LVR}	500	-	-	μs	V_{DD} ≤ V_{LVR}

RC oscillator Characteristics Graphs (for reference only)

Internal RC Oscillator Characteristics Graphs (Operating Voltage vs. Frequency):

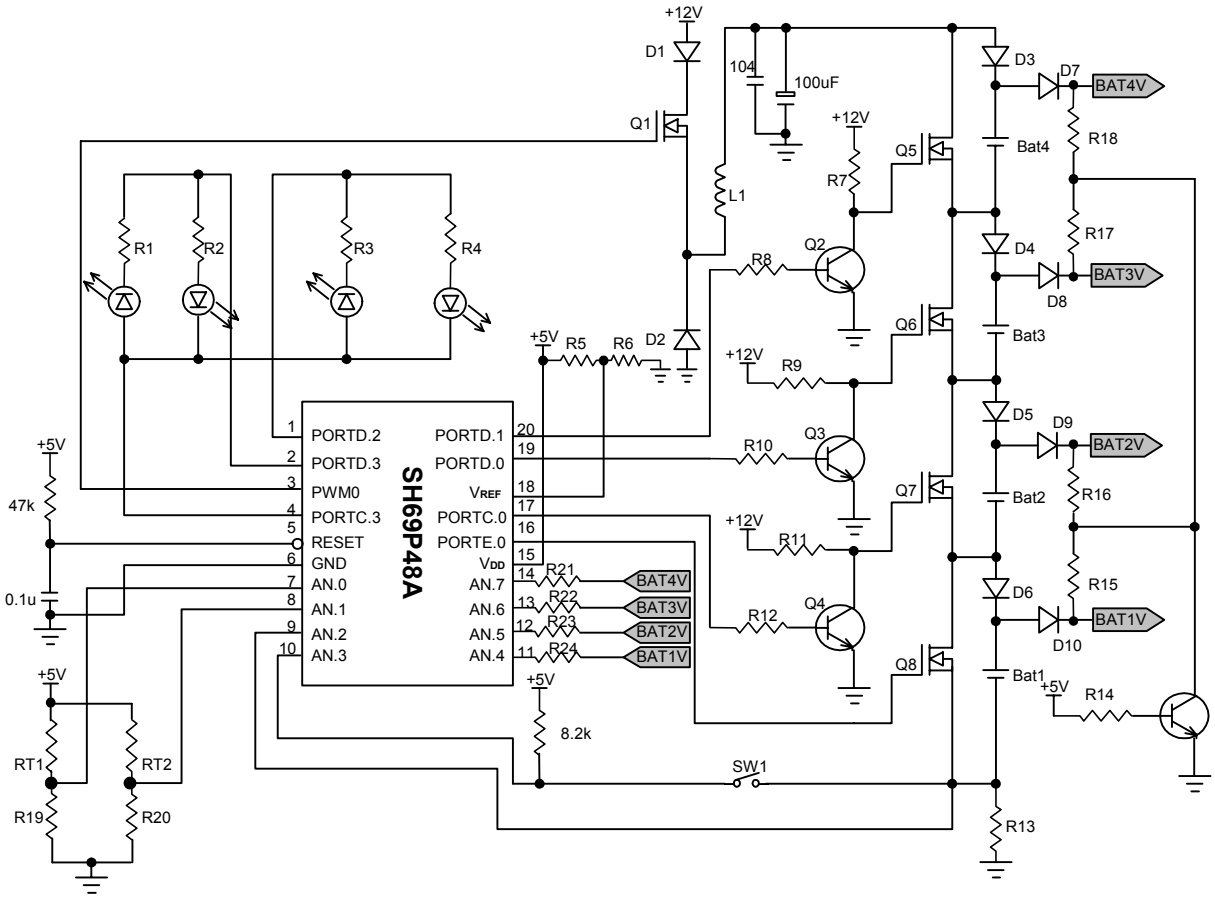


External RC Oscillator Characteristics Graphs (External Resistor vs. Frequency):

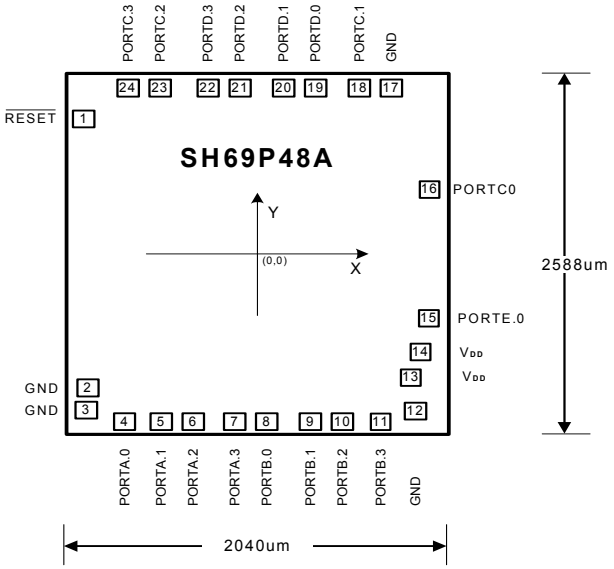


Application Circuits (For Reference Only):

(1) Operating voltage: 5.0V
(2) Oscillator: Internal RC 4MHz
(3) PORTA.0 - 1: Temperature analog input;
PORTA.2: Current analog input;
PORTA.3: Battery type analog input;
PORTB.0 - 3: Battery voltage analog input;
PORTD.0 - 1, PORTC.0, PORTE.0: Battery charging on/off output;
PORTC.1: External reference voltage input;
PORTC.2: Charging current control output;
PORTC.3, PORTD.2 - 3: LED display output



Bonding Diagram



Substratum connects to ground.

Pad Location unit: μm

Pad No.	Designation	X	Y	Pad No.	Designation	X	Y
1	$\overline{\text{RESET}}$	-880.55	992.6	13	VDD	763.4	-919.7
2	GND	-868.3	-1004.35	14	VDD	830.8	-790.85
3	GND	-886	-1126.1	15	PORTE.0	882.4	-596.8
4	PORTA.0	-714.45	-1158	16	PORTC.0	882.4	396.35
5	PORTA.1	-484.65	-1158	17	GND	683.8	1158
6	PORTA.2	-350.65	-1158	18	PORTC.1	538.35	1158
7	PORTA.3	-120.85	-1158	19	PORTD.0	307.45	1158
8	PORTB.0	13.15	-1158	20	PORTD.1	173.45	1158
9	PORTB.1	242.95	-1158	21	PORTD.2	-57.45	1158
10	PORTB.2	376.95	-1158	22	PORTD.3	-191.45	1158
11	PORTB.3	606.75	-1158	23	PORTC.2	-422.35	1158
12	GND	771.3	-1126.6	24	PORTC.3	-556.35	1158

Note:

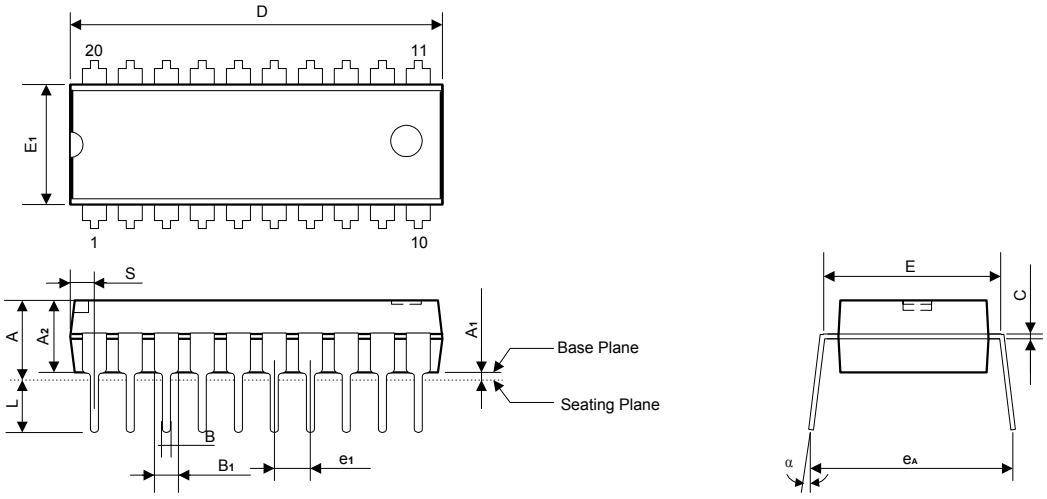
The all GND pins must be connected together outside the chip.

Ordering Information

Part No.	Package
SH69P48AH	Chip Form
SH69P48A/020DU	20L DIP
SH69P48AM/016MU	16L SOP
SH69P48AM/020MU	20L SOP

Package Information

P-DIP 20L Outline Dimensions unit: inches/mm

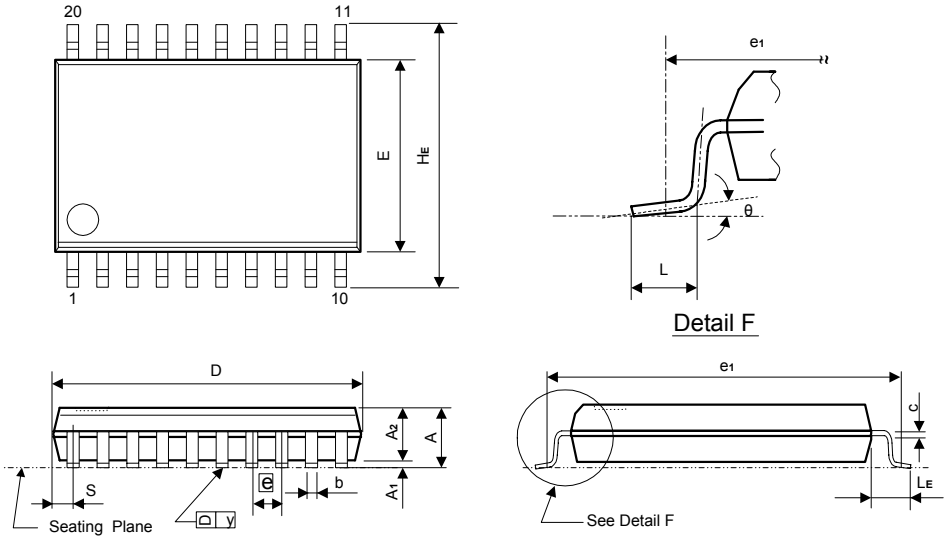


Symbol	Dimensions in inches	Dimensions in mm
A	0.175 Max.	4.45 Max.
A_1	0.010 Min.	0.25 Min.
A_2	0.138 ± 0.008	3.50 ± 0.20
B	0.018+0.004 -0.002	0.46+0.10 -0.05
B_1	0.060+0.004 -0.002	1.52+0.10 -0.05
C	0.010+0.004 -0.002	0.25+0.10 -0.05
D	1.026 Typ. (1.046 Max.)	26.06 Typ. (26.57 Max.)
E	0.300 ± 0.010	7.62 ± 0.25
E_1	0.250 Typ. (0.262 Max.)	6.35 Typ. (6.65 Max.)
e_1	0.100 Typ.	2.54 Typ.
L	0.130 ± 0.010	3.30 ± 0.25
α	0° - 15°	0° - 15°
e_A	0.345 ± 0.035	8.76 ± 0.89
S	0.078 Max.	1.98 Max.

Notes:

1. The maximum value of dimension D includes end flash.
2. Dimension E_1 does not include resin fins.
3. Dimension S includes end flash.

SOP 20L (W.B.) Outline Dimensions unit: inches/mm

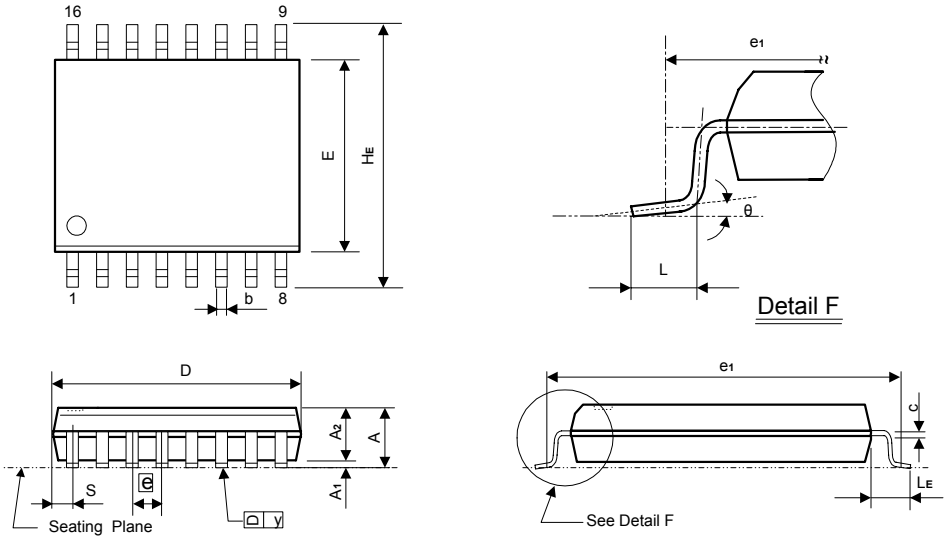


Symbol	Dimensions in inches	Dimensions in mm
A	0.106 Max.	2.69 Max.
A_1	0.004 Min.	0.10 Min.
A_2	0.092 ± 0.005	2.33 ± 0.13
b	0.016 +0.004 -0.002	0.41 +0.10 -0.05
C	0.010 +0.004 -0.002	0.25 +0.10 -0.05
D	0.500 ± 0.02	12.80 ± 0.51
E	0.295 ± 0.010	7.49 ± 0.25
e	0.050 ± 0.006	1.27 ± 0.15
e_1	0.376 NOM.	9.50 NOM.
H_E	0.406 ± 0.012	10.31 ± 0.31
L	0.032 ± 0.008	0.81 ± 0.20
L_E	0.055 ± 0.008	1.40 ± 0.20
S	0.042 Max.	1.07 Max.
y	0.004 Max.	0.10 Max.
θ	0° - 10°	0° - 10°

Notes:

1. The maximum value of dimension D includes end flash.
2. Dimension E does not include resin fins.
3. Dimension e_1 is for PC Board surface mount pad pitch design reference only.
4. Dimension S includes end flash.

SOP 16L (W.B.) Outline Dimensions unit: inches/mm



Symbol	Dimensions in inches	Dimensions in mm
A	0.175 Max.	2.79 Max.
A_1	0.004 Min.	0.10 Min.
A_2	0.092 ± 0.005	2.33 ± 0.13
b	0.016 +0.004 -0.002	0.41 +0.10 -0.05
C	0.010 +0.004 -0.002	0.25 +0.10 -0.05
D	0.400 ± 0.014	10.16 ± 0.36
E	0.295 ± 0.010	7.49 ± 0.25
e	0.050 ± 0.006	1.27 ± 0.15
e_1	0.376 NOM.	9.55 NOM.
H_E	0.406 ± 0.012	10.31 ± 0.31
L	0.030 ± 0.008	0.76 ± 0.20
L_E	0.055 ± 0.008	1.40 ± 0.20
S	0.033 Max.	0.84 Max.
y	0.004 Max.	0.10 Max.
θ	0° - 10°	0° - 10°

Notes:

1. The maximum value of dimension D includes end flash.
2. Dimension E does not include resin fins.
3. Dimension e_1 is for PC Board surface mount pad pitch design reference only.
4. Dimension S includes end flash.

Data Sheet Revision History

Version	Content	Date
2.1	Package Information update	Sep. 2008
2.0	Update Ordering Information	Mar. 2008
1.0	Original	Dec. 2007