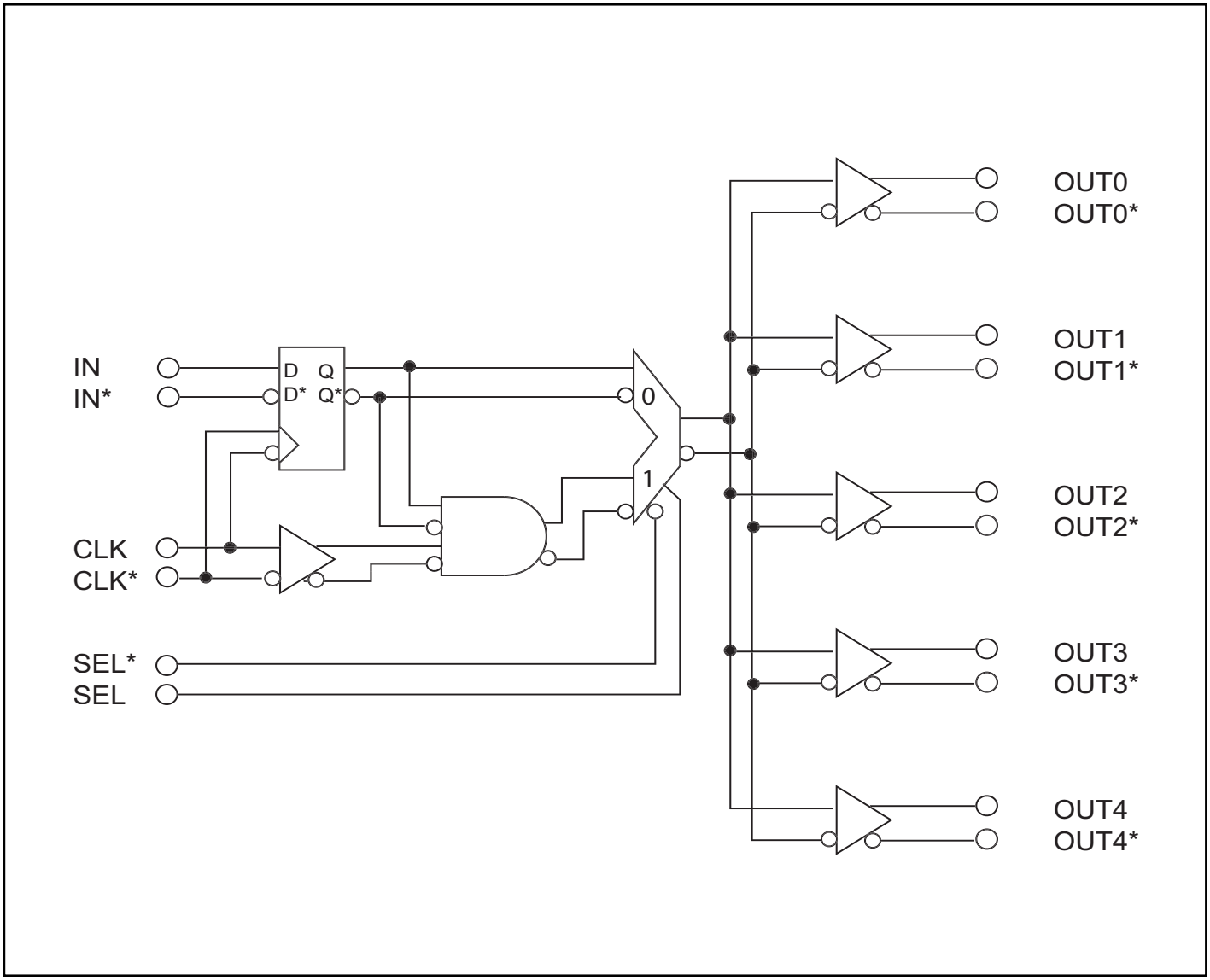
SK15XX Family Functional Block Diagram



SK15XX Family Product Selection Guide

1:5 Signal Distribution	*3 GHz*	*Synch / Asynch Operation*

Logic Family

	Power Supply		Output Configuration				Output	Availability
Product	3.3V	5.5V	Open Emitter	50Ω Double Termination	50Ω Source Termination	Internal Current Sink (Double Termination)		
SK1500	●	●	●				ECL / PECL	Now
SK1501		●	●				Double Swing	Now
SK1502	●	●		●			ECL / PECL	Now
SK1503	●	●				●	ECL / PECL	Now
SK1504	●	●			●		ECL / PECL	Now

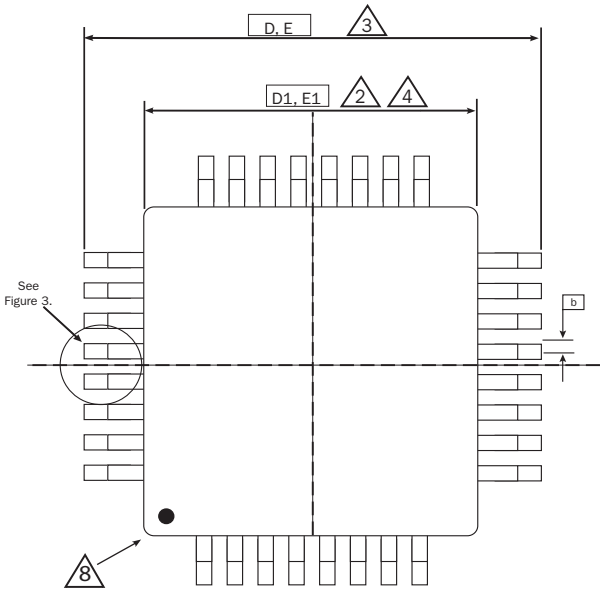
Logic / Translation Family

	Translation	Output Configuration			Availability
Product		Open Emitter	50Ω Double Termination	50Ω Source Termination	
SK1525	Anything to PECL	●			Now
SK1526	Anything to ECL	●			Now
SK1527	Anything to PECL		●		Now
SK1528	Anything to ECL		●		Now
SK1529	Anything to PECL			●	Now
SK1530	Anything to ECL			●	Now

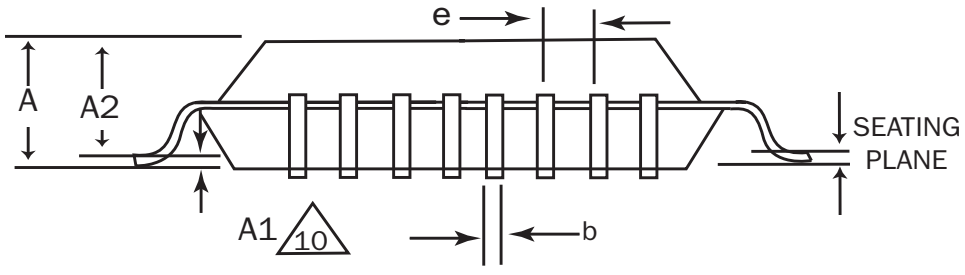
Open Collector Logic Family

	Output Configuration	**Output Current**	**Availability**
Product	Open Collector		
SK1599	●	12 mA	Now

SK15XX Family Package Information
5mm x 5mm TQFP



Top View



Side View

SK15XX Family Package Information (continued)
5mm x 5mm TQFP

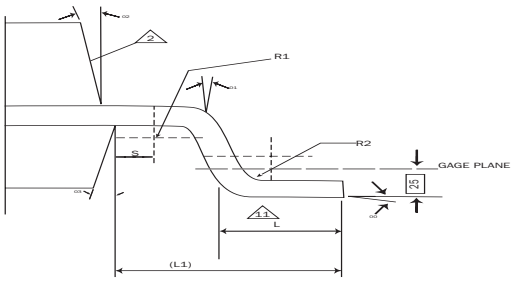


Figure 1.

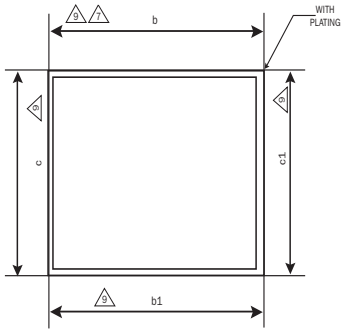


Figure 2.

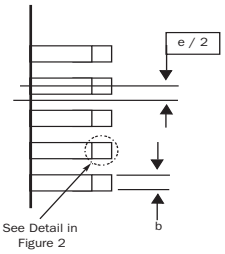


Figure 3.

1. All dimensions and tolerancing conforms to ANSI Y14.5M-1982.
2. The top package body size may be smaller than the bottom package body size by as much as 0.15 mm.
3. To be determined at seating plane.
4. Dimensions D1 and E1 do not include mold protrusion. Allowable protrusion is 0.25 mm per side. D1 and E1 are maximum plastic body size dimensions including mold mismatch.
5. Details of Pin 1 identifier optional, but must be located within the zone indicated.
6. All dimensions are in millimeters.
7. Dimension b does not include Dambar protrusion. Allowable Dambar protrusion shall not cause the lead width to exceed the maximum b dimension by more than 0.08 mm. Dambar cannot be located on the lower radius or the foot. Minimum space between protrusion and an adjacent lead is 0.07 mm for 0.4 mm and 0.5 mm pitch packages.
8. Exact shape of each corner is optional.
9. These dimensions apply to the flat section of the lead between 0.10 mm and 0.25 mm from the lead tip.
10. A1 is defined as the distance from the seating plane to the lowest point of the package body.

JEDEC Variation All Dimensions in Millimeters					
Symbol	MIN	NOM	MAX	Note	Comments
A	1.00	1.10	1.20		Package Stand Off Height
A1	0.05	0.10	0.15		Air Gap
A2	0.95	1.00	1.05		Package Body Thickness
D		7.00 BSC		3	
D1		5.00 BSC		4, 2	Package Body Length
E		7.00 BSC		3	
E1		5.00 BSC		4, 2	Package Body Width
N		32			Lead Count
e		0.50 BSC			Lead Pitch
b	0.17	0.22	0.27	7	Lead Thickness
b1	0.17	0.20	0.23		
R1	0.08	–	–		
R2	0.08	–	0.20		
00	0°	3.5°	7°		
01	0°	–	–		
02	11°	12°	13°		
03	11°	12°	13°		
S	0.20	–	–		
c	0.09	–	0.20		
c1	0.09	–	0.16		
L	0.45	0.60	0.75		
L1		1.00 REF			
aaa		0.20			
bbb		0.20			
ccc		0.08			
ddd		0.08			

Absolute Maximum Ratings*

Symbol	Parameter	Value	Unit
V_{EE}	Power Supply (V_{CC} = 0V)	-8.0 to 0	V
V_{CC}	Power Supply (V_{EE} = 0V)	+8.0 to 0	V
V_I	Input Voltage	VCC ≥ VI ≥ VEE	V
I_{OUT}	Output Current Continuous Surge	 50 100	 mA mA
T_{stg}	Storage Temperature	-65 to +150	^oC
T_{sol}	Solder Temperature (<2 to 3 seconds: 245^oC desired)	265	^oC

* Maximum Ratings are those values beyond which damage to the device may occur.

Note:

1. Device is ESD sensitive and requires protective handling.

Description

The SK1500 is an extremely fast, stable, and accurate low skew 1:5 clock / signal distributor featuring a synchronous enable, which allows the outputs to be turned off and on without the risk of an unpredictable output pulse. The D - flip-flop is triggered on the falling edge of the clock.

The SK1500 uses standard open emitter ECL outputs optimized for:

- General purpose ECL compatible applications
- Multiple destination applications (daisy chain).

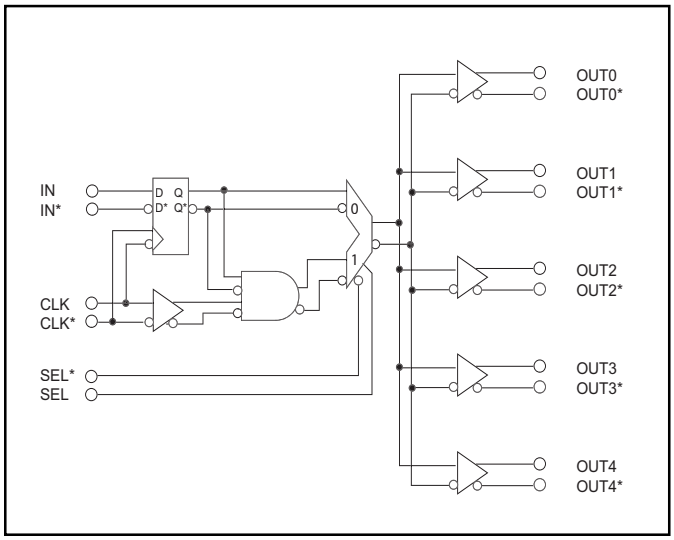
Features

- 1:5 Clock/Data Driver
- 3 GHz Fmax
- 3.3V / 5.5V Compatible
- Available in 32 pin, 5mm X5mm, TQFP Package

Application Notes

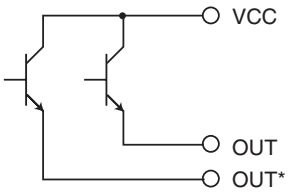
AN1001 - EPIC Family Product Line
AN1003 - Termination Techniques for ECL / LVECL PECL / LVPECL Devices
AN1004 - Interfacing Between LVDS and ECL / LVECL / PECL / LVPECL

Functional Block Diagram

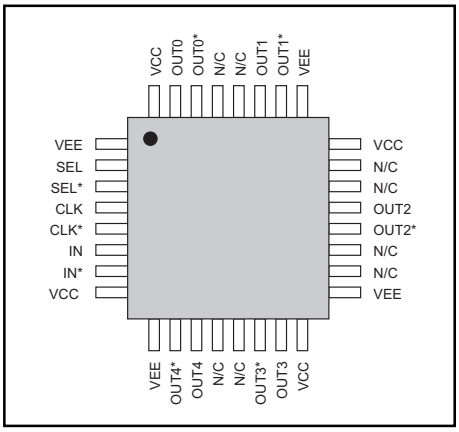


Output Option

Open Emitter



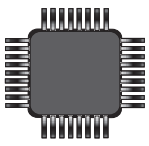
Pin Description



Package Information

32 pin, 5 mm X 5 mm

TQFP Package



DC Characteristics

(V_{CC} - V_{EE} = 3.0V to 5.5V; T_A = 0°C to 70°C)

Parameter	Symbol	Min	Typ	Max	Units
Inputs					
Input High Input Low	VIH VIL	VEE + 2.0 VEE		VCC VCC - 0.2	V V
(IN - IN*, CLK - CLK*, SEL - SEL*) Differential Input Voltage	| VIH - VIL |	0.2		4.3	V
Timing Inputs (CLK / CLK*) Input High Current Input Low Current	 IIH IIL	 -5 -6		 +30 +6	 µA µA
Functional Inputs (IN / IN*, SEL / SEL*) Input Current	IIH, IIL	-500		+500	µA
Outputs					
Digital Output Voltage Output Common Mode Range	| OUT - OUT* | (OUT + OUT*) / 2	600 VCC - 1.5	700 VCC - 1.3	 VCC - 1.1	mV V
Power Supply					
Power Supply Current	IEE			132	mA

Test Conditions: Outputs terminated with 50Ω to VCC – 2V.

AC Characteristics

(V_{CC} - V_{EE} = 3.0V to 5.5V; T_A = 0°C to 70°C)

Parameter	Symbol	Min	Typ	Max	Units
High Performance Option					
Propagation Delay CLK to OUT (SEL = 0) CLK to OUT (SEL = 1) SEL to OUT	 Tpd Tpd Tpd	 485 300 300	 630 450 450	 785 600 600	 ps ps ps
Channel to Channel Skew	t_{SKEW}			20	ps
Maximum Operating Frequency (Note 1)	Fmax	3.0			GHz
Minimum Pulse Width (Note 1)	PW min	250			ps
IN to CLK Set Up Time Hold Time	 Ts Th	 100 100			 ps ps
Output Rise and Fall Times (20% / 80%) (Note 1)	Tr / Tf		125	175	ps
Temperature Coefficient (Note 1)	ΔTpd /ΔT		<1		ps / °C

AC TEST CONDITIONS: Outputs terminated with 50Ω to VCC - 2.0V

Note 1: Guaranteed by characterization. Not production tested.

Description

The SK1501 is an extremely fast, stable, and accurate low skew 1:5 clock / signal distributor featuring a synchronous enable, which allows the outputs to be turned off and on without the risk of an unpredictable output pulse. The D - flip-flop is triggered on the falling edge of the clock.

The SK1501 uses open emitter outputs with a double amplitude swing suitable for the following applications:

- Double termination situations that require a full swing at the destination
- Long cables

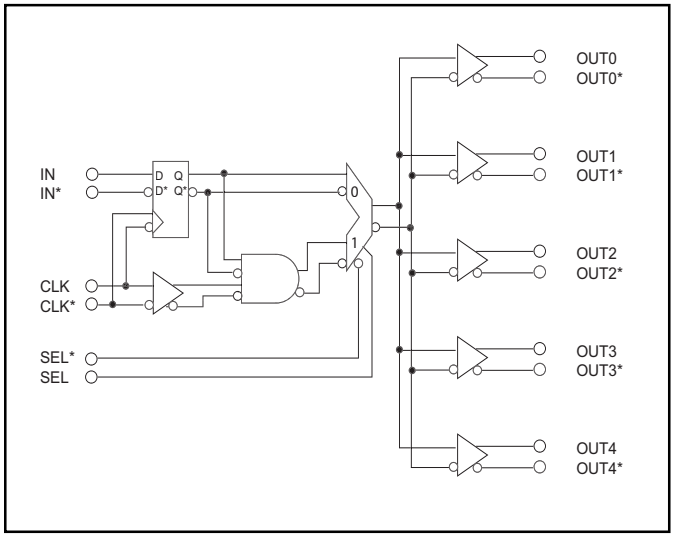
Features

- 1:5 Clock/Data Driver
- 2 GHz Fmax
- 4.2V / 5.5V Compatible
- Available in 32 pin, 5mm X5mm, TQFP Package

Application Notes

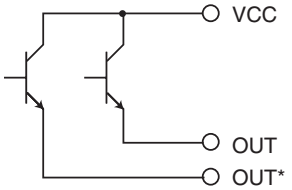
AN1001 - EPIC Family Product Line
AN1003 - Termination Techniques for ECL / LVECL PECL / LVPECL Devices
AN1004 - Interfacing Between LVDS and ECL / LVECL / PECL / LVPECL

Functional Block Diagram

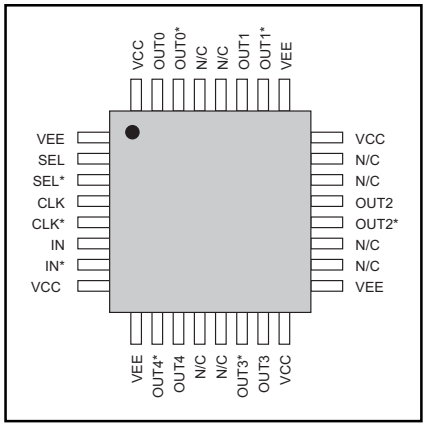


Output Option

Open Emitter



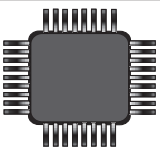
Pin Description



Package Information

32 pin, 5 mm X 5 mm

TQFP Package



DC Characteristics

(V_{CC} - V_{EE} = 4.2V to 5.5V; T_A = 0°C to 70°C)

Parameter	Symbol	Min	Typ	Max	Units
Inputs					
Input High Input Low	VIH VIL	VEE + 2.0 VEE		VCC VCC -0.2	V V
(IN - IN*, CLK - CLK*, SEL -SEL*) Differential Input Voltage	| VIH - VIL |	0.2		4.3	V
Timing Inputs (CLK / CLK*) Input High Current Input Low Current	 IIH IIL	 -5 -6		 +30 +6	 µA µA
Functional Inputs (IN / IN*, SEL / SEL*) Input Current	IIH, IIL	-500		+500	µA
Outputs					
Digital Output Voltage Output Common Mode Range	| OUT -OUT* | (OUT + OUT*) / 2	1.2 VCC -2.2	1.4 VCC - 1.9	 VCC - 1.7	V V
Power Supply					
Power Supply Current	IEE			132	mA

Test Conditions: Outputs terminated with 50Ω to VCC – 3.3V.

AC Characteristics

(V_{CC} - V_{EE} = 4.2V to 5.5V; T_A = 0°C to 70°C)

Parameter	Symbol	Min	Typ	Max	Units
High Performance Option					
Propagation Delay CLK to OUT (SEL = 0) CLK to OUT (SEL = 1) SEL to OUT	 Tpd Tpd Tpd	 500 400 350	 760 650 625	 1020 900 900	 ps ps ps
Channel to Channel Skew	t_{SKEW}			100	ps
Maximum Operating Frequency (Note 1)	Fmax	2.0			GHz
Minimum Pulse Width (Note 1)	PW min	350			ps
IN to CLK Set Up Time Hold Time	 Ts Th	 100 100			 ps ps
Output Rise and Fall Times (20% / 80%) (Note 1)	Tr / Tf		200	475	ps
Temperature Coefficient (Note 1)	ΔTpd /ΔT		<3		ps / °C

AC TEST CONDITIONS: Outputs terminated with 50Ω to VCC – 3.3V.

Note 1: Guaranteed by characterization. Not production tested.

Description

The SK1502 is an extremely fast, stable, and accurate low skew 1:5 clock / signal distributor featuring a synchronous enable, which allows the outputs to be turned off and on without the risk of an unpredictable output pulse. The D - flip-flop is triggered on the falling edge of the clock.

The SK1502 uses 50Ω outputs with source /sink capability, and is optimized for applications that require:

- Point to point, double terminated, timing critical lines

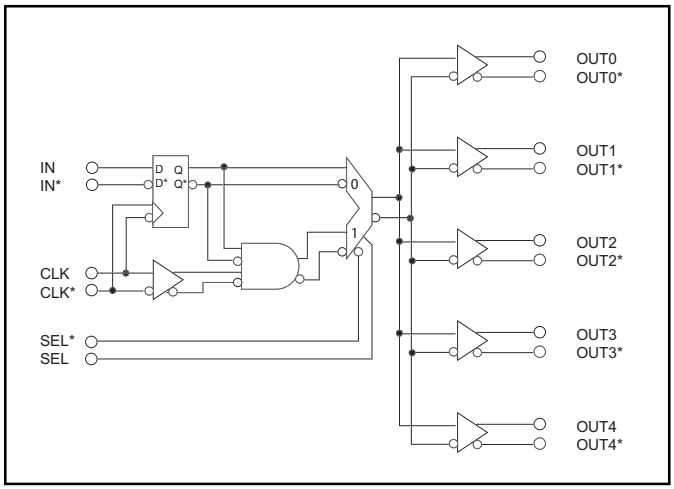
Features

- 1:5 Clock/Data Driver
- 3 GHz Fmax
- 3.3V / 5.5V Compatible
- Available in 32 pin, 5mm X5mm, TQFP Package

Application Notes

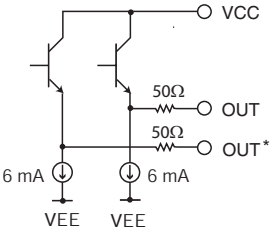
AN1001 - EPIC Family Product Line
AN1003 - Termination Techniques for ECL / LVECL PECL / LVPECL Devices
AN1004 - Interfacing Between LVDS and ECL / LVECL / PECL / LVPECL

Functional Block Diagram

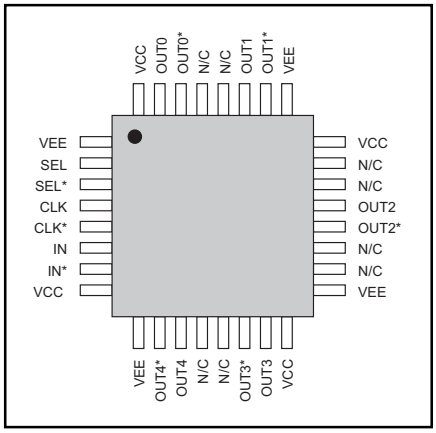


Output Option

50Ω Source / Sink



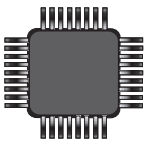
Pin Description



Package Information

32 pin, 5 mm X 5 mm

TQFP Package



DC Characteristics

(V_{CC} - V_{EE} = 3.0V to 5.5V; T_A = 0°C to 70°C)

Parameter	Symbol	Min	Typ	Max	Units
Inputs					
Input High Input Low	VIH VIL	VEE + 2.0 VEE		VCC VCC - 0.2	V V
(IN - IN*, CLK - CLK*, SEL - SEL*) Differential Input Voltage	| VIH - VIL |	0.2		4.3	V
Timing Inputs (CLK / CLK*) Input High Current Input Low Current	 IIH IIL	 -5 -6		 +30 +6	 µA µA
Functional Inputs (IN / IN*, SEL / SEL*) Input Current	 IIH, IIL	 -500		 +500	 µA
Outputs					
Digital Output Voltage Output Common Mode Range Internal Current Source Output Impedance	| OUT - OUT* | (OUT + OUT*) / 2 ISINK ROUT	600 VCC - 1.4 4 40	700 VCC -1.2 6 50	 VCC - 1.0 7.5 60	mV V mA Ω
Power Supply					
Power Supply Current	IEE			240	mA

Test Conditions: Outputs unterminated.

AC Characteristics

(V_{CC} - V_{EE} = 3.0V to 5.5V; T_A = 0°C to 70°C)

Parameter	Symbol	Min	Typ	Max	Units
High Performance Option					
Propagation Delay CLK to OUT (SEL = 0) CLK to OUT (SEL = 1) SEL to OUT	 Tpd Tpd Tpd	 485 300 300	 630 450 450	 785 600 600	 ps ps ps
Channel to Channel Skew	t_{SKEW}			20	ps
Maximum Operating Frequency (Note 1)	Fmax	3.0			GHz
Minimum Pulse Width (Note 1)	PW min	250			ps
IN to CLK Set Up Time Hold Time	 Ts Th	 100 100			 ps ps
Output Rise and Fall Times (20% / 80%)(Note 1)	Tr / Tf		125	175	ps
Temperature Coefficient(Note 1)	ΔTpd /ΔT		<1		ps / °C

AC TEST CONDITIONS: Outputs terminated with 50Ω to VCC -2.0V.

Note 1: Guaranteed by characterization. Not production tested.

Description

The SK1503 is an extremely fast, stable, and accurate low skew 1:5 clock / signal distributor featuring a synchronous enable, which allows the outputs to be turned off and on without the risk of an unpredictable output pulse. The D - flip-flop is triggered on the falling edge of the clock.

The SK1503 outputs are open emitter with an internal current source, optimized for applications that are:

- Point to point, double terminated, timing critical lines
- Non-50Ω transmission lines

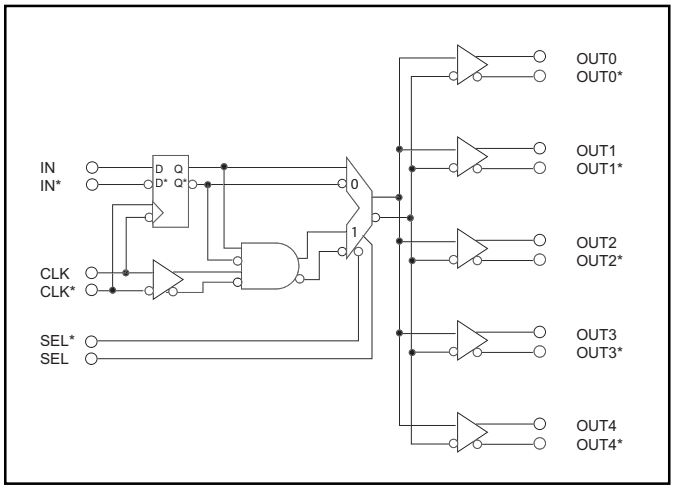
Features

- 1:5 Clock/Data Driver
- 3 GHz Fmax
- 3.0V / 5.5V Compatible
- Available in 32 pin, 5mm X5mm, TQFP Package

Application Notes

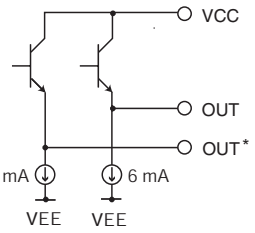
AN1001 - EPIC Family Product Line
AN1003 - Termination Techniques for ECL / LVECL PECL / LVPECL Devices
AN1004 - Interfacing Between LVDS and ECL / LVECL / PECL / LVPECL

Functional Block Diagram

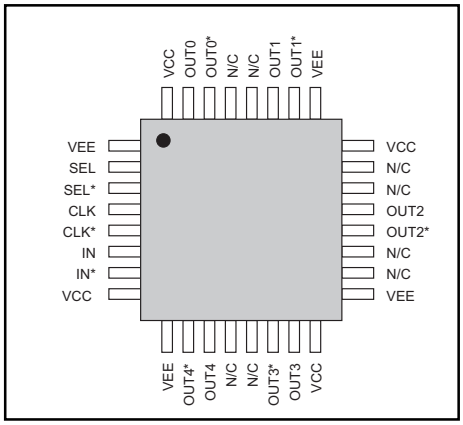


Output Option

Internal Current Sink



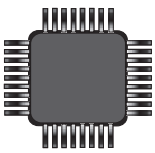
Pin Description



Package Information

32 pin, 5 mm X 5 mm

TQFP Package



DC Characteristics

(V_{CC} - V_{EE} = 3.0V to 5.5V; T_A = 0°C to 70°C)

Parameter	Symbol	Min	Typ	Max	Units
Inputs					
Input High Input Low	VIH VIL	VEE + 2.0 VEE		VCC VCC - 0.2	V V
(IN - IN*, CLK - CLK*, SEL - SEL*) Differential Input Voltage	| VIH - VIL |	0.2		4.3	V
Timing Inputs (CLK / CLK*) Input High Current Input Low Current	 IIH IIL	 -5 -6		 +30 +6	 µA µA
Functional Inputs (IN / IN*, SEL / SEL*) Input Current	IIH, IIL	-500		+500	µA
Outputs					
Digital Output Voltage Output Common Mode Range Internal Current Source	| OUT - OUT* | (OUT + OUT*) / 2 ISINK	600 VCC - 1.5 4	700 VCC -1.3 6	 VCC - 1.1 7.5	mV V mA
Power Supply					
Power Supply Current	IEE			240	mA

Test Conditions: Outputs unterminated.

AC Characteristics

(V_{CC} - V_{EE} = 3.0V to 5.5V; T_A = 0°C to 70°C)

Parameter	Symbol	Min	Typ	Max	Units
High Performance Option					
Propagation Delay CLK to OUT (SEL = 0) CLK to OUT (SEL = 1) SEL to OUT	 Tpd Tpd Tpd	 485 300 300	 630 450 450	 785 600 600	 ps ps ps
Channel to Channel Skew	t_{SKEW}			20	ps
Maximum Operating Frequency (Note 1)	Fmax	3.0			GHz
Minimum Pulse Width (Note 1)	PW min	250			ps
IN to CLK Set Up Time Hold Time	 Ts Th	 100 100			 ps ps
Output Rise and Fall Times (20% / 80%) (Note 1)	Tr / Tf		125	175	ps
Temperature Coefficient (Note 1)	ΔTpd /ΔT		<1		ps / °C

AC TEST CONDITIONS: Outputs terminated with 50Ω to VCC -2.0V.

Note 1: Guaranteed by characterization. Not production tested.

Description

The SK1504 is an extremely fast, stable, and accurate low skew 1:5 clock / signal distributor featuring a synchronous enable, which allows the outputs to be turned off and on without the risk of an unpredictable output pulse. The D - flip-flop is triggered on the falling edge of the clock.

The SK1504 outputs are 50Ω with source and sink capability, optimized for:

- Point to point, series terminated, timing critical lines

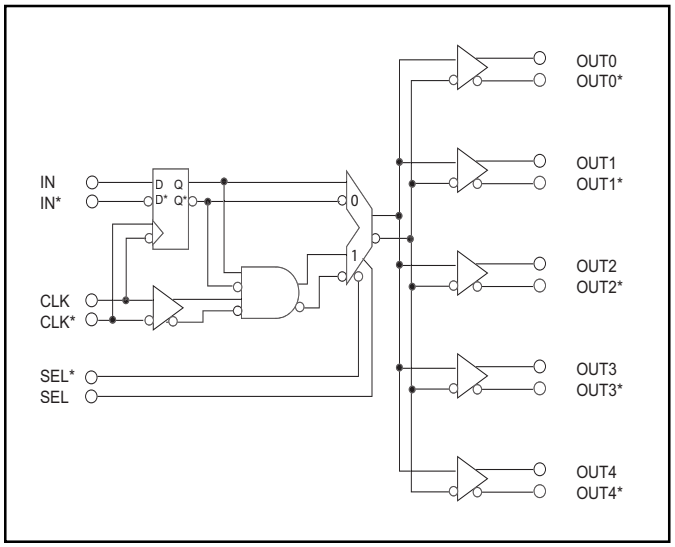
Features

- 1:5 Clock/Data Driver
- 3 GHz Fmax
- 3.3V / 5.5V Compatibles
- Available in 32 pin, 5mm X5mm, TQFP Package

Application Notes

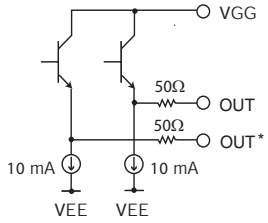
AN1001 - EPIC Family Product Line
AN1003 - Termination Techniques for ECL / LVECL PECL / LVPECL Devices
AN1004 - Interfacing Between LVDS and ECL / LVECL / PECL / LVPECL

Functional Block Diagram

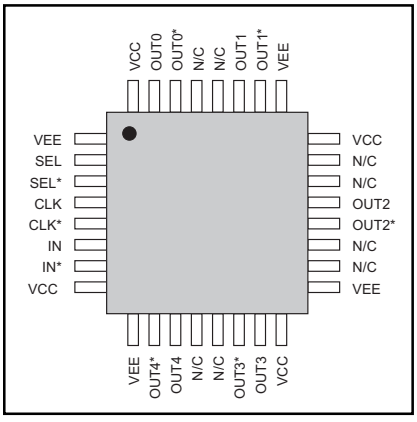


Output Option

50Ω Source / Sink



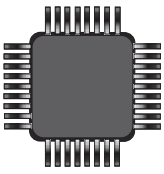
Pin Description



Package Information

32 pin, 5 mm X 5 mm

TQFP Package



DC Characteristics

(V_{CC} - V_{EE} = 3.0V to 5.5V; T_A = 0°C to 70°C)

Parameter	Symbol	Min	Typ	Max	Units
Inputs					
Input High Input Low	VIH VIL	VEE + 2.0 VEE		VCC VCC -0.2	V V
(IN - IN*, CLK - CLK*, SEL - SEL*) Differential Input Voltage	| VIH - VIL |	0.2		4.3	V
Timing Inputs (CLK / CLK*) Input High Current Input Low Current	 IIH IIL	 -5 -6		 +30 +6	 µA µA
Functional Inputs (IN / IN*, SEL / SEL*) Input Current	IIH, IIL	-500		+500	µA
Outputs					
Digital Output Voltage Output Common Mode Range Internal Current Source Output Impedance	| OUT - OUT* | (OUT + OUT*) / 2 ISINK ROUT	600 VCC - 1.4 7.5 40	700 VCC -1.2 10 50	 VCC - 1.0 13 60	mV V mA Ω
Power Supply					
Power Supply Current	IEE			240	mA

Test Conditions: Outputs unterminated.

AC Characteristics

(V_{CC} - V_{EE} = 3.0V to 5.5V; T_A = 0°C to 70°C)

Parameter	Symbol	Min	Typ	Max	Units
High Performance Option					
Propagation Delay CLK to OUT (SEL = 0) CLK to OUT (SEL = 1) SEL to OUT	 Tpd Tpd Tpd	 485 300 300	 630 450 450	 785 600 600	 ps ps ps
Channel to Channel Skew	t_{SKEW}			20	ps
Maximum Operating Frequency (Note 1)	Fmax	3.0			GHz
Minimum Pulse Width (Note 1)	PW min	250			ps
IN to CLK Set Up Time Hold Time	 Ts Th	 100 100			 ps ps
Output Rise and Fall Times (20% / 80%)(Note 1)	Tr / Tf		125	175	ps
Temperature Coefficient(Note 1)	ΔTpd /ΔT		<1		ps / °C

AC TEST CONDITIONS: Outputs terminated with 50Ω to VCC -2.0V.

Note 1: Guaranteed by characterization. Not production tested.

Description

The SK1525 is an extremely fast, stable, and accurate low skew 1:5 clock / signal distributor featuring a synchronous enable, which allows the outputs to be turned off and on without the risk of an upredictable output pulse. It is also capable of receiving inputs of any technology or voltage level. The D - flip-flop is triggered on the falling edge of the clock.

The SK1525 has open emitter PECL outputs.

Target applications:

- High speed clock / data lines that require translation
- Multiple destination (daisy chain) applications

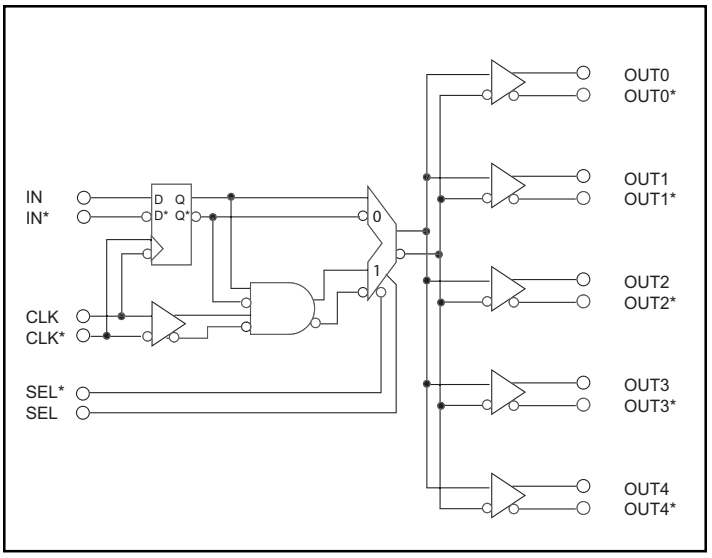
Features

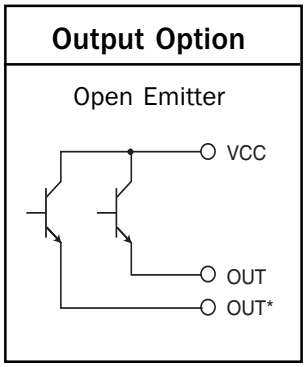
- 1:5 Clock/Data Driver
- 3 GHz Fmax
- Available in 32 pin, 5mm X5mm, TQFP Package

Application Notes

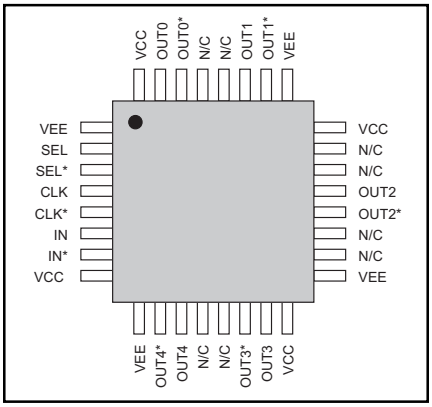
AN1001 - EPIC Family Product Line
AN1003 - Termination Techniques for ECL / LVECL PECL / LVPECL Devices
AN1004 - Interfacing Between LVDS and ECL / LVECL / PECL / LVPECL

Functional Block Diagram

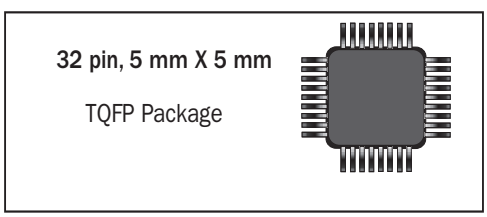




Pin Description



Package Information



DC Characteristics

(V_{CC}= 3.0V to 3.6V; V_{EE} = -3.6V to -3.0V; T_A = 0°C to 70°C)

Parameter	Symbol	Min	Typ	Max	Units
Inputs					
Input High Input Low	VIH VIL	VEE + 2.0 VEE		VCC VCC -0.2	V V
(IN - IN*, CLK - CLK*, SEL -SEL*) Differential Input Voltage	| VIH - VIL |	0.2		4.3	V
Timing Inputs (CLK / CLK*) Input High Current Input Low Current	 IIH IIL	 -5 -6		 +30 +6	 µA µA
Functional Inputs (IN / IN*, SEL / SEL*) Input Current	IIH, IIL	-500		+500	µA
Outputs					
Digital Output Voltage Output Common Mode Range	| OUT -OUT* | (OUT + OUT*) / 2	600 VCC -1.5	700 VCC -1.3	 VCC -1.1	mV V
Power Supply					
Power Supply Current	IEE			132	mA

Test Conditions: Outputs terminated with 50Ω to VCC – 2V.

AC Characteristics

(V_{CC} = 3.0V to 3.6V; V_{EE} = - 3.6V to - 3.0V; T_A = 0°C to 70°C)

Parameter	Symbol	Min	Typ	Max	Units
High Performance Option					
Propagation Delay CLK to OUT (SEL = 0) CLK to OUT (SEL = 1) SEL to OUT	 Tpd Tpd Tpd	 485 300 300	 630 450 450	 785 600 600	 ps ps ps
Channel to Channel Skew	t_{SKEW}			35	ps
Maximum Operating Frequency (Note 1)	Fmax	3.0			GHz
Minimum Pulse Width (Note 1)	PW min	250			ps
IN to CLK Set Up Time Hold Time	 Ts Th	 100 100			 ps ps
Output Rise and Fall Times (20% / 80%) (Note 1)	Tr / Tf		125	175	ps
Temperature Coefficient (Note 1)	ΔTpd /ΔT		<1		ps / °C

AC TEST CONDITIONS: Outputs terminated with 50Ω to VCC -2.0V.

Note 1: Guaranteed by characterization. Not production tested.

Description

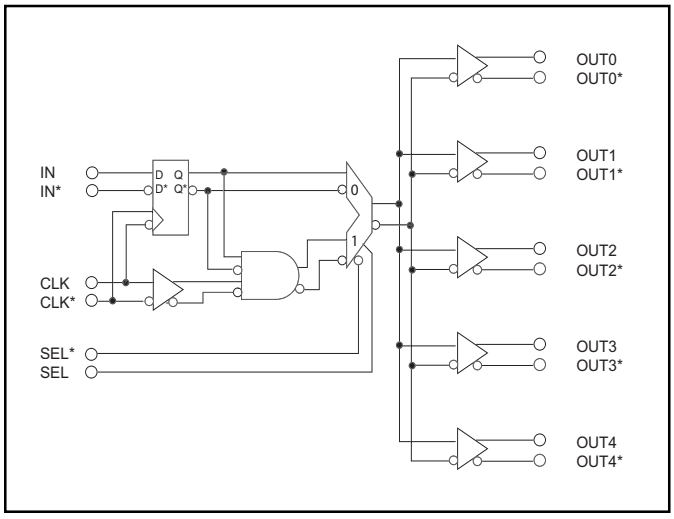
The SK1526 is an extremely fast, stable and accurate low skew 1:5 clock / signal distributor featuring a synchronous enable, which allows the outputs to be turned off and on without the risk of an upredictable output pulse. It is also capable of receiving inputs of any technology or voltage level. The D - flip-flop is triggered on the falling edge of the clock.

The SK1526 has standard open emitter ECL outputs.

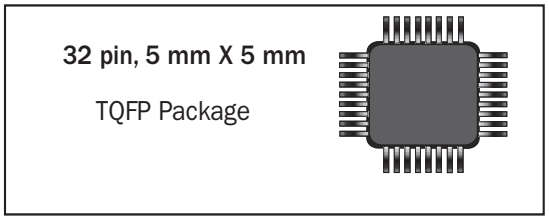
Target applications:

- High speed clock / data lines that require translation
- Multiple destination (daisy chain) applications

Functional Block Diagram



Package Information

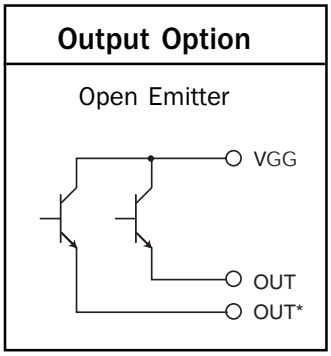


Features

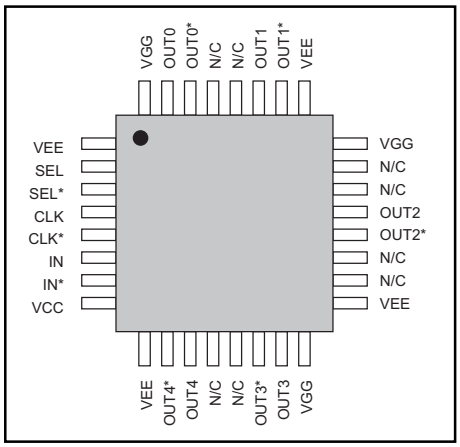
- 1:5 Clock/Data Driver
- 3 GHz Fmax
- Anything to ECL Translation
- Available in 32 pin, 5mm X5mm, TQFP Package

Application Notes

AN1001 - EPIC Family Product Line
AN1003 - Termination Techniques for ECL / LVECL PECL / LVPECL Devices
AN1004 - Interfacing Between LVDS and ECL / LVECL / PECL / LVPECL



Pin Description



DC Characteristics

(V_{GG} = - 0.1V to 2.0V; V_{CC} = 2.0V to 3.6V; VEE = -3.6V to -3.0V; T_A = 0°C to 70°C)

Parameter	Symbol	Min	Typ	Max	Units
Inputs					
Input High Input Low	VIH VIL	VEE + 2.0 VEE		VCC VCC -0.2	V V
(IN - IN*, CLK - CLK*, SEL - SEL*) Differential Input Voltage	| VIH - VIL |	0.2		4.3	V
Timing Inputs (CLK / CLK*) Input High Current Input Low Current	 IIH IIL	 -5 -6		 +30 +6	 µA µA
Functional Inputs (IN / IN*, SEL / SEL*) Input Current	IIH, IIL	-500		+500	µA
Outputs					
Digital Output Voltage Output Common Mode Range	| OUT - OUT* | (OUT + OUT*) / 2	600 VGG -1.5	700 VGG - 1.3	 VGG -1.1	mV V
Power Supply					
Power Supply Current	IEE ICC			132 60	mA mA

Test Conditions: Outputs terminated with 50Ω to VGG – 2V

AC Characteristics

(V_{GG} = - 0.1V to 2.0V; V_{CC} = 2.0V to3.6V; VEE = -3.6V to -3.0V; T_A = 0°C to 70°C)

Parameter	Symbol	Min	Typ	Max	Units
High Performance Option					
Propagation Delay CLK to OUT (SEL = 0) CLK to OUT (SEL = 1) SEL to OUT	 Tpd Tpd Tpd	 485 300 300	 630 450 450	 785 600 600	 ps ps ps
Channel to Channel Skew	t_{SKEW}			35	ps
Maximum Operating Frequency (Note 1)	Fmax	3.0			GHz
Minimum Pulse Width (Note 1)	PW min	250			ps
IN to CLK Set Up Time Hold Time	 Ts Th	 100 100			 ps ps
Output Rise and Fall Times (20% / 80%)(Note 1)	Tr / Tf		125	175	ps
Temperature Coefficient(Note 1)	ΔTpd/ΔT		<2		ps / °C

AC TEST CONDITIONS: Outputs terminated with 50Ω to VGG -2.0V.

Note 1: Guaranteed by characterization. Not production tested.

Description

The SK1527 is an extremely fast, stable, and accurate low skew 1:5 clock / signal distributor featuring a synchronous enable, which allows the outputs to be turned off and on without the risk of an upredictable output pulse. It is also capable of receiving inputs of any technology or voltage level. The D - flip-flop is triggered on the falling edge of the clock.

The SK1527 uses 50Ω outputs with source /sink capability, and is optimized for:

- High speed clock / data lines that require translation
- Point to point, double termination applications

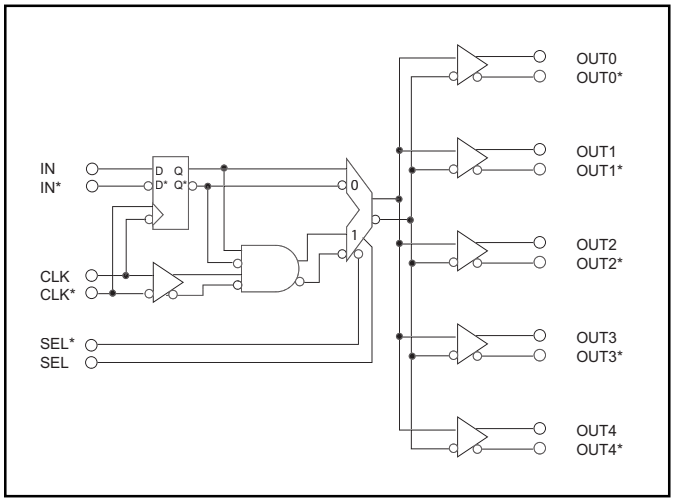
Features

- 1:5 Clock/Data Driver
- 3 GHz Fmax
- Available in 32 pin, 5mm X5mm, TQFP Package

Application Notes

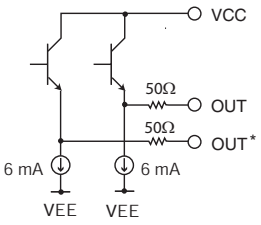
AN1001 - EPIC Family Product Line
AN1003 - Termination Techniques for ECL / LVECL PECL / LVPECL Devices
AN1004 - Interfacing Between LVDS and ECL / LVECL / PECL / LVPECL

Functional Block Diagram

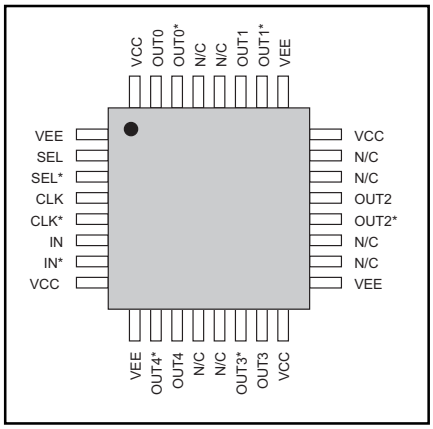


Output Option

50Ω Source / Sink



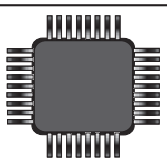
Pin Description



Package Information

32 pin, 5 mm X 5 mm

TQFP Package



DC Characteristics

(VCC = 3.0V to 3.6V; VEE = -3.6 to -3.0V; TA = 0°C to 70°C)

Parameter	Symbol	Min	Typ	Max	Units
Inputs					
Input High Input Low	VIH VIL	VEE + 2.0 VEE		VCC VCC - 0.2	V V
(IN - IN*, CLK - CLK*, SEL - SEL*) Differential Input Voltage	| VIH VIL |	0.2		4.3	V
Timing Inputs (CLK / CLK*) Input High Current Input Low Current	 IIH IIL	 -5 -6		 +30 +6	 µA µA
Functional Inputs (IN / IN*, SEL / SEL*) Input Current	IIH, IIL	-500		+500	µA
Outputs					
Digital Output Voltage Output Common Mode Range Internal Current Source Output Impedance	| OUT - OUT* | (OUT + OUT*) / 2 ISINK ROUT	600 VCC - 1.4 4 40	700 VCC -1.2 6 50	 VCC - 1.0 7.5 60	mV V mA Ω
Power Supply					
Power Supply Current	IEE			240	mA

Test Conditions: Outputs unterminated.

AC Characteristics

(VCC = 3.0V to 3.6V; VEE = -3.6 to -3.0V; TA = 0°C to 70°C)

Parameter	Symbol	Min	Typ	Max	Units
High Performance Option					
Propagation Delay CLK to OUT (SEL = 0) CLK to OUT (SEL = 1) SEL to OUT	 Tpd Tpd Tpd	 490 300 300	 690 500 500	 890 700 700	 ps ps ps
Channel to Channel Skew	t_{SKEW}			35	ps
Maximum Operating Frequency (Note 1)	Fmax	3.0			GHz
Minimum Pulse Width (Note 1)	PW min	250			ps
IN to CLK Set Up Time Hold Time	 Ts Th	 100 100			 ps ps
Output Rise and Fall Times (20% / 80%)(Note 1)	Tr / Tf		125	175	ps
Temperature Coefficient(Note 1)	ΔTpd /ΔT		<1		ps / °C

AC TEST CONDITIONS: Outputs are terminated with 50Ω to VCC-2.0V

Note 1: Guaranteed by characterization. Not production tested.

Description

The SK1528 is an extremely fast, stable, and accurate low skew 1:5 clock / signal distributor featuring a synchronous enable, which allows the outputs to be turned off and on without the risk of an upredictable output pulse. It is also capable of receiving inputs of any technology and voltage level. The D - flip-flop is triggered on the falling edge of the clock.

The SK1528 has 50Ω outputs with source /sink capability, and is optimized for:

- High speed clock / data lines that require translation
- Point to point, double termination applications

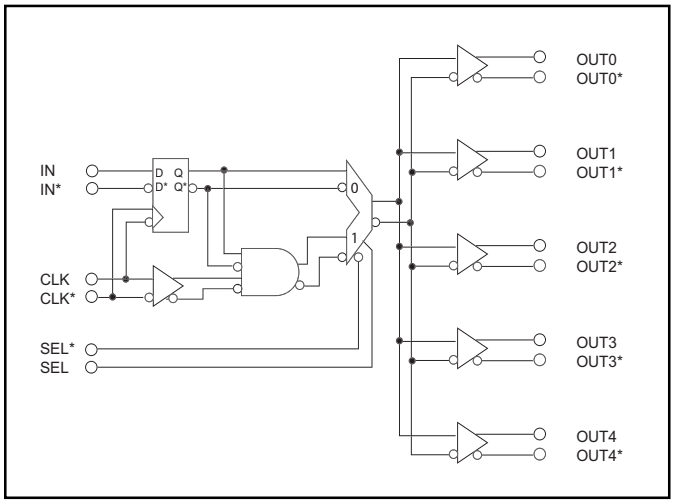
Features

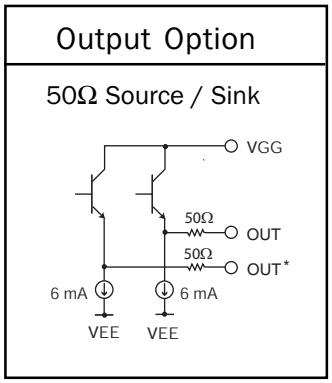
- 1:5 Clock/Data Driver
- 3 GHz Fmax
- Anything to ECL Translation
- Available in 32 pin, 5mm X5mm, TQFP Package

Application Notes

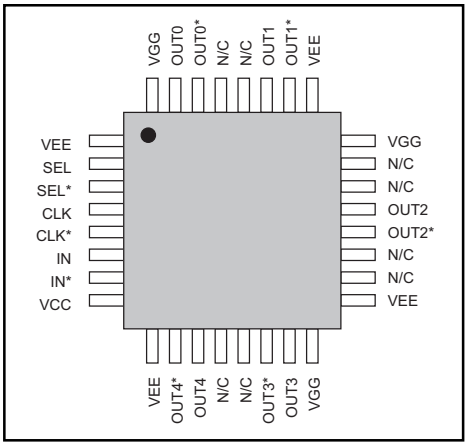
AN1001 - EPIC Family Product Line
AN1003 - Termination Techniques for ECL / LVECL PECL / LVPECL Devices
AN1004 - Interfacing Between LVDS and ECL / LVECL / PECL / LVPECL

Functional Block Diagram

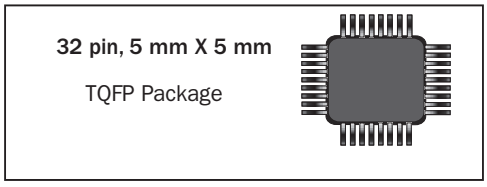




Pin Description



Package Information



DC Characteristics

(V_{GG} = - 0.1V to 2.0V; V_{CC} = 2.0V to 3.6V; VEE = -3.6V to -3.0V; T_A = 0°C to 70°C)

Parameter	Symbol	Min	Typ	Max	Units
Inputs					
Input High Input Low	VIH VIL	VEE + 2.0 VEE		VCC VCC - 0.2	V V
(IN - IN*, CLK - CLK*, SEL - SEL*) Differential Input Voltage	| VIH - VIL |	0.2		4.3	V
Timing Inputs (CLK / CLK*) Input High Current Input Low Current	 IIH IIL	 -5 -6		 +30 +6	 µA µA
Functional Inputs (IN / IN*, SEL / SEL*) Input Current	IIH, IIL	-500		+500	µA
Outputs					
Digital Output Voltage Output Common Mode Range Internal Current Source Output Impedance	| OUT - OUT* | (OUT + OUT*) / 2 ISINK ROUT	600 VGG - 1.4 4 40	700 VGG -1.2 6 50	 VGG - 1.0 7.5 60	mV V mA Ω
Power Supply					
Power Supply Current	IEE ICC			220 60	mA mA

Test Conditions: Outputs unterminated.

AC Characteristics

(V_{GG} = - 0.1V to 2.0V; V_{CC} = 2.0V to 3.6V; VEE = -3.6V to -3.0V; T_A = 0°C to 70°C)

Parameter	Symbol	Min	Typ	Max	Units
High Performance Option					
Propagation Delay CLK to OUT (SEL = 0) CLK to OUT (SEL = 1) SEL to OUT	 Tpd Tpd Tpd	 460 300 300	 786 600 600	 1100 900 900	 ps ps ps
Channel to Channel Skew	t_{SKEW}			35	ps
Maximum Operating Frequency (Note 1)	Fmax	3.0			GHz
Minimum Pulse Width (Note 1)	PW min	250			ps
IN to CLK Set Up Time Hold Time	 Ts Th	 100 100			 ps ps
Output Rise and Fall Times (20% / 80%) (Note 1)	Tr / Tf		125	300	ps
Temperature Coefficient (Note 1)	ΔTpd /ΔT		<2		ps / °C

AC TEST CONDITIONS: Outputs are terminated with 50Ω to VGG -2.0V

Note 1: Guaranteed by characterization. Not production tested.

Description

The SK1529 is an extremely fast, stable, and accurate low skew 1:5 clock / signal distributor featuring a synchronous enable, which allows the outputs to be turned off and on without the risk of an upredictable output pulse. It is also capable of receiving inputs of any technology and voltage level. The D - flip-flop is triggered on the falling edge of the clock.

The SK1529 uses 50Ω outputs with source /sink capability, and is optimized for:

- High speed clock / data lines that require translation
- Point to point, series termination applications

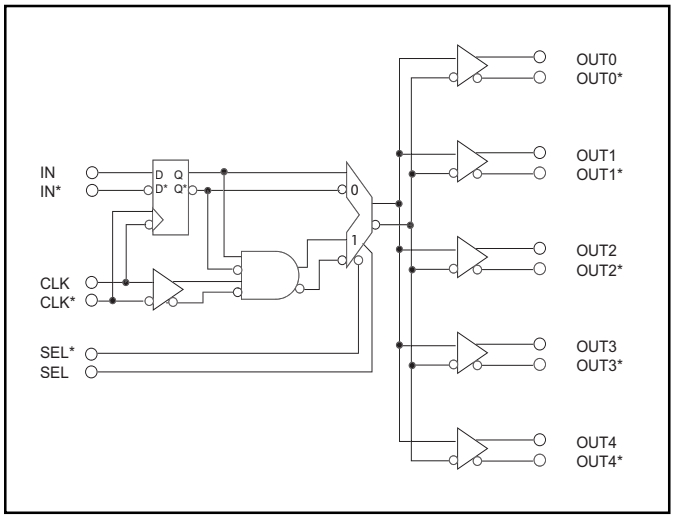
Features

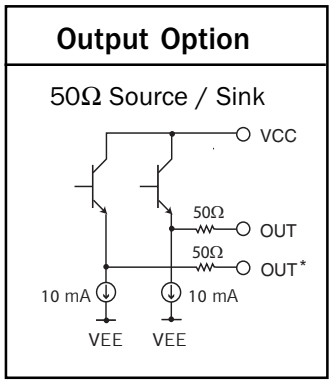
- 1:5 Clock/Data Driver
- 3 GHz Fmax
- Anything to PECL Translation
- Available in 32 pin, 5mm X5mm, TQFP Package

Application Notes

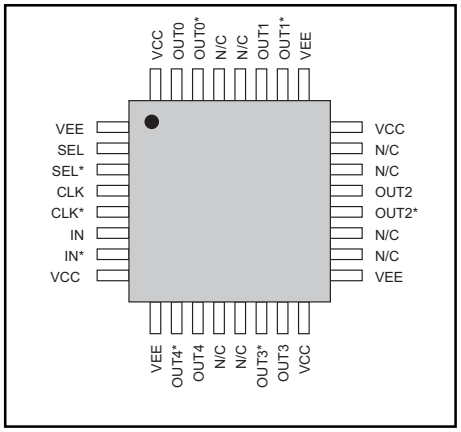
AN1001 - EPIC Family Product Line
AN1003 - Termination Techniques for ECL / LVECL PECL / LVPECL Devices
AN1004 - Interfacing Between LVDS and ECL / LVECL / PECL / LVPECL

Functional Block Diagram

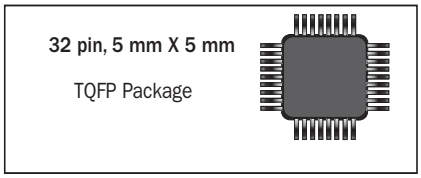




Pin Description



Package Information



DC Characteristics

(V_{CC} = 3.0V to 3.6V; VEE = -3.6V to -3.0V; T_A = 0°C to 70°C)

Parameter	Symbol	Min	Typ	Max	Units
Inputs					
Input High Input Low	VIH VIL	VEE + 2.0 VEE		VCC VCC -0.2	V V
(IN - IN*, CLK - CLK*, SEL - SEL*) Differential Input Voltage	|VIH - VIL |	0.2		4.3	V
Timing Inputs (CLK / CLK*) Input High Current Input Low Current	 IIH IIL	 -5 -6		 +30 +6	 µA µA
Functional Inputs (IN / IN*, SEL / SEL*) Input Current	IIH, IIL	-500		+500	µA
Outputs					
Digital Output Voltage Output Common Mode Range Internal Current Source Output Impedance	| OUT - OUT* | (OUT + OUT*) / 2 ISINK ROUT	600 VCC - 1.4 7.5 40	700 VCC -1.2 10 50	 VCC - 1.0 13 60	mV V mA Ω
Power Supply					
Power Supply Current	IEE			250	mA

Test Conditions: Outputs unterminated.

AC Characteristics

(V_{CC} = 3.0V to 3.6V; VEE = -3.6V to -3.0V; T_A = 0°C to 70°C)

Parameter	Symbol	Min	Typ	Max	Units
High Performance Option					
Propagation Delay CLK to OUT (SEL = 0) CLK to OUT (SEL = 1) SEL to OUT	 Tpd Tpd Tpd	 490 300 300	 690 500 500	 890 700 700	 ps ps ps
Channel to Channel Skew	t_{SKEW}			35	ps
Maximum Operating Frequency (Note 1)	Fmax	3.0			GHz
Minimum Pulse Width (Note 1)	PW min	250			ps
IN to CLK Set Up Time Hold Time	 Ts Th	 100 100			 ps ps
Output Rise and Fall Times (20% / 80%) (Note 1)	Tr / Tf		125	200	ps
Temperature Coefficient (Note 1)	ΔTpd /ΔT		<2		ps / °C

AC TEST CONDITIONS: Outputs are terminated with 50Ω to VCC-2.0V

Note 1: Guaranteed by characterization. Not production tested.

Description

The SK1530 is an extremely fast, stable and accurate low skew 1:5 clock / signal distributor featuring a synchronous enable, which allows the outputs to be turned off and on without the risk of an upredictable output pulse. It is also capable of receiving inputs of any technology or voltage level. The D - flip-flop is triggered on the falling edge of the clock.

The SK1530 uses 50Ω outputs with source /sink capability, and is optimized for:

- High speed clock / data lines that require translation
- Point to point, series termination applications

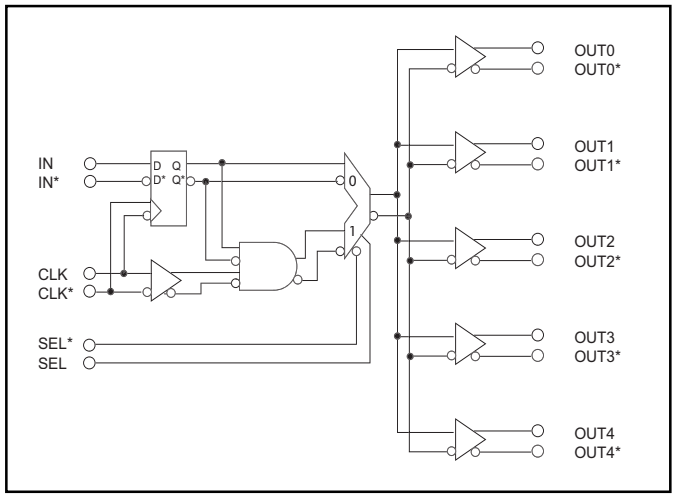
Features

- 1:5 Clock/Data Driver
- 3 GHz Fmax
- Anything to ECL Translation
- Available in 32 pin, 5mm X5mm, TQFP Package

Application Notes

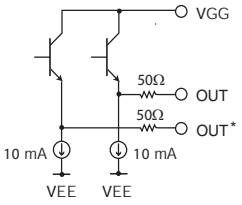
AN1001 - EPIC Family Product Line
AN1003 - Termination Techniques for ECL / LVECL PECL / LVPECL Devices
AN1004 - Interfacing Between LVDS and ECL / LVECL / PECL / LVPECL

Functional Block Diagram

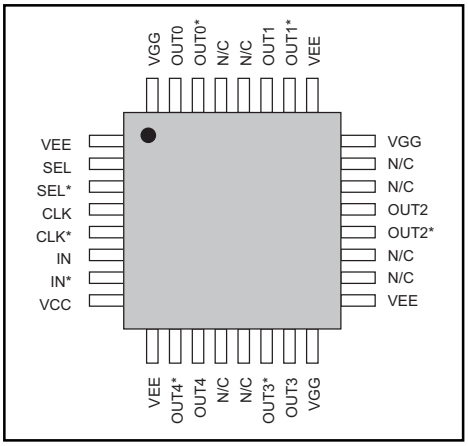


Output Option

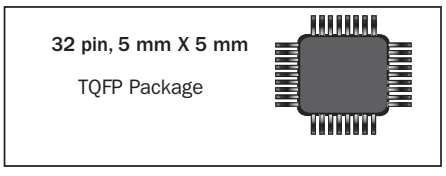
50Ω Source / Sink



Pin Description



Package Information



DC Characteristics

(V_{GG} = -0.1V to 2.0V; V_{CC} = 2.0V to 3.6V; V_{EE} = -3.6V to -3.0V; T_A = 0°C to 70°C)

Parameter	Symbol	Min	Typ	Max	Units
Inputs					
Input High Input Low	VIH VIL	VEE + 2.0 VEE		VCC VCC -0.2	V V
(IN - IN*, CLK - CLK*, SEL - SEL*) Differential Input Voltage	| VIH - VIL |	0.2		4.3	V
Timing Inputs (CLK / CLK*) Input High Current Input Low Current	 IIH IIL	 -5 -6		 +30 +6	 µA µA
Functional Inputs (IN / IN*, SEL / SEL*) Input Current	IIH, IIL	-500		+500	µA
Outputs					
Digital Output Voltage Output Common Mode Range Internal Current Source Output Impedance	| OUT - OUT* | (OUT + OUT*) / 2 ISINK ROUT	600 VGG - 1.4 7.5 40	700 VGG -1.2 10 50	 VGG - 1.0 13 60	mV V mA Ω
Power Supply					
Power Supply Current	IEE ICC	2.0		375 60	mA mA

Test Conditions: Outputs unterminated.

AC Characteristics

(V_{GG} = -0.1V to 2.0V; V_{CC} = 2.0V to 3.6V; V_{EE} = -3.6V to -3.0V; T_A = 0°C to 70°C)

Parameter	Symbol	Min	Typ	Max	Units
High Performance Option					
Propagation Delay CLK to OUT (SEL = 0) CLK to OUT (SEL = 1) SEL to OUT	 Tpd Tpd Tpd	 460 300 300	 480 600 600	 1100 900 900	 ps ps ps
Channel to Channel Skew	t_{SKEW}			35	ps
Maximum Operating Frequency (Note 1)	Fmax	3.0			GHz
Minimum Pulse Width (Note 1)	PW min	250			ps
IN to CLK Set Up Time Hold Time	 Ts Th	 100 100			 ps ps
Output Rise and Fall Times (20% / 80%) (Note 1)	Tr / Tf		125	300	ps
Temperature Coefficient (Note 1)	ΔTpd /ΔT		<2		ps / °C

AC TEST CONDITIONS: Outputs are terminated with 50Ω to VGG -2.0V

Note 1: Guaranteed by characterization. Not production tested.

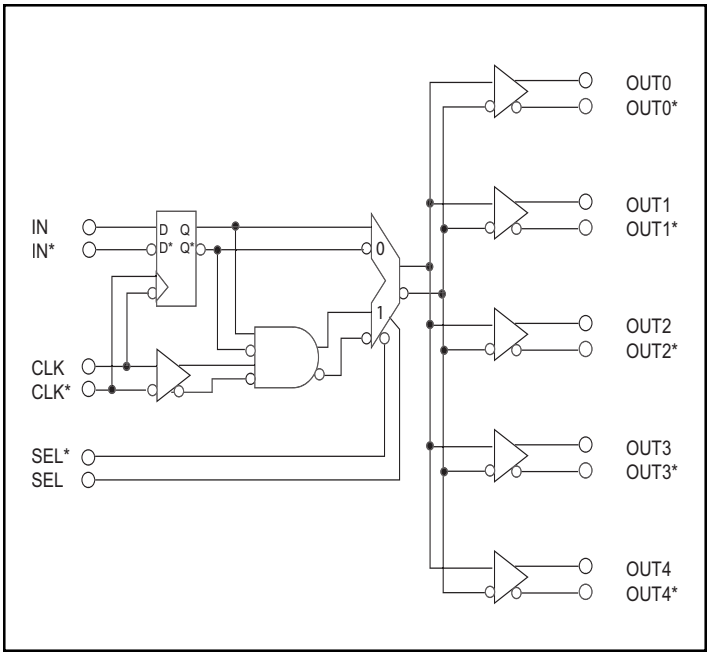
Description

The SK1599 is an extremely fast, stable, and accurate low skew 1:5 clock / signal distributor featuring a synchronous enable, which allows the outputs to be turned off and on without the risk of an unpredictable output pulse. The D - flip-flop is triggered on the falling edge of the clock.

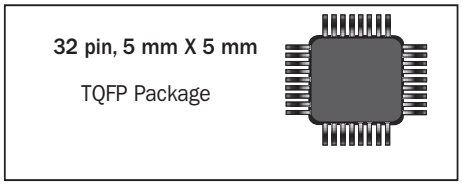
The SK1599 has open collector (CML) outputs, targeted for:

- Ultra high speed applications
- Adjustable common mode levels at the destination.

Functional Block Diagram



Package Information



Features

- 1:5 Clock/Data Driver
- 3 GHz Fmax
- 3.3V / 5.2V Compatible
- Available in 32 lead, 5mm X5mm, TQFP Package

Application Notes

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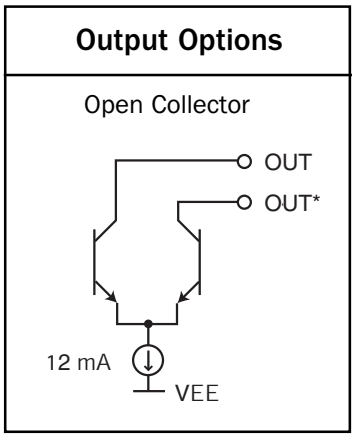
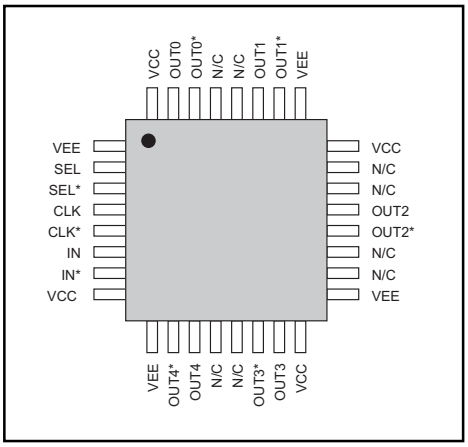
AN1004 - Interfacing Between LVDS and ECL / LVECL / PECL / LVPECL
AN1008 - Interfacing with CML



Pin Description



DC Characteristics

(V_{CC} - VEE = 3.0V to 5.5V; T_A = 0°C to 70°C)

Parameter	Symbol	Min	Typ	Max	Units
Inputs					
Input High Input Low	VIH VIL	VEE + 2.0 VEE		VCC VCC -0.2	V V
(IN - IN*, CLK - CLK*, SEL - SEL*) Differential Input Voltage	| VIH - VIL |	0.2		4.3	V
Timing Inputs (CLK / CLK*) Input High Current Input Low Current	 IIH IIL	 -5 -6		 +30 +6	 µA µA
Functional Inputs (IN / IN*, SEL / SEL*) Input Current	IIH, IIL	-500		+500	µA
Outputs					
Output Current High Output Current Low	IOZ IOL	-500 9	0 12	+500 15	µA mA
Power Supply					
Power Supply Current	IEE		145	225	mA

Test Conditions: Outputs terminated with 50Ω to VCC.

AC Characteristics

(V_{CC} - VEE = 3.0V to 5.5V; T_A = 0°C to 70°C)

Parameter	Symbol	Min	Typ	Max	Units
High Performance Option					
Propagation Delay CLK to OUT (SEL = 0) CLK to OUT (SEL = 1) SEL to OUT	 Tpd Tpd Tpd	 485 300 300	 630 450 450	 785 600 600	 ps ps ps
Channel to Channel Skew	t_{SKEW}			35	ps
Maximum Operating Frequency (Note 1)	Fmax	3.0			GHz
Minimum Pulse Width (Note 1)	PW min	250			ps
IN to CLK Set Up Time Hold Time	 Ts Th	 100 100			 ps ps
Output Rise and Fall Times (20% / 80%) (Note 1)	Tr / Tf		125	250	ps
Temperature Coefficient (Note 1)	ΔTpd /ΔT		<1		ps / °C

AC TEST CONDITIONS: Outputs are terminated with 50Ω to VCC

Note 1: Guaranteed by characterization. Not production tested.

Ordering Information

Ordering Code	Package ID
SK1500ATF	32 - TQFP 5 X 5 mm
SK1501ATF	32 - TQFP 5 X 5 mm
SK1502ATF	32 - TQFP 5 X 5 mm
SK1503ATF	32 - TQFP 5 X 5 mm
SK1504ATF	32 - TQFP 5 X 5 mm
SK1525ATF	32 - TQFP 5 X 5 mm
SK1526ATF	32 - TQFP 5 X 5 mm
SK1527ATF	32 - TQFP 5 X 5 mm
SK1528ATF	32 - TQFP 5 X 5 mm
SK1529ATF	32 - TQFP 5 X 5 mm
SK1530ATF	32 - TQFP 5 X 5 mm
SK1599ATF	32 - TQFP 5 X 5 mm

Notes:

1. For Tape and Reel, add the letter “T” at the end of Ordering Code.
2. For Tape and Reel information, see TMD Part Ordering Information Data Sheet.

Contact Information

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