First-In First-Out Memory

64 Words by 9 Bits Cascadable

The TRW TDC1030 is an expandable, First-In First-Out (FIFO) memory organized as 64 words by 9 bits. A 15MHz data rate makes it ideal in high-speed applications. Burst data rates of 18MHz can be obtained in applications where the device status flags are not used.

With separate Shift-In (SI) and Shift-Out (SO) controls, reading and writing operations are completely independent, allowing synchronous and asynchronous data transfers. Additional controls include a Master Reset ($\overline{MR}$), and Output Enable ($\overline{OE}$). Input Ready (IR) and Output Ready (OR) flags are provided to indicate device status.

Devices can be easily interconnected to expand word and bit dimensions. The device has all output pins directly opposite the corresponding input pins, facilitating board layouts in expanded format. All inputs and outputs are TTL compatible.

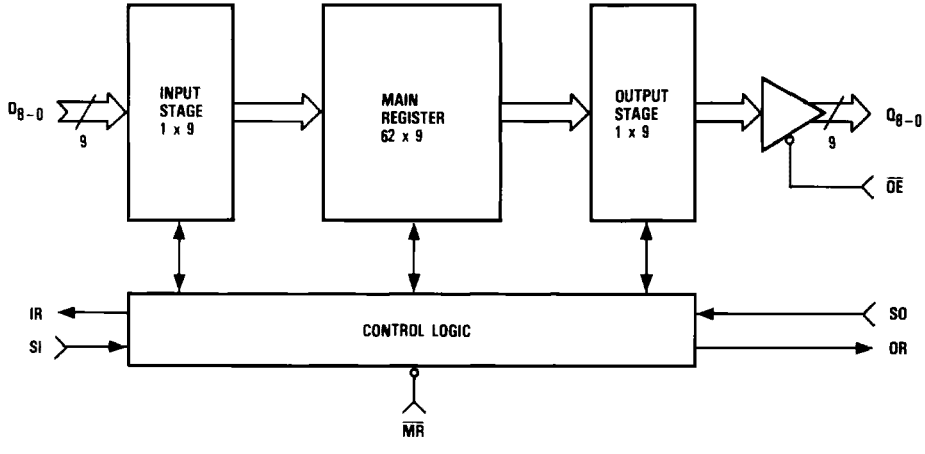
Features

- 64 Words By 9 Bits Organization
- 15MHz Shift-In, Shift-Out Rates With Flags
- 18MHz Burst-In, Burst-Out Rates Without Flags
- Cascadable To 13MHz
- Readily Expandable In Word And Bit Dimension
- TTL Compatible
- Asynchronous Or Synchronous Operation
- Three-State Outputs
- Master Reset Input To Clear Control
- Output Pins Directly Opposite Corresponding Input Pins For Easy Board Layout
- Available In 28 Pin Ceramic DIP, CERDIP, Or Contact Chip Carrier

Applications

- High-Speed Disk Or Tape Controller
- Video Time Base Correction
- A/D Output Buffers
- Voice Synthesis
- Input/Output Formatter For Digital Filters And FFTs

Functional Block Diagram



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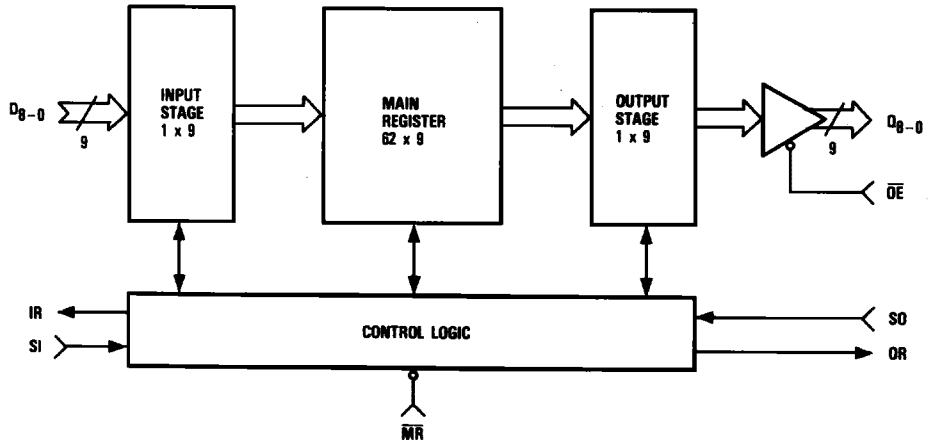
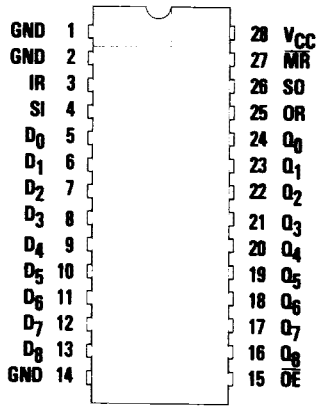
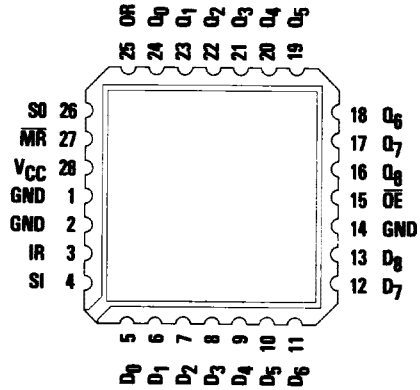
Functional Block Diagram



Pin Assignments



28 Lead DIP – J6 Package
28 Lead CERDIP – B6 Package



28 Contact Chip Carrier – C3 Package

Functional Description

Data Input (Figure 1)

Following power up, the Master Reset ($\overline{MR}$) is pulsed LOW to clear the FIFO (Figure 2). The Input Ready (IR) flag HIGH indicates that the FIFO input stage is empty and available to receive data. When IR is valid (HIGH), Shift-In (SI) may be asserted, thus loading the data present at D_0 through D_8 into the FIFO. Bringing the SI signal HIGH causes IR to drop LOW. The data remains at the first location until SI is set LOW. With SI LOW, the data then propagates to the second location and continues to "fall through" to the output stage or last empty location. If the FIFO is not full after the SI pulse, IR will again be valid (HIGH), indicating that there is space available in the FIFO. If the memory is full, the IR flag remains invalid (LOW).

With the FIFO full, the SI can be held HIGH until a Shift-Out (SO) occurs (Figure 3). Following the SO pulse, the empty location "bubbles up" to the input stage. This results in an Input Ready (IR) pulse HIGH and awaiting data is shifted in. The SI must be brought LOW before additional data can be shifted in.

Data Transfer

After data has been transferred into the second location by bringing SI LOW, the data continues to "fall through" the FIFO in an asynchronous manner. The data stacks up at the end of the device, leaving the empty locations up front.

Data Output (Figure 4)

The Output Ready (OR) flag HIGH indicates that there is valid data at the output stage (pins Q_0-Q_8). An initial Master Reset ($\overline{MR}$) pulse LOW at power up sets the Output Ready LOW (Figure 2). Although the internal control circuitry is cleared, random data remains on the output pins. Data shifted into the FIFO (after $\overline{MR}$) "falls through" to the output stage, causing OR to go HIGH, and replaces the random data with valid data.

When the OR flag is valid (HIGH), data can be transferred out via the Shift-Out (SO) control. An SO HIGH results in a "busy" (LOW) signal at the OR flag. When SO is brought LOW, data is shifted to the output stage, and the empty location "bubbles up" to the input stage. At the completion of the SO pulse, OR goes HIGH. If the last valid piece of data has been shifted out, leaving the memory empty, the OR flag remains invalid (LOW). With the FIFO empty, the last word shifted out remains on the output pins Q_0-Q_8.

With the FIFO empty, the SO can be held HIGH until a SI occurs (Figure 5). Following the SI pulse, the data "falls through" to the output stage. This results in an OR pulse HIGH and data is shifted out. The SO must be brought LOW before additional data can be shifted out.

Data Inputs

The nine data inputs of the TDC1030 are TTL compatible. There is no weighting to the inputs, and any one of them can be assigned as the MSB. The memory size of the FIFO can be reduced from the 9 x 64 configuration by leaving open unused data input pins (i.e., 8 x 64, 7 x 64 . . . 1 x 64). In the reduced format, the unused data output pins must also be left open.

Name	Function	Value	J6, C3, B6 Package
D_0	Data Input	TTL	Pin 5
D_1		TTL	Pin 6
D_2		TTL	Pin 7
D_3		TTL	Pin 8
D_4		TTL	Pin 9
D_5		TTL	Pin 10
D_6		TTL	Pin 11
D_7		TTL	Pin 12
D_8	Data Input	TTL	Pin 13

Data Outputs

The nine data outputs of the TDC1030 are TTL compatible, capable of driving four low-power Schottky TTL (54/74 LS) unit loads or the equivalent. There is no weighting to the outputs, and any one of them can be assigned as the MSB.

The memory size of the FIFO can be reduced from the 9 x 64 configuration by leaving open unused data output pins (i.e., 8 x 64, 7 x 64 . . . 1 x 64). In the reduced format, the unused data input pins must also be left open.

Name	Function	Value	J6, C3, B6 Package
Q_0	Data Output	TTL	Pin 24
Q_1		TTL	Pin 23
Q_2		TTL	Pin 22
Q_3		TTL	Pin 21
Q_4		TTL	Pin 20
Q_5		TTL	Pin 19
Q_6		TTL	Pin 18
Q_7		TTL	Pin 17
Q_8	Data Output	TTL	Pin 16

Controls

SI — The rising edge loads data into the input stage. The falling edge triggers the automatic data transfer process.

SO — The rising edge causes OR to go LOW. The falling edge moves upstream data into the output stage and triggers the "bubble up" process of empty locations.

$\overline{MR}$ — $\overline{MR}$ LOW clears all data and control within the FIFO: Input Ready flag is set HIGH, Output Ready flag is set LOW, and the FIFO is cleared. The output stage remains in the state of the last word shifted out, or in the random state of power up.

$\overline{OE}$ — With the $\overline{OE}$ LOW, the outputs of the FIFO are TTL compatible. When disabled ($\overline{OE}$ HIGH), the outputs go into their high-impedance state.

Name	Function	Value	J6, C3, B6 Package
SI	Shift-In	TTL	Pin 4
SO	Shift-Out	TTL	Pin 26
$\overline{MR}$	Master Reset	TTL	Pin 27
$\overline{OE}$	Output Enable	TTL	Pin 15

Power

The TDC1030 operates from a single +5.0V supply. All power and ground pins must be connected.

Name	Function	Value	J6, C3, B6 Package
V_{CC}	Supply Voltage	+5.0	Pin 28
GND	Digital Ground	0.0	Pins 1, 2, 14

Status Flags

Input Ready (IR) and Output Ready (OR) flags are provided to indicate the status of the FIFO. Operation with use of the flags is explained in the Functional Description. In this mode of operation, the Shift-In and Shift-Out rates are determined by the status flags. It is assumed that a Shift-In or Shift-Out pulse is not applied until the respective flag (IR, OR) is valid (Figures 1 and 4).

The IR and OR flags are not required to operate the device. A high-speed burst mode is achievable when operating without the flags. Refer to the High-Speed Burst Mode section for a complete description.

IR — An IR flag HIGH indicates that the input stage is empty and ready to accept valid data. An IR LOW indicates that the FIFO is full or that a previous SI operation is not complete.

OR — An OR flag HIGH assures valid data at the output stage (pins Q_0-Q_8). However, the OR flag does not indicate whether or not there is any new data awaiting transfer into the output stage. An OR LOW indicates that the output stage is "busy", or that there is no valid data.

Name	Function	Value	J6, C3, B6 Package
IR	Input Ready Flag	TTL	Pin 3
OR	Output Ready Flag	TTL	Pin 25

Application Notes

Expanded Format

The TDC1030 is easily cascaded to increase word capacity without any external circuitry. Word capacity can be expanded beyond the 128 words X 9 bits configuration shown in Figure 6. In the cascaded format, all necessary communications and timing are handled by the FIFOs themselves. The intercommunication speed is controlled by the minimum flag pulse widths and the flag delays. (See Figures 7 and 8.)The maximum data rate when cascading devices is 13MHz.

With the addition of a logic gate, the FIFO is easily expanded to increase word length (Figure 9). The basic operation and timing are identical to a single FIFO, with the exception of an additional gate delay on the flags. Word length can be expanded beyond the 18 bits X 64 words configuration shown in Figure 9.

High-Speed Burst Mode

Burst rates of 18MHz can be obtained for applications in which the device status flags are not used. In this mode of operation, the Burst-In and Burst-Out rates are determined by the minimum Shift-In Pulse Widths, and Shift-Out Pulse Widths (See Figures 10 and 11). With the Input Ready and Output Ready flags not monitored, a shift pulse can be applied without regard to the status flag. However, a Shift-In pulse which would overflow the storage capacity of the FIFO is not permitted.

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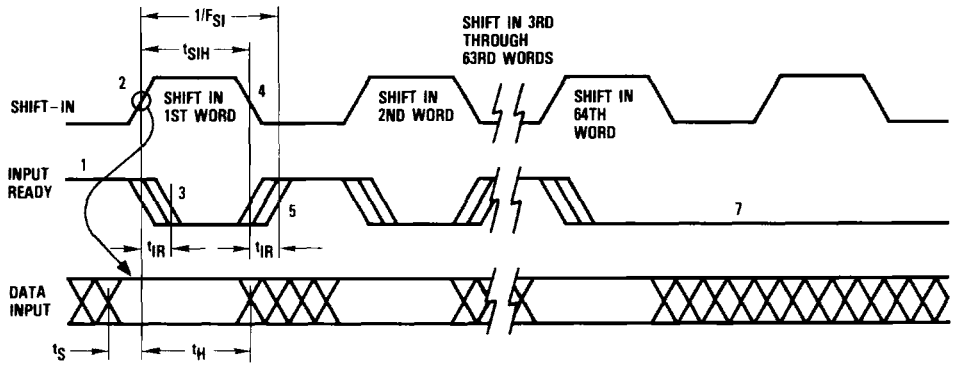
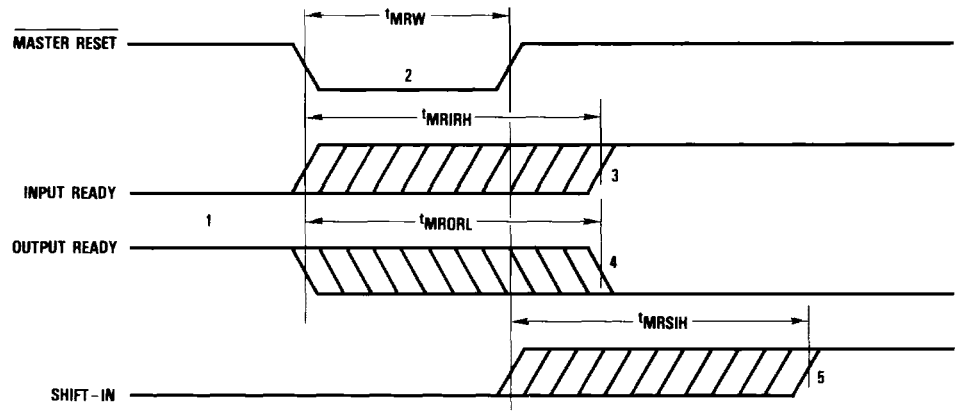
TDC1030 Timing Diagrams

Figure 1. Shifting In Sequence, FIFO Empty To FIFO Full



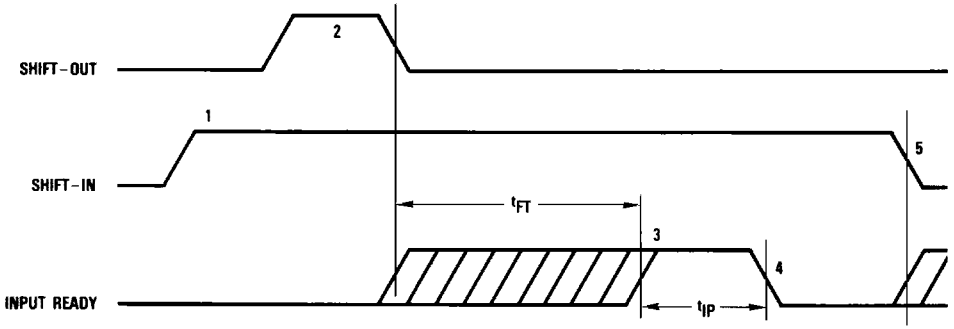
1. Input Ready initially HIGH – FIFO is prepared for valid data.
2. Shift-In set HIGH – data loaded into input stage.
3. Input Ready drops LOW (t_{IR} delay after SI HIGH) – input stage "busy."
4. Shift-In set LOW – data from first location "falls through."
5. Input Ready goes HIGH (t_{IR} delay after SI LOW) – status flag indicates FIFO prepared for additional data.
6. Repeat process to load 2nd through 64th word into FIFO.
7. Input Ready remains LOW – with attempt to shift into full FIFO, no data transfer occurs.

Figure 2. Master Reset Applied With FIFO Full



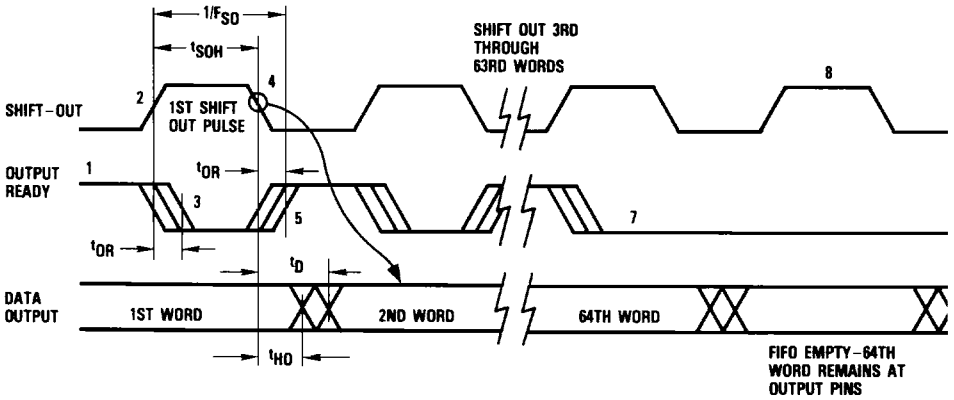
1. Input Ready LOW, Output Ready HIGH – assume FIFO is full.
2. Master Reset pulse LOW – clears FIFO.
3. Input Ready goes HIGH (t_{MRIRH} delay after $\overline{MR}$) – flag indicates input prepared for valid data.
4. Output Ready drops LOW (t_{MRORL} delay after $\overline{MR}$) – flag indicates FIFO empty.
5. Shift-In HIGH (t_{MRSI} delay after $\overline{MR}$) – clearing process complete, move new data into FIFO.

Figure 3. With FIFO Full, Shift-In Held High In Anticipation Of Empty Location



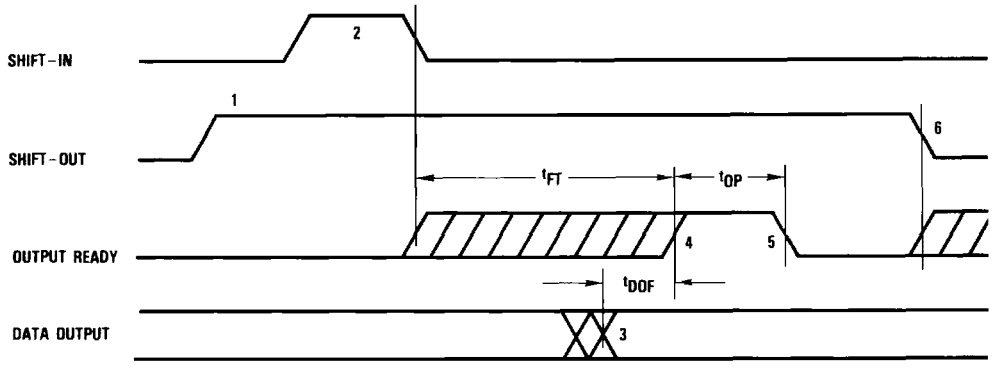
1. FIFO is initially full, Shift-In is held HIGH.
2. Shift-Out pulse - data in the output stage is unloaded, "bubble up" process of empty location begins.
3. Input Ready HIGH (t_{FT} fallthrough delay after SO pulse) - when empty location reaches input stage, flag indicates FIFO is prepared for data input.
4. Input Ready returns LOW - data Shift-In to empty location is complete, FIFO is again full.
5. SI brought LOW - necessary to complete Shift-In process, allows data "fall through" if additional empty location "bubbles up."

Figure 4. Shifting Out Sequence, FIFO Full to FIFO Empty



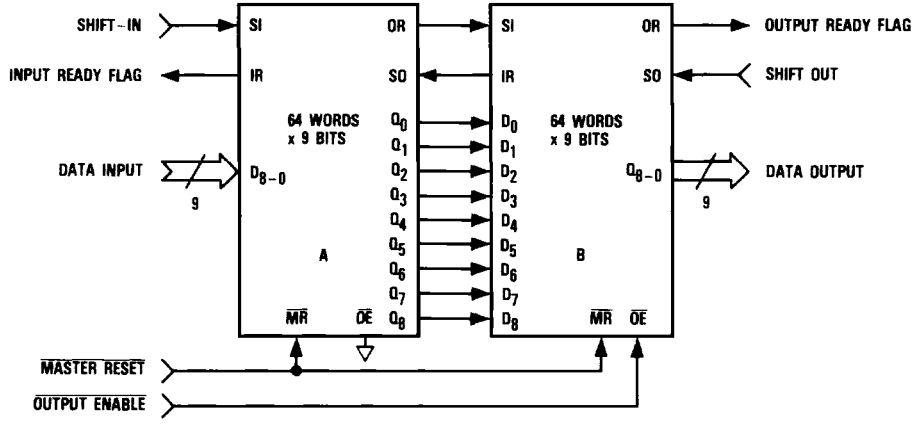
1. Output Ready HIGH - no data transferring in progress, valid data is present at output stage.
2. Shift-Out set HIGH - results in OR LOW.
3. Output Ready drops LOW (t_{OR} delay after SO HIGH) - output stage "busy."
4. Shift-Out set LOW - data in the input stage is unloaded, and new data replaces it as empty location "bubbles up" to input stage.
5. Output Ready goes HIGH - transfer process completed, valid data present at output.
6. Repeat process to unload the 3rd through 64th word from FIFO.
7. Output Ready remains LOW - FIFO is empty.
8. Shift-Out pulse asserted - with attempt to unload from empty FIFO, no data transfer occurs.

Figure 5. With FIFO Empty Shift Out Is Held High In Anticipation Of Data



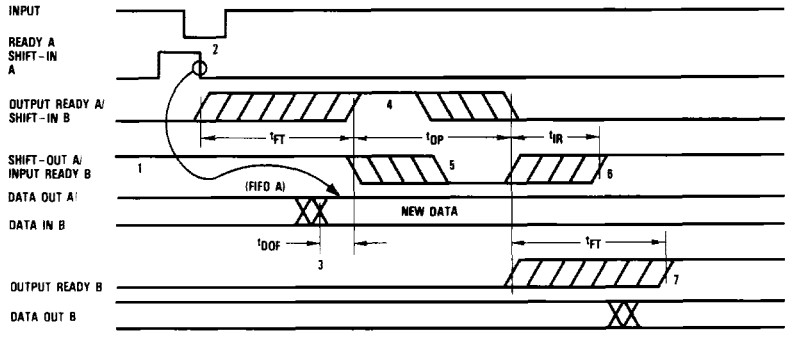
1. FIFO is initially empty, Shift-Out is held HIGH.
2. Shift-In pulse - loads data into FIFO and initiates "fall through" process.
3. Data Output transition - (t_{DOF} delay before OR HIGH), valid data arrives at output stage.
4. Output Ready HIGH - (t_{FT} fallthrough delay after SI pulse), OR flag signals the arrival of valid data at the output stage.
5. Output Ready goes LOW - data Shift-Out is complete, FIFO is again empty.
6. Shift-Out set LOW - necessary to complete Shift-Out process, allows "bubble up" of empty location as data "falls through."

Figure 6. Cascading For Increased Word Capacity - 128 Words X 9 Bits



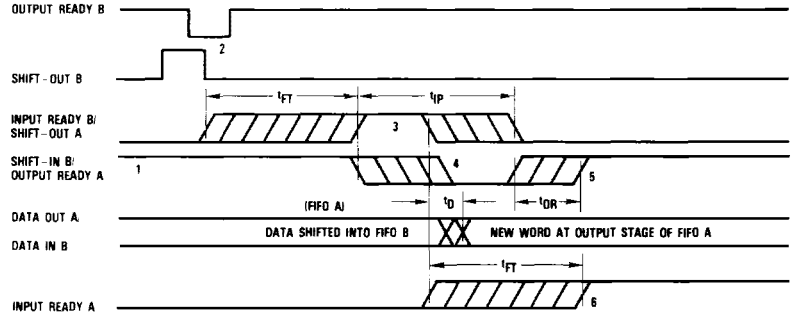
The TDC1030 is easily cascaded to increase word capacity without any external circuitry. In the cascaded format, all necessary communications are handled by the FIFOs themselves. Figures 7 and 8 demonstrate the intercommunication timing between FIFO A and FIFO B.

Figure 7. FIFO – FIFO Communication: Input Timing Under Empty Condition



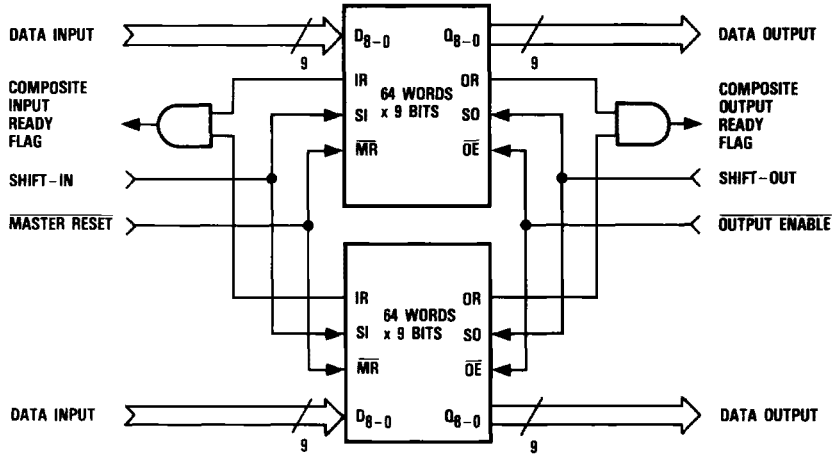
1. FIFO A and B initially empty, SO (A) held HIGH in anticipation of data.
2. Load one word into FIFO A – SI pulse applied, IR pulse results.
3. Data Out A/Data In B transition – (t_{DOF} delay before OR (A) HIGH), valid data arrives at FIFO A output stage prior to OR flag, meeting data input setup requirements of FIFO B.
4. OR (A) and SI (B) pulse HIGH – (t_{FT} delay after SI (A) LOW), data is unloaded from FIFO A as a result of the Output Ready Pulse (T_{OP}), data is shifted into FIFO B.
5. IR (B) and SO (A) go LOW – (t_{IR} delay after SI (B) HIGH), flag indicates input stage of FIFO B is "busy," Shift-Out of FIFO A is complete.
6. IR (B) and SO (A) go HIGH – (t_{IR} delay after SI (B) LOW), input stage of FIFO B is again available to receive data, SO is held HIGH in anticipation of additional data.
7. OR (B) goes HIGH – (t_{FT} delay after SI (B) LOW), valid data is present at the FIFO B output stage.

Figure 8. FIFO – FIFO Communication: Output Timing Under Full Condition



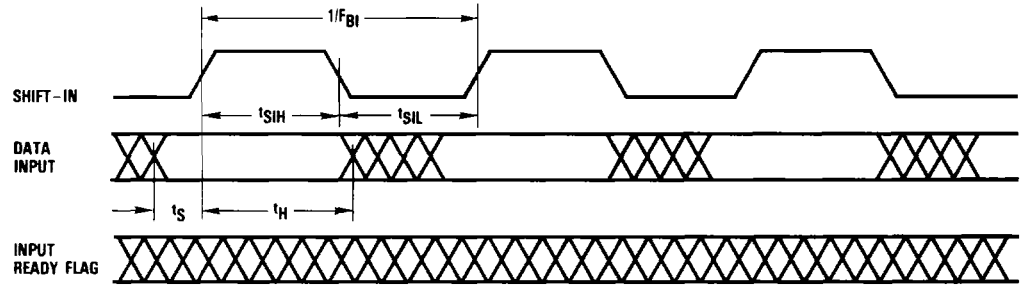
1. FIFO A and B initially full, SI (B) held HIGH in anticipation of shifting in new data as empty location "bubbles up."
2. Unload one word from FIFO B – SO pulse applied, OR pulse results.
3. IR (B) and SO (A) pulse HIGH – (t_{FT} delay after SO (B) LOW), data is loaded into FIFO B as a result of the Input Ready Pulse (tIP), data is shifted out of FIFO A.
4. OR (A) and SI (B) go LOW – (t_{OR} delay after SO (A) HIGH), flag indicates the output stage of FIFO A is "busy," Shift-In to FIFO B is complete.
5. OR (A) and SI (B) go HIGH – (t_{OR} delay after SO (A) LOW), flag indicates valid data is again available at the FIFO A output stage, SI (B) is held HIGH, awaiting "bubble up" of empty location.
6. IR (A) goes HIGH – (t_{FT} delay after SO (A) LOW), an empty location is present at input stage of FIFO A.

Figure 9. Expanded FIFO for Increased Word Length – 64 Words X 18 Bits



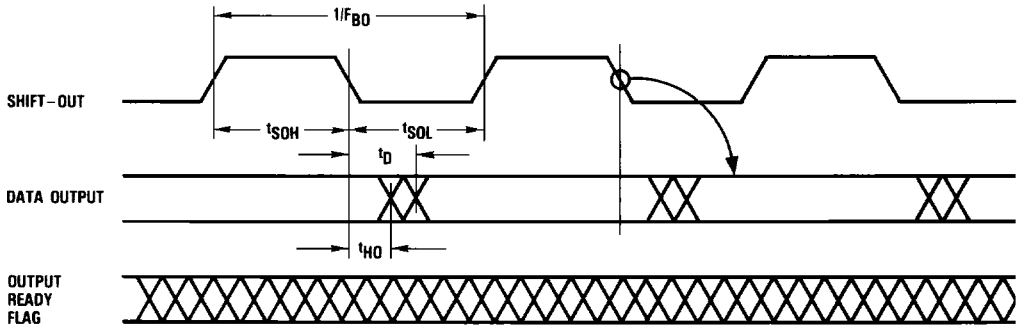
The TDC1030 is easily expanded to increase word length. Composite Input Ready and Output Ready flags are formed with the addition of an AND logic gate. The basic operation and timing are identical to a single FIFO, with the exception of an added gate delay on the flags.

Figure 10. Shift-In Operation In High-Speed Burst Mode



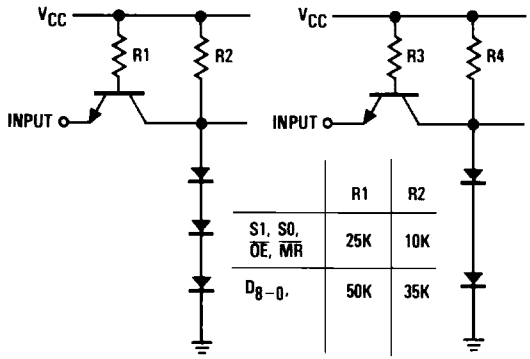
In the high-speed mode, the Burst-In rate is determined by the minimum Shift-In HIGH and Shift-In LOW specifications. The IR status flag is a "don't care" condition, and a Shift-In pulse can be applied without regard to the flag. A Shift-In pulse which would overflow the storage capacity of the FIFO is not permitted.

Figure 11. Shift-Out Operation In High-Speed Burst Mode



In the high-speed mode, the Burst-Out rate is determined by the minimum Shift-Out HIGH and Shift-Out LOW specifications. The OR flag is a "don't care" condition, and a Shift-Out pulse can be applied without regard to the flag.

Figure 12. Equivalent Input Circuit



	R1	R2
S1, S0, $\overline{OE}$, $\overline{MR}$	25K	10K
D_{8-0},	50K	35K

Figure 13. Equivalent Output Circuit

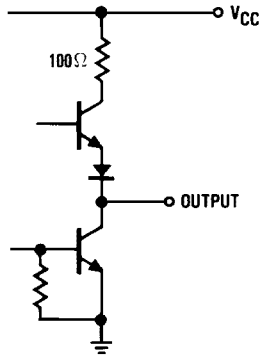


Figure 14. Test Load

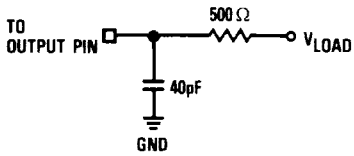
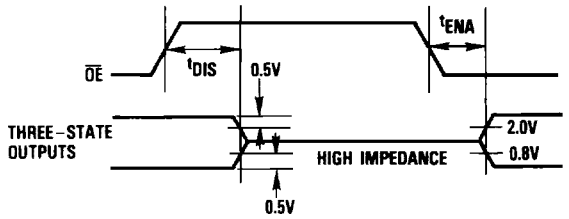


Figure 15. Transition Levels For Three-State Measurements



Absolute maximum ratings (beyond which the device will be damaged) [1]

Supply Voltage	−0.5 to +7.0V
Input	
Applied voltage	−0.5 to +5.5V [2]
Forced current	−6.0 to +6.0mA
Output	
Applied voltage	−0.5 to +5.5V [2]
Forced current	−1.0 to +6.0mA [3,4]
Short circuit duration (single output in high state to ground)	1 sec
Temperature	
Operating, case	−60 to +140°C
junction	+175°C
Lead, soldering (10 seconds)	+300°C
Storage	−65 to +150°C

Notes

1. Absolute maximum ratings are limiting values applied individually while all other parameters are within specified operating conditions. Functional operation under any of these conditions is NOT implied.
2. Applied voltage must be current limited to specified range, and measured with respect to GND.
3. Forcing voltage must be limited to specified range
4. Current is specified as positive when flowing into the device.

Operating conditions

Parameter		Temperature Range						Units
		Standard			Extended			
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.75	5.0	5.25	4.5	5.0	5.5	V
t_{SIL}	Shift-In Pulse Width, LOW	20			20			ns
t_{SIH}	Shift-In Pulse Width, HIGH	15			18			ns
t_S	Input Setup Time	0			0			ns
t_H	Input Hold Time	25			30			ns
t_{SOL}	Shift-Out Pulse Width, LOW	20			20			ns
t_{SOH}	Shift-Out Pulse Width, HIGH	15			18			ns
V_{IL}	Input Voltage, Logic LOW			0.8			0.8	V
V_{IH}	Input Voltage, Logic HIGH	2.0			2.0			V
I_{OL}	Output Current, Logic LOW			4.0			4.0	mA
I_{OH}	Output Current, Logic HIGH			−400			−400	μA
T_A	Ambient Temperature, Still Air	0		70				°C
T_C	Case Temperature				−55		125	°C

Electrical characteristics within specified operating conditions

Parameter		Test Conditions	Temperature Range				Units
			Standard		Extended		
			Min	Max	Min	Max	
I_{CC}	Supply Current	V_{CC} = Max, static					
		T_A = 0°C to 70°C		350			mA
		T_A = 70°C		280			mA
		T_C = −55°C to 125°C				400	mA
		T_C = 125°C				260	mA
I_{IL}	Input Current, Logic LOW	V_{CC} = Max, V_I = 0.4V					
		D_{8-0}		−0.4		−0.4	mA
		SI, SO, $\overline{OE}$, $\overline{MR}$		−1.0		−1.0	mA
I_{IH}	Input Current, Logic HIGH	V_{CC} = Max, V_I = 2.4V		75		75	μA
I_I	Input Current, Max Input Voltage	V_{CC} = Max, V_I = 5.5V		1.0		1.0	mA
V_{OL}	Output Voltage, Logic LOW	V_{CC} = Min, I_{OL} = Max		0.5		0.5	V
V_{OH}	Output Voltage, Logic HIGH	V_{CC} = Min, I_{OH} = Max	2.4		2.4		V
I_{OZL}	HIGH-Z Output, Leakage Current, Logic LOW	V_{CC} = Max, V_I = 0.4V		−40		−40	μA
I_{OZH}	HIGH-Z Output, Leakage Current, Logic HIGH	V_{CC} = Max, V_I = 2.4V		40		40	μA
I_{OS}	Short Circuit Output Current	V_{CC} = Max, One pin to ground, one second duration, output HIGH.		−40		−40	mA
C_I	Input Capacitance	T_A = 25°C, F = 1.0MHz		15		15	pF
C_O	Output Capacitance	T_A = 25°C, F = 1.0MHz		15		15	pF

Switching characteristics within specified operating conditions [1]

Parameter		Test Conditions	Temperature Range				Units
			Standard		Extended		
			Min	Max	Min	Max	
F_{SI}	Shift-In Clock Rate	V_{CC} = Min	18		16		MHz
F_{BI}	Burst-In Clock Rate	V_{CC} = Min	20		18		MHz
t_{IR}	Input Ready Delay	V_{CC} = Min		40		50	ns
t_{FT}	Fallthrough Time	V_{CC} = Min, Test Load: V_{LOAD} = 2.2V		1.6		1.8	μs
F_{SO}	Shift-Out Clock Rate	V_{CC} = Min	15		13		MHz
F_{BO}	Burst-Out Clock Rate	V_{CC} = Min	18		16		MHz
t_{OR}	Output Ready Delay	V_{CC} = Min, Test Load: V_{LOAD} = 2.2V		51		65	ns
t_{D}	Data Output Delay	V_{CC} = Min, Test Load: V_{LOAD} = 2.2V		50		65	ns
t_{HO}	Data Output Hold Time	V_{CC} = Min, Test Load: V_{LOAD} = 2.2V	15		15		ns
t_{MRW}	Master Reset Pulse Width	V_{CC} = Min	20		25		ns
t_{MRORL}	Master Reset to OR LOW	V_{CC} = Min, Test Load: V_{LOAD} = 2.2V		60		80	ns
t_{MRIRH}	Master Reset to IR HIGH	V_{CC} = Min, Test Load: V_{LOAD} = 2.2V		45		65	ns
t_{MRSI}	Master Reset to SI	V_{CC} = Min	55		65		ns
t_{IP}	Input Ready Pulse	V_{CC} = Min, Test Load: V_{LOAD} = 2.2V	40		45		ns
t_{OP}	Output Ready Pulse	V_{CC} = Min, Test Load: V_{LOAD} = 2.2V	45		50		ns
t_{DOF}	Data To Output Flag Delay	V_{CC} = Min, Test Load: V_{LOAD} = 2.2V	1		1		ns
t_{ENA}	Three-State Output Enable Delay	V_{CC} = Min, Test Load: V_{LOAD} = 1.8V		35		45	ns
t_{DIS}	Three-State Output Disable Delay	V_{CC} = Min, Test Load: V_{LOAD} = 2.6V for t_{DIS0}, 0.0V for t_{DIS1} [2]		30		40	ns

Notes:
1. All transitions are measured at a 1.5V level except for t_{DIS} and t_{ENA}, which are shown in Figure 15.
2. t_{DIS1} denotes the transition from logical 1 to three-state.
   t_{DIS0} denotes the transition from logical 0 to three-state.

Ordering Information

Product Number	Temperature Range	Screening	Package	Package Marking
TDC1030B6C	STD – T_A = 0°C to 70°C	Commercial	28 Pin CERDIP	1030B6C
TDC1030B6A	EXT – T_C = –55°C to 125°C	High Reliability	28 Pin CERDIP	1030B6A
TDC1030C3C	STD – T_A = 0°C to 70°C	Commercial	28 Contact Hermetic Ceramic Chip Carrier	1030C3C
TDC1030C3A	EXT – T_C = –55°C to 125°C	High Reliability	28 Contact Hermetic Ceramic Chip Carrier	1030C3A
TDC1030J6C	STD – T_A = 0°C to 70°C	Commercial	28 Pin Hermetic Ceramic DIP	1030J6C
TDC1030J6A	EXT – T_C = –55°C to 125°C	High Reliability	28 Pin Hermetic Ceramic DIP	1030J6A