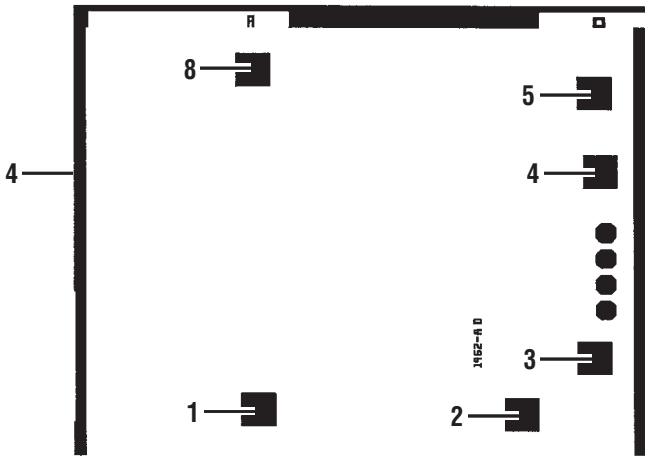
DICE/DWF SPECIFICATION

LT1962
300mA, Low Noise, Micropower LDO Regulator



74mils × 61mils,

PAD FUNCTION

1. OUT
2. ADJ
3. BYP
4. GND
5. SHDN
6. NC
7. NC
8. IN

DIE CROSS REFERENCE

LTC Finished Part Number	Order DICE CANDIDATE Part Number Below
LT1962	LT1962 DICE LT192 DWF*

Please refer to LTC standard product data sheet for other applicable product information.
***DWF = DICE in wafer form.**

ABSOLUTE MAXIMUM RATINGS

(Note 1)

IN Pin Voltage ..... ±20V
OUT Pin Voltage ..... ±20V
Input to Output Differential Voltage (Note 2) ..... ±20V
ADJ Pin Voltage ..... ±7V
BYP Pin Voltage ..... ±0.6V
SHDN Pin Voltage ..... ±20V
Output Short-Circuit Duration ..... Indefinite

DICE/DWF ELECTRICAL TEST LIMITS T_A = 25°C (Note 3)

PARAMETER	CONDITIONS	MIN	MAX	UNITS
ADJ Pin Voltage (Notes 4, 5)	V_{IN} = 2V, I_{LOAD} = 1mA	1.208	1.232	V
Line Regulation	ΔV_{IN} = 2V to 20V, I_{LOAD} = 1mA (Note 4)		5	mV
Load Regulation	V_{IN} = 2.3V, ΔI_{LOAD} = 1mA to 50mA (Note 4)		5	mV
Dropout Voltage (Notes 6, 7, 12) $V_{IN} = V_{OUT(NOMINAL)}$	I_{LOAD} = 10mA I_{LOAD} = 50mA		0.15 0.20	V V
GND Pin Current (Notes 6, 8) V_{IN} = 2.3V	I_{LOAD} = 0mA I_{LOAD} = 1mA I_{LOAD} = 50mA I_{LOAD} = 100mA		75 120 1.6 3	µA µA mA mA
ADJ Pin Bias Current	(Notes 4, 9)		100	nA
Shutdown Threshold	V_{OUT} = Off to On V_{OUT} = On to Off	 0.25	2	V V
$\overline{SHDN}$ Pin Current (Note 10)	$V_{\overline{SHDN}}$ = 0V $V_{\overline{SHDN}}$ = 20V		0.5 5	µA µA
Quiescent Current in Shutdown	V_{IN} = 6V, $V_{\overline{SHDN}}$ = 0V		1	µA
Input Reverse Leakage Current	V_{IN} = –20V, V_{OUT} = 0V		1	mA
Reverse Output Current (Note 11)	V_{OUT} = 1.22V, V_{IN} < 1.22V		10	µA

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: Absolute maximum input to output differential voltage cannot be achieved with all combinations of rated IN pin and OUT pin voltages. With the IN pin at 20V, the OUT pin may not be pulled below 0V. The total measured voltage from in to out can not exceed ±20V.

Note 3: The LT1962 regulators are tested and specified under pulse load conditions such that $T_J \approx T_A$. The LT1962 is 100% tested at T_A = 25°C.

Note 4: The LT1962 (adjustable version) is tested and specified for these conditions with the ADJ pin connected to the OUT pin.

Note 5: Operating conditions are limited by maximum junction temperature. The regulated output voltage specification will not apply for all possible combinations of input voltage and output current. When operating at maximum input voltage, the output current range must be limited. When operating at maximum output current, the input voltage range must be limited.

Note 6: To satisfy requirements for minimum input voltage, the LT1962 (adjustable version) is tested and specified for these conditions with an external resistor divider (two 250k resistors) for an output voltage of 2.44V. The external resistor divider will add a 5µA DC load on the output.

Note 7: Dropout voltage is the minimum input to output voltage differential needed to maintain regulation at a specified output current. In dropout, the output voltage will be equal to: $V_{IN} - V_{DROPOUT}$.

Note 8: GND pin current is tested with V_{IN} = 2.3V and a current source load. This means the device is tested while operating close to its dropout region. This is the worst-case GND pin current. The GND pin current will decrease slightly at higher input voltages.

Note 9: ADJ pin bias current flows into the ADJ pin.

Note 10: $\overline{SHDN}$ pin current flows into the $\overline{SHDN}$ pin. This current is included in the specification for GND pin current.

Note 11: Reverse output current is tested with the IN pin grounded and the OUT pin forced to the rated output voltage. This current flows into the OUT pin and out the GND pin.

Note 12: For the LT1962, dropout voltage will be limited by the minimum input voltage specification under some output voltage/load conditions. See the curve of Minimum Input Voltage in the Typical Performance Characteristics in the LT1962 data sheet.

Wafer level testing is performed per the indicated specifications for dice. Considerable differences in performance can often be observed for dice versus packaged units due to the influences of packaging and assembly on certain devices and/or parameters. Please consult factory for more information on dice performance and lot qualifications via lot sampling test procedures.

Dice data sheet subject to change. Please consult factory for current revision in production.

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