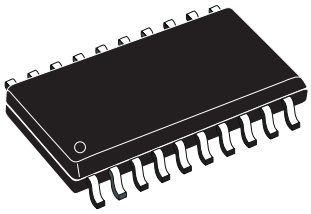
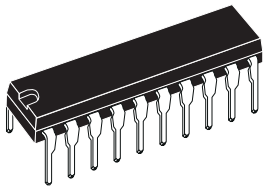
STV6400

DOUBLE SCART INTERFACE

- Two Periplugs I/O Source Management
- Two 150Ω Integrated Buffers for Plug Drive
- One Output with Muting Capability
- 3 Digital Buffer Outputs for external Switches Control
- Large Supply Voltage Range
- Bandwidth : 19 MHz typ.
- Crosstalk : 50 dB (Min.)
- I^2C Bus Control



SO20
(Plastic Package)



DIP20
(Plastic Package)

ORDER CODE: STV6400

DESCRIPTION

The STV6400 is a bipolar circuit for TV and VCR applications.

It is intended to process all switches relating to a 2 periplugs I/O application

Figure 1. PIN CONNECTIONS

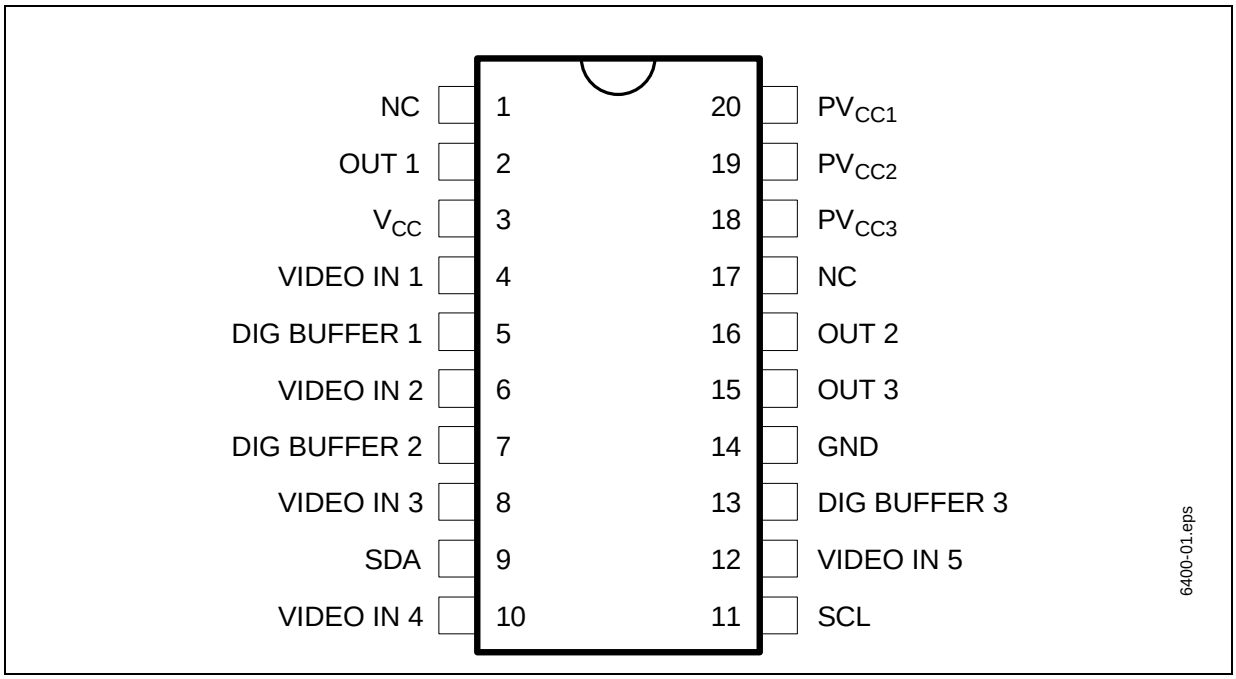
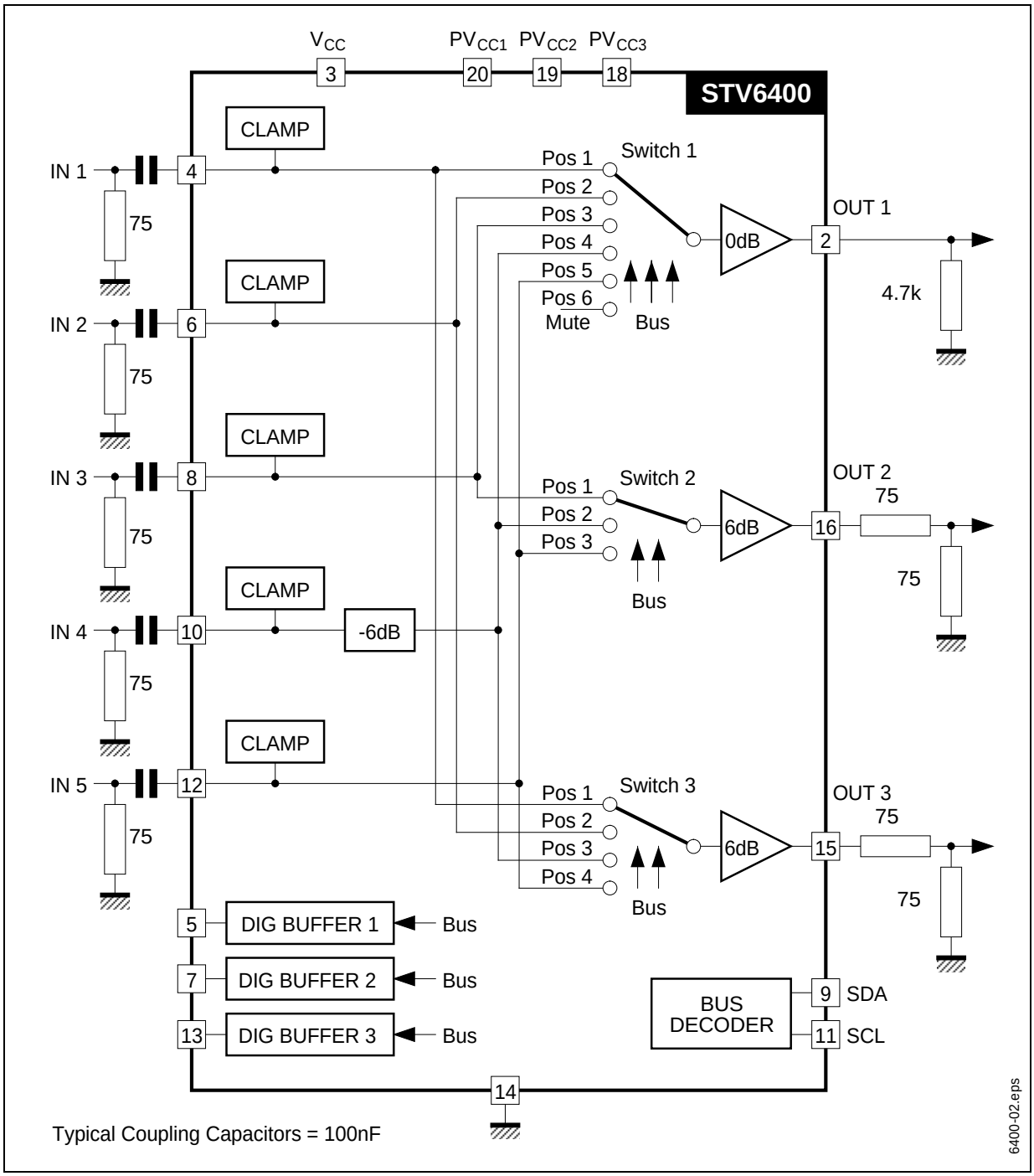


Figure 2. BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	12.0	V
T_{oper}	Operating Temperature	-10, + 70	^{o}C
T_{stg}	Storage Temperature	-55, + 150	^{o}C

THERMAL DATA

Symbol	Parameter		Value	Unit
R_{th} (j-a)	Junction-ambient Thermal Resistance	DIP20 SO20	70 100	°C/W °C/W

DC AND AC ELECTRICAL CHARACTERISTICS

V_{CC} = 5V, T_{amb} = 25^{oC} (Unless otherwise specified)
R_{LOAD} OUT 1= 4.7kΩ, R_{LOAD} OUT2 OUT3 = 150Ω, V_{IN} = 1V_{PP}

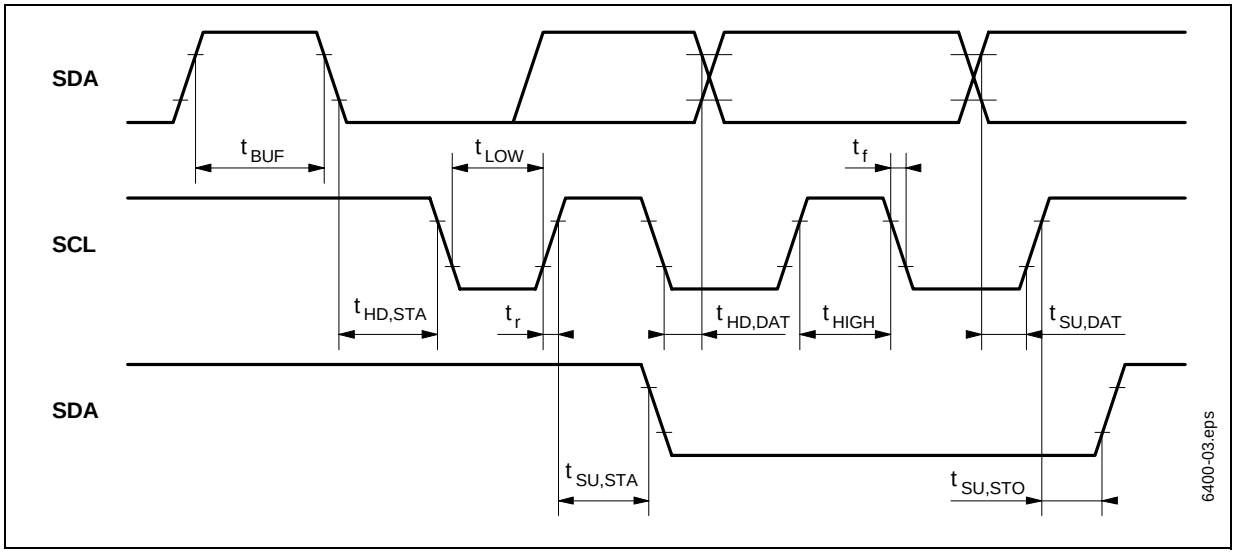
Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_{CC}	Operating Supply Voltage		4, 75	5	11.0	V
I_{CC}	Supply Current	Without loads		27	40	mA
Svr	Supply Voltage Rejection	1kHz		-36		dB
VIDEO INPUTS						
V_{DCIN}	DC Input Voltage (black level)			1, 4	4	V
I_{LCAK}	Leakage Current Input			1	3	µA
CAPIN	Input Capacitance			5		pF
V_{IN0}	Input Signal Amplitude	Video 4			2.5	V_{PP}
V_{IN6}	Input Signal Amplitude	Video 1 2 3 5			1.5	V_{PP}
VIDEO OUTPUTS						
DYN	Dynamic Output Signal (out 1)	V_{CC} = 5V	2, 5			V_{PP}
DYN	Dynamic Output Signal (out 1)	V_{CC} = 4.75V	2, 3			V_{PP}
DYN	Dynamic Output Signal (out 2, 3	V_{CC} = 5V V_{CC} = 4.75V	3 2.8			V_{PP} V_{PP}
BW0	0dB Gain Bandwidth at -3dB	V_{IN} = 1V_{PP}	10	23		MHz
BW6	6dB Gain Bandwidth at - 3dB	V_{IN} = 1V_{PP}	10	19		MHz
CT*	Crosstalk between Input 1, 2, 3, 5 and Output 2, 3	V_{IN} = 1V_{PP}, f = 5MHz		-62	-53	dB
CT*	Crosstalk between Input 4, and Output 2, 3	V_{IN4} = 2V_{PP}, f = 5MHz		-60	-52	dB
CT*	Crosstalk between Input 1, 2, 3, 5 and Output 1	V_{IN} = 1V_{PP}, f = 5MHz		-60	-55	dB
CT*	Crosstalk between Input 4 and Output 1	V_{IN4} = 2V_{PP}, f = 5MHz		-53	-50	dB
Z_{OUT}	Output Impedance			4	10	W
G_0	0dB Gain		-0.5	0	+0.5	dB
G_6	6dB Gain		5.5	6	6.5	dB
DCOUT	DC Output Voltage			0.7		V
DPH10	Differential Phase 0dB Output	V_{IN} =1V_{PP}		0.25		
DPHL6	Differential Phase 6dB Output	V_{IN} =1V_{PP}		0.5		
DGAIN0	Differential Gain 0dB Output	V_{IN} =1V_{PP}		1.5		%
DGAIN6	Differential Gain 6dB Output	V_{IN} =1V_{PP}		1.8		%
MUTE	Muting Suppression at Output 1	V_{IN} =1V_{PP}, f = 5MHz		-50	-45	dB
DIGITAL BUFFERS						
V_{OL}	Low Level Output Voltage	I = 3 mA			0, 4	V
Z_{OUT}	Output Resistance at High Level			30		kΩ
DCMAX	Max DC Voltage				V_{CC}	V

* DIP20 package.

I²C BUS CHARACTERISTICS

Symbol	Parameter	Test Conditions	Min.	Max.	Unit
SCL					
V_{IL}	Low Level Input Voltage		- 0.3	+ 1.5	V
V_{IH}	High Level Input Voltage		3.0	V_{CC} + 0.5	V
I_{LI}	Input Leakage Current	V_I = 0 to V_{CC}	- 10	+ 10	µA
f_{SCL}	Clock Frequency		0	100	kHz
t_R	Input Rise Time	1.5V to 3V		1000	ns
t_F	Input Fall Time	1.5V to 3V		300	ns
C_I	Input Capacitance			10	pF
SDA					
V_{IL}	Low Level Input Voltage		- 0.3	+ 1.5	V
V_{IH}	High Level Input Voltage		3.0	V_{CC} + 0.5	V
I_{LI}	Input Leakage Current	V_I = 0 to V_{CC}	- 10	+ 10	µA
C_I	Input Capacitance			10	pF
t_R	Input Rise Time	1.5V to 3V		1000	ns
t_F	Input Fall Time	1.5V to 3V		300	ns
V_{OL}	Low Level Output Voltage	I_{OL} = 3mA		0.4	V
t_F	Output Fall Time	3V to 1.5V		250	ns
C_L	Load Capacitance			400	pF
TIMING					
t_{LOW}	Clock Low Period		4.7		µs
t_{HIGH}	Clock High Period		4.0		µs
t_{SU}, DAT	Data Set-up Time		250		ns
t_{HD}, DAT	Data Hold Time		0	340	ns
t_{SU}, STO	Set-up Time from Clock High to Stop		4.0		µs
t_{BUF}	Start Set-up Time following a Stop		4.7		µs
t_{HD}, STA	Start Hold Time		4.0		µs
t_{SU}, STA	Start Set-up Time following Clock Low-to High Transition		4.7		µs

Figure 3. I²C Bus Timing



SOFTWARE SPECIFICATION

I^2C Address Byte

92 HEXA

DATA BYTE

B7	B6	B5	B4	B3	B2	B1	B0	
								SWITCH 1
X	X	0	0		0	0	0	POSITION 1 VIDEO IN 1
					0	0	1	POSITION 2 VIDEO IN 2
					0	1	0	POSITION 3 VIDEO IN 3
					0	1	1	POSITION 4 VIDEO IN 4
					1	0	0	POSITION 5 VIDEO IN 5
					1	0	1	POSITION 6 MUTE
					1	1	0	NOT ALLOWED
					1	1	1	NOT ALLOWED
								SWITCH 2
X	X	0	1		X	0	0	POSITION 1 VIDEO IN 3
					X	0	1	POSITION 2 VIDEO IN 4
					X	1	0	POSITION 3 VIDEO IN 5
					X	1	1	NOT ALLOWED
								SWITCH 2
X	X	1	0		X	0	0	POSITION 1 VIDEO IN 1
					X	0	1	POSITION 2 VIDEO IN 2
					X	1	0	POSITION 3 VIDEO IN 4
					X	1	1	POSITION 4 VIDEO IN 5
								DIGITAL BUFFER
X	X	1	1		X	X	1/0	DIG BUFFER 1
					X	1/0	X	DIG BUFFER 2
					1/0	X	X	DIG BUFFER 3

Remark : The letter "X" means dont't care.

Example : XX00X100 means. The switch 1 is connected to Video input 5

Example : XX11X011 means. Digital buffer 1 is at high level
Digital buffer 2 is at high level
Digital buffer 3 is at low level

The starting condition upon power-on is undetermined.
In this case 4 words of 16 bits are necessary to fix the device configuration.
In other case only one word of 16 bits is necessary to modify one configuration of the device.

INPUT/OUTPUT PIN CONFIGURATION

Figure 4.

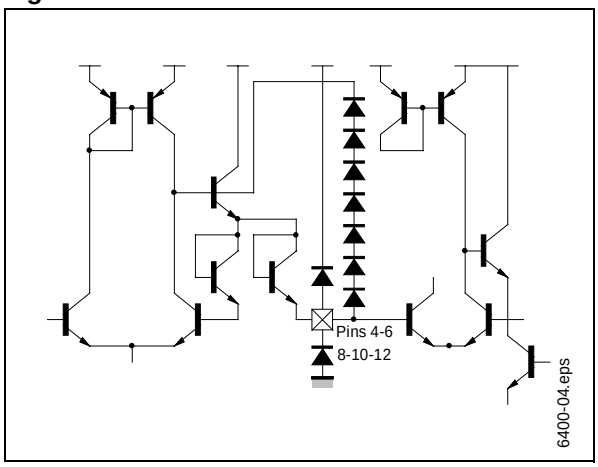


Figure 5.

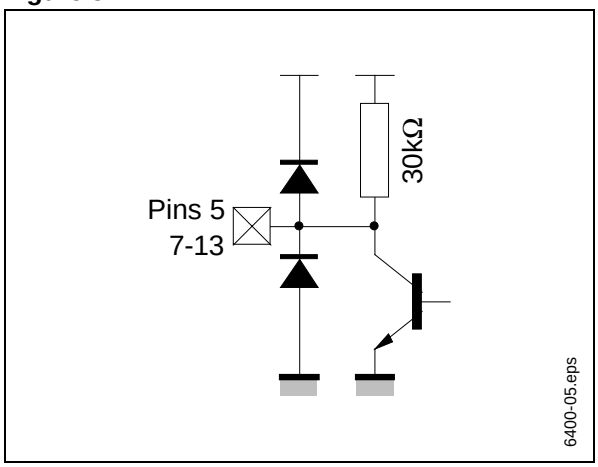


Figure 6.

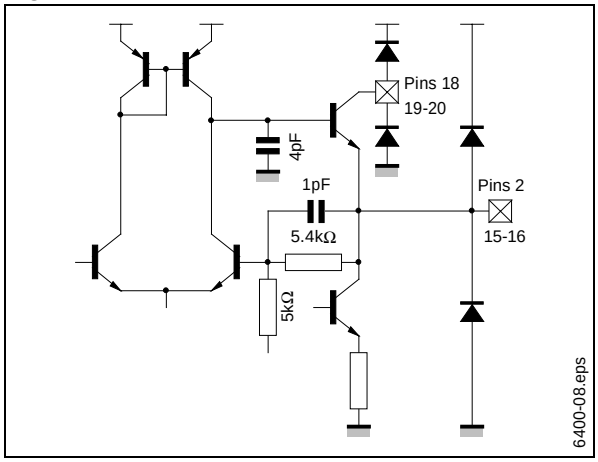


Figure 7.

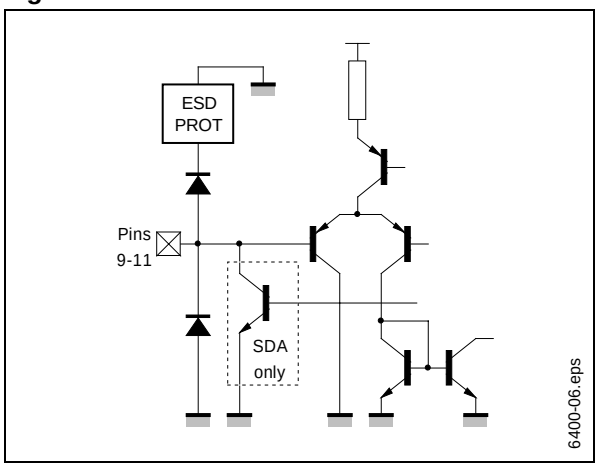
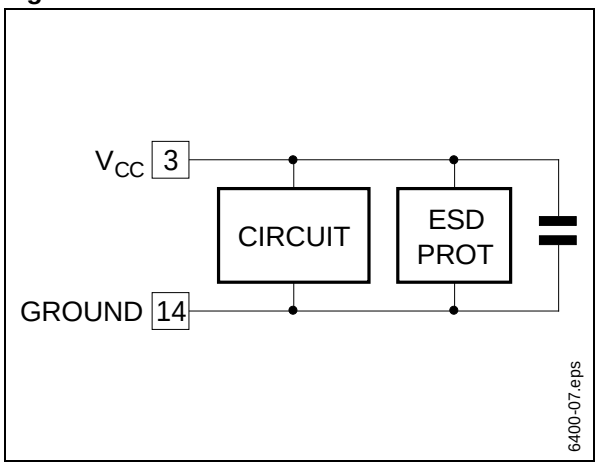


Figure 8.



TYPICAL APPLICATION

Figure 9.