

Active Errata List

- UART/Reception in Modes 1, 2 and 3/UART False Start Bits Detection
- During UART Reception, Clearing REN May Generate Unexpected IT
- Timer 2/Downcounter Mode/Double IT with Slow External Clock
- JBC/Double IT when External Interrupt Occurs During JBC Instruction
- On Start-up the Microcontroller Goes Into Test Mode

Errata History

Lot Number	Errata List
Z41648 and below	1, 2, 3, 4, 5
Z41648 and above	1, 2, 3, 4

Errata Description

1. UART/Reception in Modes 1, 2 and 3/UART False Start Bits Detection

When a false start bit occurs on the UART, some UART internal signals are not reset. Then when a real start bit occurs, the sampling is shifted.

Workaround

None.

2. During UART Reception, Clearing REN May Generate Unexpected IT

During UART reception, if the REN bit is cleared between a start bit detection and the end of reception, the UART will not discard the data (RI is set).

Workaround

Test REN at the beginning of the Interrupt routine just after CLR RI, and run the Interrupt routine code only if REN is set.

3. Timer 2/Countdown Mode/Double IT with Slow External Clock

Double IT with slow external clock in countdown mode. Timer 2 in 16-bit auto-reload in countdown mode with external clock input 2 interrupts are generated successively with low frequency on clock input (typ 10 - 40 kHz).

Workaround

Caution: Will not work if initially RCAP = 0x0000

Reload FFFE into TH2 - TL2 in ISR and countdown to RCAP-1 (to recover cycle lost in ISR).

4. JBC/Double IT when External Interrupt Occurs During JBC Instruction

On polling algorithm in ISR on IE1 or IE0 bit, when external IT appears during JBC instruction, flag is not cleared and next JBC sees another IT, then the same IT is seen twice.

Workaround

Use JB Instruction instead of JBC instruction to test bit and CLR instruction to clear it.



8051

Microcontrollers

T87C5101

T83C5101

T83C5102

Errata Sheet



5. On Start-up the Microcontroller Goes Into Test Mode

Under specific conditions (power lead edge, temperature and P3 value) on start-up T8xC5101/02 devices do not execute the user code. It goes into test mode and stays there.

Workaround

1. P3 = 0x00
2. Send another reset pulse a few machine cycles after the falling edge of the first reset pulse.



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