Active Errata List

- **UART/Reception in Modes 1, 2 and 3/UART False Start Bits Detection**
- **During UART Reception, Clearing REN May Generate Unexpected IT**
- **Timer 2/Downcounter Mode/Double IT with Slow External Clock**
- **JBC/Double IT when External Interrupt Occurs During JBC Instruction**
- **On Start-up the Microncontroller Goes Into Test Mode**

Errata History

Lot Number	Errata List
Z41648 and below	1, 2, 3, 4, 5
Z41648 and above	**1, 2, 3, 4**

Errata Description

1. UART/Reception in Modes 1, 2 and 3/UART False Start Bits Detection

When a false start bit occurs on the UART, some UART internal signals are not reset. Then when a real start bit occurs, the sampling is shifted.

Workaround

None.

2. During UART Reception, Clearing REN May Generate Unexpected IT

During UART reception, if the REN bit is cleared between a start bit detection and the end of reception, the UART will not discard the data (RI is set).

Workaround

Test REN at the beginning of the Interrupt routine just after CLR RI, and run the Interrupt routine code only if REN is set.

3. Timer 2/Countdown Mode/Double IT with Slow External Clock

Double IT with slow external clock in countdown mode. Timer 2 in 16-bit auto-reload in countdown mode with external clock input 2 interrupts are generated successively with low frequency on clock input (typ 10 - 40 kHz).

Workaround

Caution: Will not work if initially RCAP = 0x0000

Reload FFFE into TH2 - TL2 in ISR and countdown to RCAP-1 (to recover cycle lost in ISR).

4. JBC/Double IT when External Interrupt Occurs During JBC Instruction

On polling algorithm in ISR on IE1 or IE0 bit, when external IT appears during JBC instruction, flag is not cleared and next JBC sees another IT, then the same IT is seen twice.

Workaround

Use JB Instruction instead of JBC instruction to test bit and CLR instruction to clear it.

8051 Microcontrollers

T87C5101
T83C5101
T83C5102
Errata Sheet

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5. On Start-up the Microcontroller Goes Into Test Mode

Under specific conditions (power lead edge, temperature and P3 value) on start-up T8xC5101/02 devices do not execute the user code. It goes into test mode and stays there.

Workaround

1. P3 = 0x00
2. Send another reset pulse a few machine cycles after the falling edge of the first reset pulse.

Atmel Headquarters

Corporate Headquarters
2325 Orchard Parkway
San Jose, CA 95131
TEL 1(408) 441-0311
FAX 1(408) 487-2600

Europe
Atmel Sarl
Route des Arsenaux 41
Case Postale 80
CH-1705 Fribourg
Switzerland
TEL (41) 26-426-5555
FAX (41) 26-426-5500

Asia
Room 1219
Chinachem Golden Plaza
77 Mody Road Tsimhatsui
East Kowloon
Hong Kong
TEL (852) 2721-9778
FAX (852) 2722-1369

Japan
9F, Tonetsu Shinkawa Bldg.
1-24-8 Shinkawa
Chuo-ku, Tokyo 104-0033
Japan
TEL (81) 3-3523-3551
FAX (81) 3-3523-7581

Atmel Operations

Memory
2325 Orchard Parkway
San Jose, CA 95131
TEL 1(408) 441-0311
FAX 1(408) 436-4314

Microcontrollers
2325 Orchard Parkway
San Jose, CA 95131
TEL 1(408) 441-0311
FAX 1(408) 436-4314

La Chantrerie
BP 70602
44306 Nantes Cedex 3, France
TEL (33) 2-40-18-18-18
FAX (33) 2-40-18-19-60

ASIC/ASSP/Smart Cards
Zone Industrielle
13106 Rousset Cedex, France
TEL (33) 4-42-53-60-00
FAX (33) 4-42-53-60-01

1150 East Cheyenne Mtn. Blvd.
Colorado Springs, CO 80906
TEL 1(719) 576-3300
FAX 1(719) 540-1759

Scottish Enterprise Technology Park
Maxwell Building
East Kilbride G75 0QR, Scotland
TEL (44) 1355-803-000
FAX (44) 1355-242-743

RF/Automotive
Theresienstrasse 2
Postfach 3535
74025 Heilbronn, Germany
TEL (49) 71-31-67-0
FAX (49) 71-31-67-2340

1150 East Cheyenne Mtn. Blvd.
Colorado Springs, CO 80906
TEL 1(719) 576-3300
FAX 1(719) 540-1759

Biometrics/Imaging/Hi-Rel MPU/ High Speed Converters/RF Data-com
Avenue de Rochepleine
BP 123
38521 Saint-Egreve Cedex, France
TEL (33) 4-76-58-30-00
FAX (33) 4-76-58-34-80

e-mail
literature@atmel.com

Web Site
http://www.atmel.com

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