64M x 72 DDR2 SDRAM 208 PBGA Multi-Chip Package

FEATURES

- Data rate = 667*, 533, 400
- Package:
  - 208 Plastic Ball Grid Array (PBGA), 17 x 23mm
  - 1.0mm pitch
- DDR2 Data Rate = 667*, 533, 400
- Core Supply Voltage = 1.8V ± 0.1V
- I/O Supply Voltage = 1.8V ± 0.1V - (SSTL_18 compatible)
- Differential data strobe (DQS, DQS#) per byte
- Internal, pipelined, double data rate architecture
- 4-bit prefetch architecture
- DLL for alignment of DQ and DQS transitions with clock signal
- Eight internal banks for concurrent operation (Per DDR2 SDRAM Die)
- Programmable Burst lengths: 4 or 8
- Auto Refresh and Self Refresh Modes
- On Die Termination (ODT)
- Adjustable data – output drive strength
- Programmable CAS latency: 3, 4 or 5
- Posted CAS additive latency: 0, 1, 2, 3 or 4
- Write latency = Read latency - 1* ^{t}CK
- Commercial, Industrial and Military Temperature Ranges
- Organized as 64M x 72
- Weight: W3H64M72E-XSBX - 2.5 grams typical

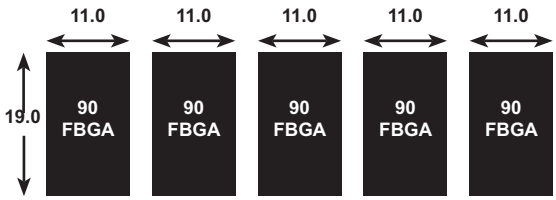
BENEFITS

- 63% SPACE SAVINGS vs. FPBGA
- Reduced part count
- 55% I/O reduction vs FPBGA
- Reduced trace lengths for lower parasitic capacitance
- Suitable for hi-reliability applications
- Upgradable to 128M x 72 density (contact factory for information)

* This product is under development, is not qualified or characterized and is subject to change or cancellation without notice.

FIGURE 1 – DENSITY COMPARISONS

	CSP Approach (mm)	Actual Size W3H64M72E-XSBX	SAVINGS
Area	5 x 209mm² = 1,045mm²	391mm²	63%
I/O Count	5 x 92 balls = 460 balls	208 Balls	55%



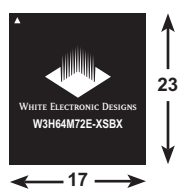


FIGURE 2 – FUNCTIONAL BLOCK DIAGRAM

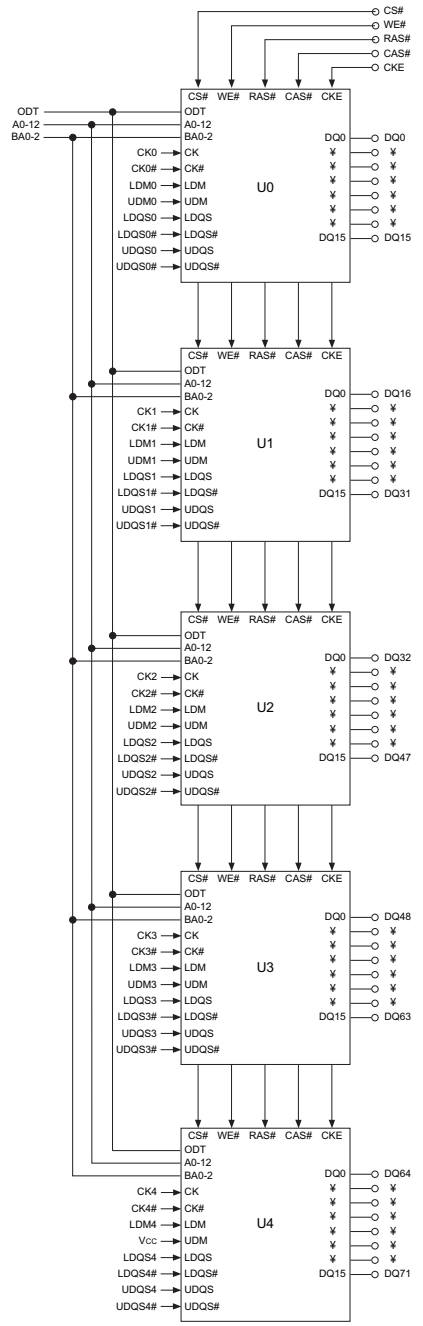
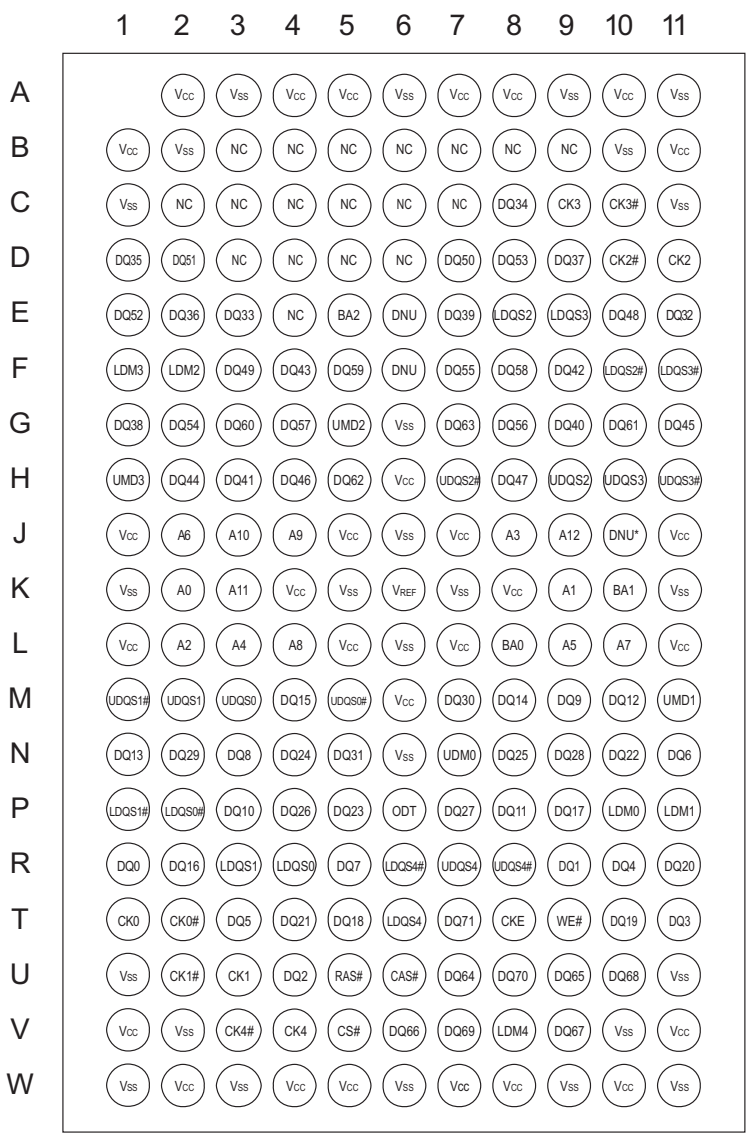


FIGURE 3 - PIN CONFIGURATION

TOP VIEW



* Pin J10 is reserved for signal A13 on 128Mx72 and higher densities.
Note: UDQS4 and UDQS4# require a 10KΩ pull up resistor.

TABLE 1 – BALL DESCRIPTIONS

Symbol	Type	Description
ODT	Input	On-Die termination: ODT (registered HIGH) enables termination resistance internal to the DDR2 SDRAM. When enabled, ODT is only applied to each of the following balls: DQ0–DQ71, LDM, UDM, LDQS, LDQS#, UDQS, and UDQS#. The ODT input will be ignored if disabled via the LOAD MODE command.
CK, CK#	Input	Clock: CK and CK# are differential clock inputs. All address and control input signals are sampled on the crossing of the positive edge of CK and negative edge of CK#. Output data (DQs and DQS/DQS#) is referenced to the crossings of CK and CK#.
CKE	Input	Clock enable: CKE (registered HIGH) activates and CKE (registered LOW) deactivates clocking circuitry on the DDR2 SDRAM. The specific circuitry that is enabled/disabled is dependent on the DDR2 SDRAM configuration and operating mode. CKE LOW provides PRECHARGE power-down mode and SELF-REFRESH action (all banks idle), or ACTIVE power-down (row active in any bank). CKE is synchronous for power-down entry, Power-down exit, output disable, and for self refresh entry. CKE is asynchronous for self refresh exit. Input buffers (excluding CKE, and ODT) are disabled during power-down. Input buffers (excluding CKE) are disabled during self refresh. CKE is an SSTL_18 input but will detect a LVCMO SLOW level once V_{CC} is applied during first power-up. After V_{REF} has become stable during the power on and initialization sequence, it must be maintained for proper operation of the CKE receiver. For proper SELF-REFRESH operation, V_{REF} must be maintained.
CS#	Input	Chip select: CS# enables (registered LOW) and disables (registered HIGH) the command decoder. All commands are masked when CS# is registered HIGH.
RAS#, CAS#, WE#	Input	Command inputs: RAS#, CAS#, WE# (along with CS#) define the command being entered.
LDM, UDM	Input	Input data mask: DM is an input mask signal for write data. Input data is masked when DM is concurrently sampled HIGH during a WRITE access. DM is sampled on both edges of DQS. Although DM balls are input-only, the DM loading is designed to match that of DQ and DQS balls. LDM is DM for lower byte DQ0–DQ7 and UDM is DM for upper byte DQ8–DQ15, of each of U0-U4
BA0–BA2	Input	Bank address inputs: BA0–BA2 define to which bank an ACTIVE, READ, WRITE, or PRECHARGE command is being applied. BA0–BA2 define which mode register including MR, EMR, EMR(2), and EMR(3) is loaded during the LOAD MODE command.

Continued on next page

TABLE – 1 BALL DESCRIPTIONS (continued)

A0-A12	Input	Address inputs: Provide the row address for ACTIVE commands, and the column address and auto precharge bit (A10) for READ/WRITE commands, to select one location out of the memory array in the respective bank. A10 sampled during a PRECHARGE command determines whether the PRECHARGE applies to one bank (A10 LOW, bank selected by BA2–BA0) or all banks (A10 HIGH) The address inputs also provide the op-code during a LOAD MODE command.
DQ0-71	I/O	Data input/output: Bidirectional data bus
UDQS, UDQS#	I/O	Data strobe for upper byte: Output with read data, input with write data for source synchronous operation. Edge-aligned with read data, center-aligned with write data. UDQS# is only used when differential data strobe mode is enabled via the LOAD MODE command.
LDQS, LDQS#	I/O	Data strobe for lower byte: Output with read data, input with write data for source synchronous operation. Edge-aligned with read data, center-aligned with write data. LDQS# is only used when differential data strobe mode is enabled via the LOAD MODE command.
V_{CC}	Supply	Power Supply: 1.8V ±0.1V
V_{CCQ}	Supply	DQ Power supply: 1.8V ±0.1V. Isolated on the device for improved noise immunity
V_{REF}	Supply	SSTL_18 reference voltage.
V_{SS}	Supply	Ground
NC	-	No connect: These balls should be left unconnected.
DNU	-	Future use; address bits A14 and A15 are reserved for future densities.

DESCRIPTION

The 4Gb DDR2 SDRAM is a high-speed CMOS, dynamic random-access memory containing 4,294,967,296 bits. Each of the five chips in the MCP are internally configured as 8-bank DRAM. The block diagram of the device is shown in Figure 2. Ball assignments and are shown in Figure 3.

The 4Gb DDR2 SDRAM uses a double-data-rate architecture to achieve high-speed operation. The double data rate architecture is essentially a 4*n*-prefetch architecture, with an interface designed to transfer two data words per clock cycle at the I/O balls. A single read or write access for the 4Gb DDR2 SDRAM effectively consists of a single 4*n*-bit-wide, one-clock-cycle data transfer at the internal DRAM core and four corresponding *n*-bit-wide, one-half-clock-cycle data transfers at the I/O balls.

A bidirectional data strobe (DQS, DQS#) is transmitted externally, along with data, for use in data capture at the receiver. DQS is a strobe transmitted by the DDR2 SDRAM during READs and by the memory controller during WRITEs. DQS is edge-aligned with data for READs and center-aligned with data for WRITEs. There are strobes, one for the lower byte (LDQS, LDQS#) and one for the upper byte (UDQS, UDQS#).

The 4Gb DDR2 SDRAM operates from a differential clock (CK and CK#); the crossing of CK going HIGH and CK# going LOW will be referred to as the positive edge of CK. Commands (address and control signals) are registered at every positive edge of CK. Input data is registered on both edges of DQS, and output data is referenced to both edges of DQS, as well as to both edges of CK.

Read and write accesses to the DDR2 SDRAM are burst oriented; accesses start at a selected location and continue for a programmed number of locations in a programmed sequence. Accesses begin with the registration of an ACTIVE command, which is then followed by a READ or WRITE command. The address bits registered coincident with the ACTIVE command are used to select the bank and row to be accessed. The address bits registered coincident with the READ or WRITE command are used to select the bank and the starting column location for the burst access.

The DDR2 SDRAM provides for programmable read or write burst lengths of four or eight locations. DDR2 SDRAM supports interrupting a burst read of eight with another read, or a burst write of eight with another write.

An auto precharge function may be enabled to provide a self-timed row precharge that is initiated at the end of the burst access.

As with standard DDR SDRAMs, the pipelined, multibank architecture of DDR2 SDRAMs allows for concurrent operation, thereby providing high, effective bandwidth by hiding row precharge and activation time.

A self refresh mode is provided, along with a power-saving power-down mode.

All inputs are compatible with the JEDEC standard for SSTL_18. All full drive-strength outputs are SSTL_18-compatible.

GENERAL NOTES

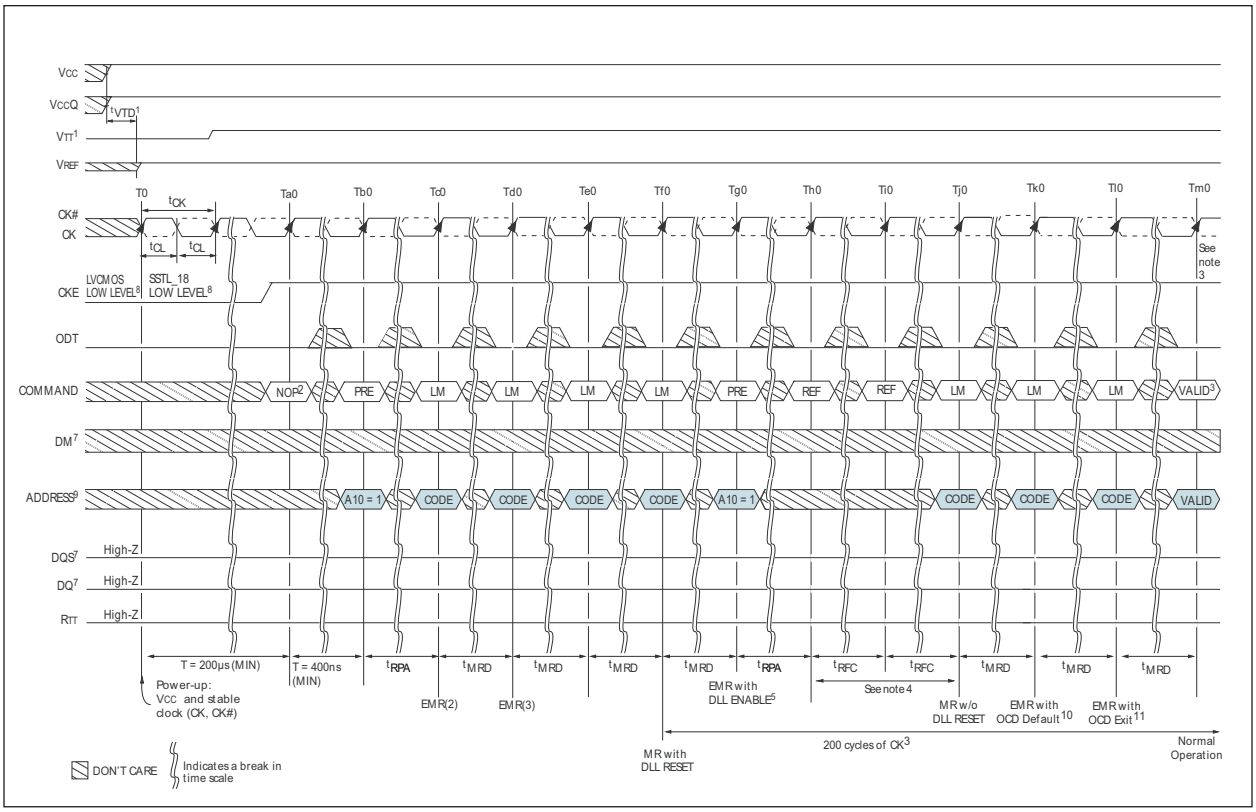
- The functionality and the timing specifications discussed in this data sheet are for the DLL-enabled mode of operation.
- Throughout the data sheet, the various figures and text refer to DQs as “DQ.” The DQ term is to be interpreted as any and all DQ collectively, unless specifically stated otherwise. Additionally, each chip is divided into 2 bytes, the lower byte and upper byte. For the lower byte (DQ0–DQ7), DM refers to LDM and DQS refers to LDQS. For the upper byte (DQ8–DQ15), DM refers to UDM and DQS refers to UDQS. Note that the there is no upper byte for U4 and therefore no UDM4.
- Complete functionality is described throughout the document and any page or diagram may have been simplified to convey a topic and may not be inclusive of all requirements.
- Any specific requirement takes precedence over a general statement.

INITIALIZATION

DDR2 SDRAMs must be powered up and initialized in a predefined manner. Operational procedures other than those specified may result in undefined operation. The following sequence is required for power up and initialization and is shown in Figure 4 on page 8.

FIGURE 4 – POWER-UP AND INITIALIZATION

Notes appear on page 9



NOTES:

1. Applying power; if CKE is maintained below 0.2 x V_{CCQ}, outputs remain disabled. To guarantee R_{TT} (ODT resistance) is off, VREF must be valid and a low level must be applied to the ODT ball (all other inputs may be undefined, I/Os and outputs must be less than V_{CCQ} during voltage ramp time to avoid DDR2 SDRAM device latch-up). At least one of the following two sets of conditions (A or B) must be met to obtain a stable supply state (stable supply defined as V_{CC}, V_{CCQ},V_{REF}, and V_{TT} are between their minimum and maximum values as stated in DC Operating Conditions table):
   A. (single power source) The V_{CC} voltage ramp from 300mV to V_{CC} (MIN) must take no longer than 200ms; during the V_{CC} voltage ramp, $|V_{CC} - V_{CCQ}| \leq 0.3V$. Once supply voltage ramping is complete (when V_{CCQ} crosses V_{CC} (MIN), DC Operating Conditions table specifications apply.
      - V_{CC}, V_{CCQ} are driven from a single power converter output
      - V_{TT} is limited to 0.95V MAX
      - V_{REF} tracks $V_{CCQ/2}$; V_{REF} must be within ±0.3V with respect to $V_{CCQ/2}$ during supply ramp time.
      - $V_{CCQ} \geq V_{REF}$ at all times
   B. (multiple power sources) $V_{CC} \geq V_{CCQ}$ must be maintained during supply voltage ramping, for both AC and DC levels, until supply voltage ramping completes (V_{CCQ} crosses V_{CC} [MIN]). Once supply voltage ramping is complete, DC Operating Conditions table specifications apply.
      - Apply V_{CC} before or at the same time as V_{CCQ}; V_{CC} voltage ramp time must be ≤ 200ms from when V_{CC} ramps from 300mV to V_{CC} (MIN)
      - Apply V_{CCQ} before or at the same time as V_{TT}; the V_{CCQ} voltage ramp time from when V_{CC} (MIN) is achieved to when V_{CCQ} (MIN) is achieved must be ≤ 500ms; while V_{CC} is ramping, current can be supplied from V_{CC} through the device to V_{CCQ}
      - V_{REF} must track $V_{CCQ/2}$, V_{REF} must be within ±0.3V with respect to $V_{CCQ/2}$ during supply ramp time; $V_{CCQ} \geq V_{REF}$ must be met at all times
      - Apply V_{TT}; The V_{TT} voltage ramp time from when V_{CCQ} (MIN) is achieved to when V_{TT} (MIN) is achieved must be no greater than 500ms
2. CKE uses LVCMOS input levels prior to state T0 to ensure DQs are High-Z during device power-up prior to V_{REF}. being stable. After state T0, Cke is required to have SSTL_18 input levels. Once CKE transitions to a high level, it must stay HIGH for the duration on the initialization sequence.
3. PRE = PRECHARGE command, LM = LOAD MODE command, MR = Mode Register, EMR = extended mode register, EMR2 = extended mode register 2, EMR3 = extended mode register 3, REF = REFRESH command, ACT = ACTIVE command, A10 = PRECHARGE ALL, CODE = desired value for mode registers (blank addresses are required to be decoded), VALID - any valid command/ address, RA = row address, bank address.
4. DM represents UDM & LDM, DQS represents, UDQS, UDQS#, LDQS, LDQS#, RDQS, RDQS#, DQ represents DQ0-71.
5. For a minimum of 200µs after stable power and clock (CK, CK#), apply NOP or DESELECT commands, then take CKE HIGH.
6. Wait a minimum of 400ns, then issue a PRECHARGE ALL command.
7. Issue a LOAD MODE command to the EMR(2). (To issue an EMR(3) command, provide LOW to BA2 and BA0, and provide HIGH to BA1.) Set register E7 to "0" or "1;" all others must be "0".
8. Issue LOAD MODE command to the EMR(3). (to issue and EMR(3) command, provide HIGH to BA0 = 1, BA1 = 1, and BA2 = 0.) Set all registers to "0".
9. Issue a LOAD MODE command to the EMR to enable DLL. To issue a CLL ENABLE command provide LOW to BA1, BA2 and A0; provide HIGH to BA0. Bits E7, E8 and E9 can be set to "0" or "1;" Micron recommends setting them to "0".
10. Issue a LOAD MODE command for DLL RESET. 200 cycles of clock input is required to lock the DLL. (To issue a DLL RESET, provide HIGH to A8 and provide LOW to BA2 = BA1 = BA0 = 0.) CKE must be HIGH the entire time. .
11. Issue PRECHARGE ALL command.
12. Issue two or more REFRESH commands.
13. Issue a LOAD MODE command with LOW to A8 to initialize device operation (i.e., to program operating parameters without resetting the DLL). To access the mode registers, BA0 = 0, BA1 = 0, BA2 = 0.
14. Issue a LOAD MODE command to the EMR to enable OCD default by setting bits E7, E8, and E9 to "1," and then setting all other desired parameters. To access the extended mode register, BA2 = 0, BA1 = 0, BA0 = 1.
15. Issue a LOAD MODE command to the EMR to enable OCD exit by setting bits E7, E8, and E9 to "0," and then setting all other desired parameters. To access the extended mode registers, BA2 = 0, BA1 = 0, BA0 = 1.
16. The DDR2 SDRAM is now initialized and ready for normal operation 200 clock cycles after the DLL RESET at Tf0.

MODE REGISTER (MR)

The mode register is used to define the specific mode of operation of the DDR2 SDRAM. This definition includes the selection of a burst length, burst type, CL, operating mode, DLL RESET, write recovery, and power-down mode, as shown in Figure 5. Contents of the mode register can be altered by re-executing the LOAD MODE (LM) command. If the user chooses to modify only a subset of the MR variables, all variables (M0–M14) must be programmed when the command is issued.

The mode register is programmed via the LM command (bits BA2–BA0 = 0, 0, 0) and other bits (M12–M0) will retain the stored information until it is programmed again or the device loses power (except for bit M8, which is self-clearing). Reprogramming the mode register will not alter the contents of the memory array, provided it is performed correctly.

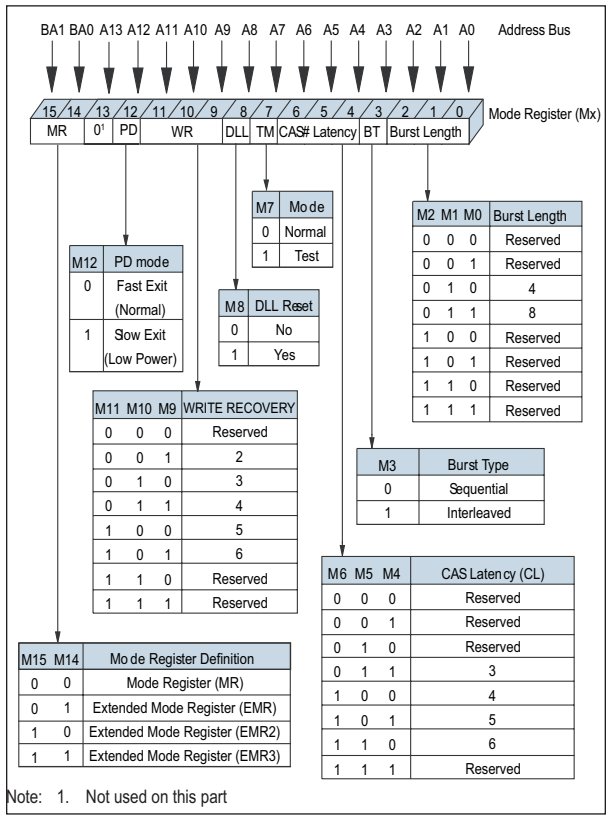
The LM command can only be issued (or reissued) when all banks are in the precharged state (idle state) and no bursts are in progress. The controller must wait the specified time ^{t}MRD before initiating any subsequent operations such as an ACTIVE command. Violating either of these requirements will result in unspecified operation.

BURST LENGTH

Burst length is defined by bits M0–M3, as shown in Figure 5. Read and write accesses to the DDR2 SDRAM are burst-oriented, with the burst length being programmable to either four or eight. The burst length dete rmines the maximum number of column locations that can be accessed for a given READ or WRITE command.

When a READ or WRITE command is issued, a block of columns equal to the burst length is effectively selected. All accesses for that burst take place within this block, meaning that the burst will wrap within the block if a boundary is reached. The block is uniquely selected by A2–Ai when BL = 4 and by A3–Ai when BL = 8 (where Ai is the most significant column address bit for a given configuration). The remaining (least significant) address bit(s) is (are) used to select the starting location within the block. The programmed burst length applies to both READ and WRITE bursts.

FIGURE 5 – MODE REGISTER (MR) DEFINITION



Note: 1. Not used on this part

BURST TYPE

Accesses within a given burst may be programmed to be either sequential or interleaved. The burst type is selected via bit M3, as shown in Figure 5. The ordering of accesses within a burst is determined by the burst length, the burst type, and the starting column address, as shown in Table 2. DDR2 SDRAM supports 4-bit burst mode and 8-bit burst mode only. For 8-bit burst mode, full interleave address ordering is supported; however, sequential address ordering is nibble-based.

TABLE 2 – BURST DEFINITION

Burst Length	Starting Column Address			Order of Accesses Within a Burst	
				Type = Sequential	Type = Interleaved
4		A1	A0		
		0	0	0-1-2-3	0-1-2-3
		0	1	1-2-3-0	1-0-3-2
		1	0	2-3-0-1	2-3-0-1
		1	1	3-0-1-2	3-2-1-0
8	A2	A1	A0		
	0	0	0	0-1-2-3-4-5-6-7	0-1-2-3-4-5-6-7
	0	0	1	1-2-3-0-5-6-7-4	1-0-3-2-5-4-7-6
	0	1	0	2-3-0-1-6-7-4-5	2-3-0-1-6-7-4-5
	0	1	1	3-0-1-2-7-4-5-6	3-2-1-0-7-6-5-4
	1	0	0	4-5-6-7-0-1-2-3	4-5-6-7-0-1-2-3
	1	0	1	5-6-7-4-1-2-3-0	5-4-7-6-1-0-3-2
	1	1	0	6-7-4-5-2-3-0-1	6-7-4-5-2-3-0-1
	1	1	1	7-4-5-6-3-0-1-2	7-6-5-4-3-2-1-0

NOTES:
1. For a burst length of two, A1-Ai select two-data-element block; A0 selects the starting column within the block.
2. For a burst length of four, A2-Ai select four-data-element block; A0-1 select the starting column within the block.
3. For a burst length of eight, A3-Ai select eight-data-element block; A0-2 select the starting column within the block.
4. Whenever a boundary of the block is reached within a given sequence above, the following access wraps within the block.

OPERATING MODE

The normal operating mode is selected by issuing a command with bit M7 set to "0," and all other bits set to the desired values, as shown in Figure 5. When bit M7 is "1," no other bits of the mode register are programmed. Programming bit M7 to "1" places the DDR2 SDRAM into a test mode that is only used by the manufacturer and should not be used. No operation or functionality is guaranteed if M7 bit is '1.'

DLL RESET

DLL RESET is defined by bit M8, as shown in Figure 5. Programming bit M8 to "1" will activate the DLL RESET function. Bit M8 is self-clearing, meaning it returns back to a value of "0" after the DLL RESET function has been issued.

Anytime the DLL RESET function is used, 200 clock cycles must occur before a READ command can be issued to allow time for the internal clock to be synchronized with the external clock. Failing to wait for synchronization to occur may result in a violation of the ^{t}AC or ^{t}DQSCK parameters.

WRITE RECOVERY

Write recovery (WR) time is defined by bits M9–M11, as shown in Figure 5. The WR register is used by the DDR2 SDRAM during WRITE with auto precharge operation. During WRITE with auto precharge operation, the DDR2 SDRAM delays the internal auto precharge operation by WR clocks (programmed in bits M9–M11) from the last data burst.

WR values of 2, 3, 4, 5, or 6 clocks may be used for programming bits M9–M11. The user is required to program the value of WR, which is calculated by dividing ^{t}WR (in ns) by ^{t}CK (in ns) and rounding up a non integer value to the next integer; WR [cycles] = ^{t}WR [ns] / ^{t}CK [ns]. Reserved states should not be used as unknown operation or incompatibility with future versions may result.

POWER-DOWN MODE

Active power-down (PD) mode is defined by bit M12, as shown in Figure 5. PD mode allows the user to determine the active power-down mode, which determines performance versus power savings. PD mode bit M12 does not apply to precharge PD mode.

When bit M12 = 0, standard active PD mode or "fast-exit" active PD mode is enabled. The ^{t}XARD parameter is used for fast-exit active PD exit timing. The DLL is expected to be enabled and running during this mode.

When bit M12 = 1, a lower-power active PD mode or "slow-exit" active PD mode is enabled. The ^{t}XARD parameter is used for slow-exit active PD exit timing. The DLL can be enabled, but "frozen" during active PD mode since the exit-to-READ command timing is relaxed. The power difference expected between PD normal and PD low-power mode is defined in the I_{CC} table.

CAS LATENCY (CL)

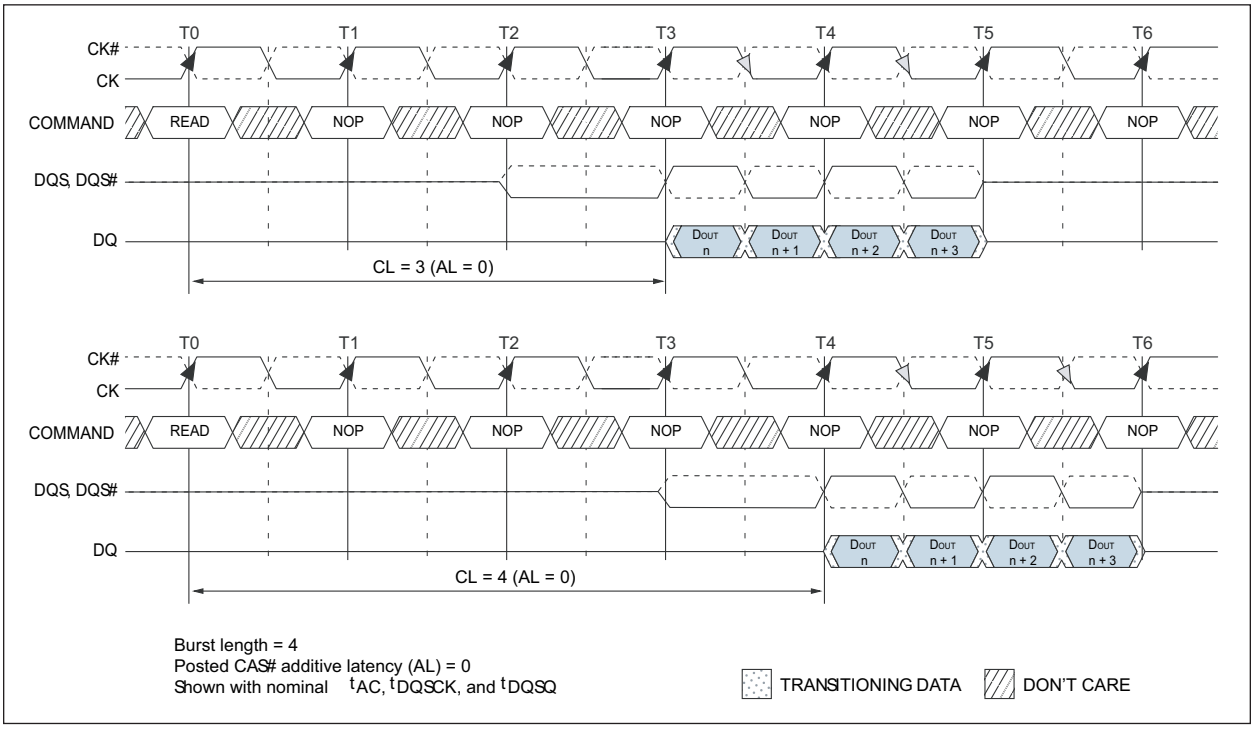
The CAS latency (CL) is defined by bits M4–M6, as shown in Figure 5. CL is the delay, in clock cycles, between the registration of a READ command and the availability of the first bit of output data. The CL can be set to 3, 4, 5, or 6 clocks, depending on the speed grade option being used.

DDR2 SDRAM does not support any half-clock latencies. Reserved states should not be used as unknown operation or incompatibility with future versions may result.

DDR2 SDRAM also supports a feature called posted CAS additive latency (AL). This feature allows the READ command to be issued prior to ^{t}RCD (MIN) by delaying the internal command to the DDR2 SDRAM by AL clocks.

Examples of CL = 3 and CL = 4 are shown in Figure 6; both assume AL = 0. If a READ command is registered at clock edge *n*, and the CL is *m* clocks, the data will be available nominally coincident with clock edge *n+m (this assumes AL = 0).*

FIGURE 6 – CAS LATENCY (CL)

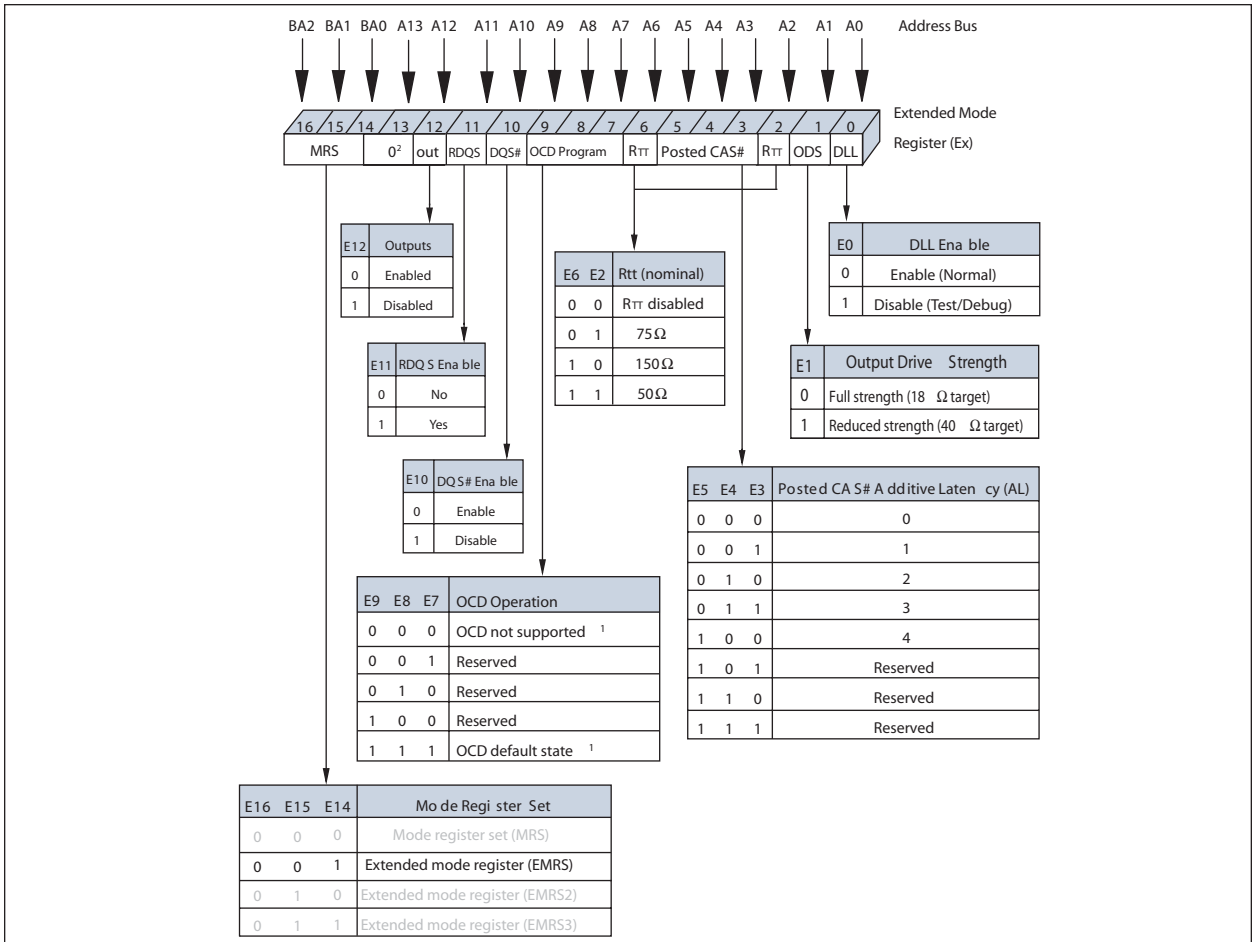


EXTENDED MODE REGISTER (EMR)

The extended mode register controls functions beyond those controlled by the mode register; these additional functions are DLL enable/disable, output drive strength, on die termination (ODT) (RTT), posted AL, off-chip driver impedance calibration (OCD), DQS# enable/disable, RDQS/RDQS# enable/disable, and output disable/enable. These functions are controlled via the bits shown in Figure 7. The EMR is programmed via the LOAD MODE (LM) command and will retain the stored information until it is programmed again or the device loses power. Reprogramming the EMR will not alter the contents of the memory array, provided it is performed correctly.

The EMR must be loaded when all banks are idle and no bursts are in progress, and the controller must wait the specified time ^{t}MRD before initiating any subsequent operation. Violating either of these requirements could result in unspecified operation.

FIGURE 7 – EXTENDED MODE REGISTER DEFINITION



Note: 1. During initialization, all three bits must be set to "1" for OCD default state, then must be set to "0" before initialization is finished, as detailed in the initialization procedure.
2.. E13 (A13) is not used on this device.

DLL ENABLE/DISABLE

The DLL may be enabled or disabled by programming bit E0 during the LM command, as shown in Figure 7. The DLL must be enabled for normal operation. DLL enable is required during power-up initialization and upon returning to normal operation after having disabled the DLL for the purpose of debugging or evaluation. Enabling the DLL should always be followed by resetting the DLL using an LM command.

The DLL is automatically disabled when entering SELF REFRESH operation and is automatically re-enabled and reset upon exit of SELF REFRESH operation.

Any time the DLL is enabled (and subsequently reset), 200 clock cycles must occur before a READ command can be issued, to allow time for the internal clock to synchronize with the external clock. Failing to wait for synchronization to occur may result in a violation of the ^{t}AC or ^{t}DQSCK parameters.

OUTPUT DRIVE STRENGTH

The output drive strength is defined by bit E1, as shown in Figure 7. The normal drive strength for all outputs are specified to be SSTL_18. Programming bit E1 = 0 selects normal (full strength) drive strength for all outputs. Selecting a reduced drive strength option (E1 = 1) will reduce all outputs to approximately 60 percent of the SSTL_18 drive strength. This option is intended for the support of lighter load and/or point-to-point environments.

DQS# ENABLE/DISABLE

The DQS# ball is enabled by bit E10. When E10 = 0, DQS# is the complement of the differential data strobe pair DQS/DQS#. When disabled (E10 = 1), DQS is used in a single ended mode and the DQS# ball is disabled. When disabled, DQS# should be left floating. This function is also used to enable/disable RDQS#. If RDQS is enabled (E11 = 1) and DQS# is enabled (E10 = 0), then both DQS# and RDQS# will be enabled.

OUTPUT ENABLE/DISABLE

The OUTPUT ENABLE function is defined by bit E12, as shown in Figure 7. When enabled (E12 = 0), all outputs (DQs, DQS, DQS#, RDQS, RDQS#) function normally. When disabled (E12 = 1), all DDR2 SDRAM outputs (DQs, DQS, DQS#, RDQS, RDQS#) are disabled, thus removing output buffer current. The output disable feature is intended to be used during I_{CC} characterization of read current.

ON-DIE TERMINATION (ODT)

ODT effective resistance, R_{TT} (EFF), is defined by bits E2 and E6 of the EMR, as shown in Figure 7. The ODT feature is designed to improve signal integrity of the memory channel by allowing the DDR2 SDRAM controller to independently turn on/off ODT for any or all devices. R_{TT} effective resistance values of 50Ω ,75Ω, and 150Ω are selectable and apply to each DQ, DQS/DQS#, RDQS/RDQS#, UDQS/UDQS#, LDQS/LDQS#, DM, and UDM/LDM signals. Bits (E6, E2) determine what ODT resistance is enabled by turning on/off “sw1,” “sw2,” or “sw3.” The ODT effective resistance value is elected by enabling switch “sw1,” which enables all R1 values that are 150Ω each, enabling an effective resistance of 75Ω (R_{TT2}(EFF) = R2/2). Similarly, if “sw2” is enabled, all R2 values that are 300Ω each, enable an effective ODT resistance of 150Ω (R_{TT2}(EFF) = R2/2). Switch “sw3” enables R1 values of 100Ω enabling effective resistance of 50Ω Reserved states should not be used, as unknown operation or incompatibility with future versions may result.

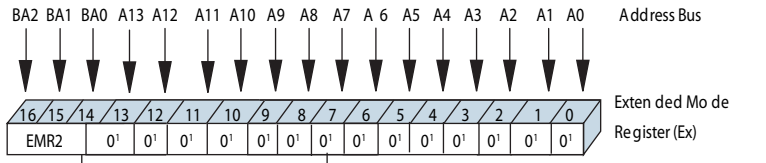
The ODT control ball is used to determine when R_{TT}(EFF) is turned on and off, assuming ODT has been enabled via bits E2 and E6 of the EMR. The ODT feature and ODT input ball are only used during active, active power-down (both fast-exit and slow-exit modes), and precharge power-down modes of operation. ODT must be turned off prior to entering self refresh. During power-up and initialization of the DDR2 SDRAM, ODT should be disabled until issuing the EMR command to enable the ODT feature, at which point the ODT ball will determine the R_{TT}(EFF) value. Any time the EMR enables the ODT function, ODT may not be driven HIGH until eight clocks after the EMR has been enabled. See “ODT Timing” section for ODT timing diagrams.

POSTED CAS ADDITIVE LATENCY (AL)

Posted CAS additive latency (AL) is supported to make the command and data bus efficient for sustainable bandwidths in DDR2 SDRAM. Bits E3–E5 define the value of AL, as shown in Figure 7. Bits E3–E5 allow the user to program the DDR2 SDRAM with an inverse AL of 0, 1, 2, 3, or 4 clocks. Reserved states should not be used as unknown operation or incompatibility with future versions may result.

In this operation, the DDR2 SDRAM allows a READ or WRITE command to be issued prior to ^{t}RCD (MIN) with the requirement that AL ≤ ^{t}RCD (MIN). A typical application using this feature would set AL = ^{t}RCD (MIN) - 1x ^{t}CK. The READ or WRITE command is held for the time of the AL before it is issued internally to the DDR2 SDRAM device. RL is controlled by the sum of AL and CL; RL = AL+CL. Write latency (WL) is equal to RL minus one clock; WL = AL + CL - 1 x ^{t}CK.

FIGURE 8 – EXTENDED MODE REGISTER 2 (EMR2) DEFINITION

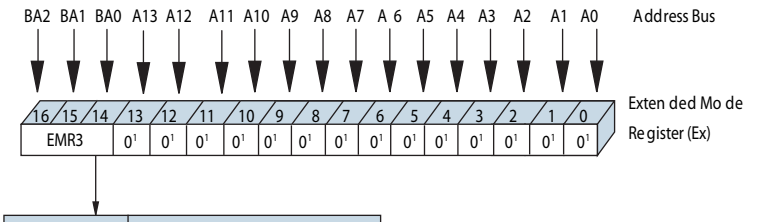


M1 6	M15	M14	Mode Register Definition
0	0	0	Mode register (MR)
0	0	1	Extended mode register (EMR)
0	1	0	Extended mode register (EMR2)
0	1	1	Extended mode register (EMR3)

E7	High Temperature Self Refresh rate enable
0	Commercial temperature default
1	In dustrial temperature option; use if T $_{C}$ exceeds 85° C

Note: 1. E13 (A13)-E0(A0) are reserved for future use and must be programmed to "0." A13 is not used in this device.

FIGURE 9 – EXTENDED MODE REGISTER 3 (EMR3) DEFINITION



M1 6	M15	M14	Mode Register Definition
0	0	0	Mode register (MR)
0	0	1	Extended mode register (EMR)
0	1	0	Extended mode register (EMR2)
0	1	1	Extended mode register (EMR3)

Note: 1. E13 (A13)-E0 (A0) are reserved for future use and must be programmed to "0." A13 is not used in this device.

EXTENDED MODE REGISTER 2

The extended mode register 2 (EMR2) controls functions beyond those controlled by the mode register. Currently all bits in EMR2 are reserved, as shown in Figure 8. The EMR2 is programmed via the LM command and will retain the stored information until it is programmed again or the device loses power. Reprogramming the EMR will not alter the contents of the memory array, provided it is performed correctly.

Bit E7 (A7) must be programmed as"1" to provide a faster refresh rate on devices if the T_{CASE} exceeds 85°C

EMR2 must be loaded when all banks are idle and no bursts are in progress, and the controller must wait the specified time ^{t}MRD before initiating any subsequent operation. Violating either of these requirements could result in unspecified operation.

EXTENDED MODE REGISTER 3

The extended mode register 3 (EMR3) controls functions beyond those controlled by the mode register. Currently, all bits in EMR3 are reserved, as shown in Figure 9. The EMR3 is programmed via the LM command and will retain the stored information until it is programmed again or the device loses power. Reprogramming the EMR will not alter the contents of the memory array, provided it is performed correctly.

EMR3 must be loaded when all banks are idle and no bursts are in progress, and the controller must wait the specified time ^{t}MRD before initiating any subsequent operation. Violating either of these requirements could result in unspecified operation.

COMMAND TRUTH TABLES

The following tables provide a quick reference of DDR2 SDRAM available commands, including CKE power-down modes, and bank-to-bank commands.

TABLE 3 – TRUTH TABLE - DDR2 COMMANDS

Notes 1, 5, and 6 apply to all

Function	CKE		CS#	RAS#	CAS#	WE#	BA2 BA1 BA0	A12 A11	A10	A9-A0	Notes
	Previous Cycle	Current Cycle									
LOAD MODE	H	H	L	L	L	L	BA	OP Code			2
REFRESH	H	H	L	L	L	H	X	X	X	X	
SELF-REFRESH Entry	H	L	L	L	L	H	X	X	X	X	
SELF-REFRESH Exit	L	H	H	X	X	X	X	X	X	X	7
			L	H	H	H					
Single bank precharge	H	H	L	L	H	L	X	X	L	X	2
All banks PRECHARGE	H	H	L	L	H	L	X	X	H	X	
Bank activate	H	H	L	L	H	L	BA	Row Address			
WRITE	H	H	L	L	H	L	BA	Column Address	L	Column Address	2, 3
WRITE with auto precharge	H	H	L	H	L	L	BA	Column Address	H	Column Address	2, 3
READ	H	H	L	H	L	H	BA	Column Address	L	Column Address	2, 3
READ with auto precharge	H	H	L	H	L	H	BA	Column Address	H	Column Address	2, 3
NO OPERATION	H	X	L	H	H	H	X	X	X	X	
Device DESELECT	H	X	H	X	X	X	X	X	X	X	
POWER-DOWN entry	H	L	H	X	X	X	X	X	X	X	4
			L	H	H	H					
POWER-DOWN exit	L	H	H	X	X	X	X	X	X	X	4
			L	H	H	H					

Note: 1. All DDR2 SDRAM commands are defined by states of CS#, RAS#, CAS#, WE#, and CKE at the rising edge of the clock.

2. Bank addresses (BA) BA0–BA2 determine which bank is to be operated upon. BA during a LM command selects which mode register is programmed.

3. 3. Burst reads or writes at BL = 4 cannot be terminated or interrupted.

4. The power-down mode does not perform any REFRESH operations. The duration of power-down is therefore limited by the refresh requirements outlined in the AC parametric section.

5. The state of ODT does not affect the states described in this table. The ODT function is not available during self refresh. See “On-Die Termination (ODT)” for details.

6. “X” means “H or L” (but a defined logic level).

7. Self refresh exit is asynchronous.

DESELECT

The DESELECT function (CS# HIGH) prevents new commands from being executed by the DDR2 SDRAM. The DDR2 SDRAM is effectively deselected. Operations already in progress are not affected.

NO OPERATION (NOP)

The NO OPERATION (NOP) command is used to instruct the selected DDR2 SDRAM to perform a NOP (CS# is LOW; RAS#, CAS#, and WE are HIGH). This prevents unwanted commands from being registered during idle or wait states. Operations already in progress are not affected.

LOAD MODE (LM)

The mode registers are loaded via inputs BA2–BA0, and A12–A0. BA2–BA0 determine which mode register will be programmed. See "Mode Register (MR)". The LM command can only be issued when all banks are idle, and a subsequent execute able command cannot be issued until ^{t}MRD is met.

BANK/ROW ACTIVATION

ACTIVE COMMAND

The ACTIVE command is used to open (or activate) a row in a particular bank for a subsequent access. The value on the BA2–BA0 inputs selects the bank, and the address provided on inputs A12–A0 selects the row. This row remains active (or open) for accesses until a PRECHARGE command is issued to that bank. A PRECHARGE command must be issued before opening a different row in the same bank.

ACTIVE OPERATION

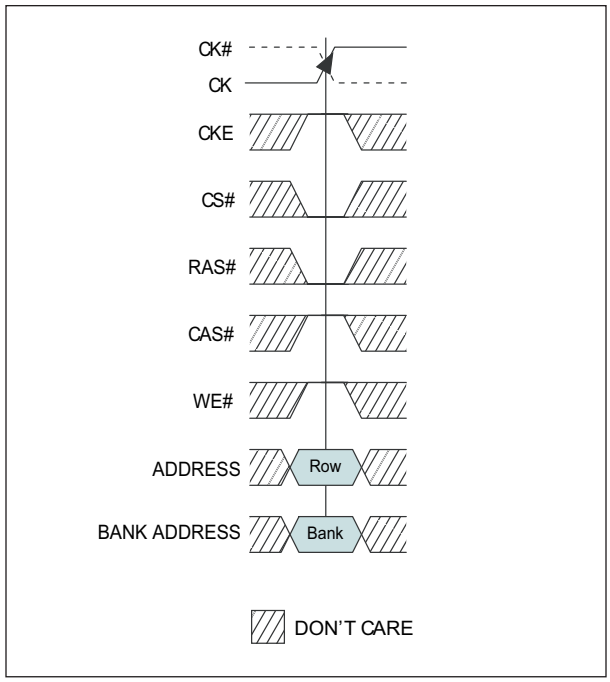
Before any READ or WRITE commands can be issued to a bank within the DDR2 SDRAM, a row in that bank must be opened (activated), even when additive latency is used. This is accomplished via the ACTIVE command, which selects both the bank and the row to be activated.

After a row is opened with an ACTIVE command, a READ or WRITE command may be issued to that row, subject to the ^{t}RCD specification. ^{t}RCD (MIN) should be divided by the clock period and rounded up to the next whole number to determine the earliest clock edge after the ACTIVE command on which a READ or WRITE command can be entered. The same procedure is used to convert other specification limits from time units to clock cycles. For example, a ^{t}RCD (MIN) specification of 20ns with a 266 MHz clock (^{t}CK = 3.75ns) results in 5.3 clocks, rounded up to 6.

A subsequent ACTIVE command to a different row in the same bank can only be issued after the previous active row has been closed (precharged). The minimum time interval between successive ACTIVE commands to the same bank is defined by ^{t}RC

A subsequent ACTIVE command to another bank can be issued while the first bank is being accessed, which results in a reduction of total row-access overhead. The minimum time interval between successive ACTIVE commands to different banks is defined by ^{t}RRD

FIGURE 10 – ACTIVE COMMAND



READ COMMAND

The READ command is used to initiate a burst read access to an active row. The value on the BA2–BA0 inputs selects the bank, and the address provided on inputs A0–i (where i = A9) selects the starting column location. The value on input A10 determines whether or not auto precharge is used. If auto precharge is selected, the row being accessed will be precharged at the end of the READ burst; if auto precharge is not selected, the row will remain open for subsequent accesses.

READ OPERATION

READ bursts are initiated with a READ command. The starting column and bank addresses are provided with the READ command and auto precharge is either enabled or disabled for that burst access. If auto precharge is enabled, the row being accessed is automatically precharged at the completion of the burst. If auto precharge is disabled, the row will be left open after the completion of the burst.

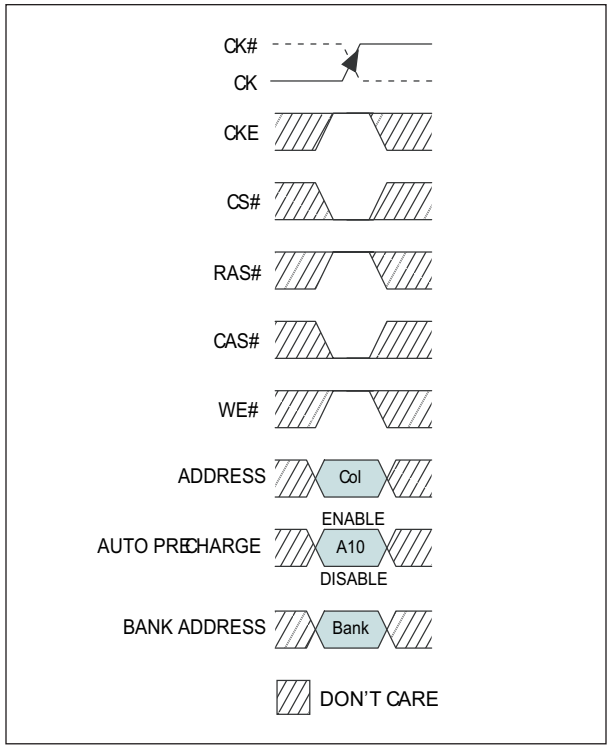
During READ bursts, the valid data-out element from the starting column address will be available READ latency (RL) clocks later. RL is defined as the sum of AL and CL; RL = AL + CL. The value for AL and CL are programmable via the MR and EMR commands, respectively. Each subsequent data-out element will be valid nominally at the next positive or negative clock edge (i.e., at the next crossing of CK and CK#).

DQS/DQS# is driven by the DDR2 SDRAM along with output data. The initial LOW state on DQS and HIGH state on DQS# is known as the read preamble (^{t}RPRE). The LOW state on DQS and HIGH state on DQS# coincident with the last data-out element is known as the read postamble (^{t}RPST).

Upon completion of a burst, assuming no other commands have been initiated, the DQ will go High-Z.

Data from any READ burst may be concatenated with data from a subsequent READ command to provide a continuous flow of data. The first data element from the new burst follows the last element of a completed burst. The new READ command should be issued *x* cycles after the first READ command, where *x* equals BL / 2 cycles.

FIGURE 11 – READ COMMAND



WRITE COMMAND

The WRITE command is used to initiate a burst write access to an active row. The value on the BA2–BA0 inputs selects the bank, and the address provided on inputs A0–9 selects the starting column location. The value on input A10 determines whether or not auto precharge is used. If auto precharge is selected, the row being accessed will be precharged at the end of the WRITE burst; if auto precharge is not selected, the row will remain open for subsequent accesses.

Input data appearing on the DQ is written to the memory array subject to the DM input logic level appearing coincident with the data. If a given DM signal is registered LOW, the corresponding data will be written to memory; if the DM signal is registered HIGH, the corresponding data inputs will be ignored, and a WRITE will not be executed to that byte/column location.

WRITE OPERATION

WRITE bursts are initiated with a WRITE command, as shown in Figure 12. DDR2 SDRAM uses WL equal to RL minus one clock cycle [WL = RL - 1CK = AL + (CL - 1CK)]. The starting column and bank addresses are provided with the WRITE command, and auto precharge is either enabled or disabled for that access. If auto precharge is enabled, the row being accessed is precharged at the completion of the burst.

During WRITE bursts, the first valid data-in element will be registered on the first rising edge of DQS following the WRITE command, and subsequent data elements will be registered on successive edges of DQS. The LOW state on DQS between the WRITE command and the first rising edge is known as the write preamble; the LOW state on DQS following the last data-in element is known as the write postamble.

The time between the WRITE command and the first rising DQS edge is WL ± ^{t}DQSS. Subsequent DQS positive rising edges are timed, relative to the associated clock edge, as ± ^{t}DQSS. ^{t}DQSS is specified with a relatively wide range (25 percent of one clock cycle). All of the WRITE diagrams show the nominal case, and where the two extreme cases (^{t}DQSS [MIN] and ^{t}DQSS [MAX]) might not be intuitive, they have also been included. Upon completion of a burst, assuming no other commands have been initiated, the DQ will remain High-Z and any additional input data will be ignored.

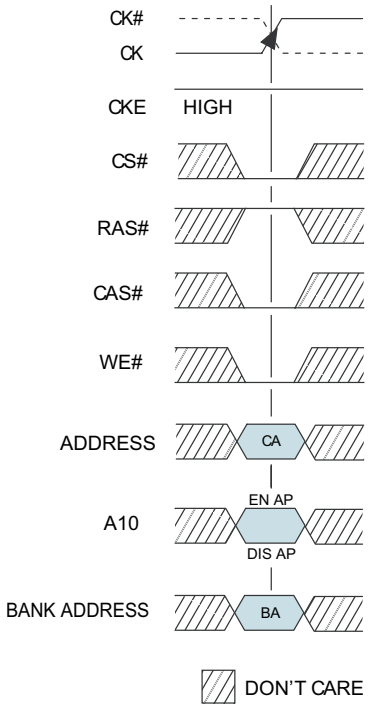
Data for any WRITE burst may be concatenated with a subsequent WRITE command to provide continuous flow of input data. The first data element from the new burst is applied after the last element of a completed burst. The new WRITE command should be issued *x* cycles after the first WRITE command, where *x* equals BL/2.

DDR2 SDRAM supports concurrent auto precharge options, as shown in Table 4.

DDR2 SDRAM does not allow interrupting or truncating any WRITE burst using BL = 4 operation. Once the BL = 4 WRITE command is registered, it must be allowed to complete the entire WRITE burst cycle. However, a WRITE (with auto precharge disabled) using BL = 8 operation might be interrupted and truncated ONLY by another WRITE burst as long as the interruption occurs on a 4-bit boundary, due to the 4*n* prefetch architecture of DDR2 SDRAM. WRITE burst BL = 8 operations may not to be interrupted or truncated with any command except another WRITE command.

Data for any WRITE burst may be followed by a subsequent READ command. The number of clock cycles required to meet ^{t}WTR is either 2 or ^{t}WTR/^{t}CK, whichever is greater. Data for any WRITE burst may be followed by a subsequent PRECHARGE command. ^{t}WT starts at the end of the data burst, regardless of the data mask condition.

FIGURE 12 – WRITE COMMAND



Note: CA = column address; BA = bank address; EN AP = enable auto precharge; and DIS AP = disable auto precharge.

TABLE 4 – WRITE USING CONCURRENT AUTO PRECHARGE

From Command (Bank *n*)	To Command (Bank *m*)	Minimum Delay (With Concurrent Auto Precharge)	Units
WRITE with Auto Precharge	READ OR READ w/AP	(CL-1) + (BL/2) + ^{t}WTR	^{t}CK
	WRITE or WRITE w/AP	(BL/2)	^{t}CK
	PRECHARGE or ACTIVE	1	^{t}CK

PRECHARGE COMMAND

The PRECHARGE command, illustrated in Figure 13, is used to deactivate the open row in a particular bank or the open row in all banks. The bank(s) will be available for a subsequent row activation a specified time (^{t}RP) after the PRECHARGE command is issued, except in the case of concurrent auto precharge, where a READ or WRITE command to a different bank is allowed as long as it does not interrupt the data transfer in the current bank and does not violate any other timing parameters. Once a bank has been precharged, it is in the idle state and must be activated prior to any READ or WRITE commands being issued to that bank. A PRECHARGE command is allowed if there is no open row in that bank (idle state) or if the previously open row is already in the process of precharging. However, the precharge period will be determined by the last PRECHARGE command issued to the bank.

PRECHARGE OPERATION

Input A10 determines whether one or all banks are to be precharged, and in the case where only one bank is to be precharged, inputs BA2–BA0 select the bank. Otherwise BA2–BA0 are treated as “Don’t Care.”

When all banks are to be precharged, inputs BA2–BA0 are treated as “Don’t Care.” Once a bank has been precharged, it is in the idle state and must be activated prior to any READ or WRITE commands being issued to that bank. ^{t}RPA timing applies when the PRECHARGE (ALL) command is issued, regardless of the number of banks already open or closed. If a single-bank PRECHARGE command is issued, ^{t}RP timing applies. ^{t}RPA (MIN) applies to all 8-bank DDR2 devices.

SELF REFRESH COMMAND

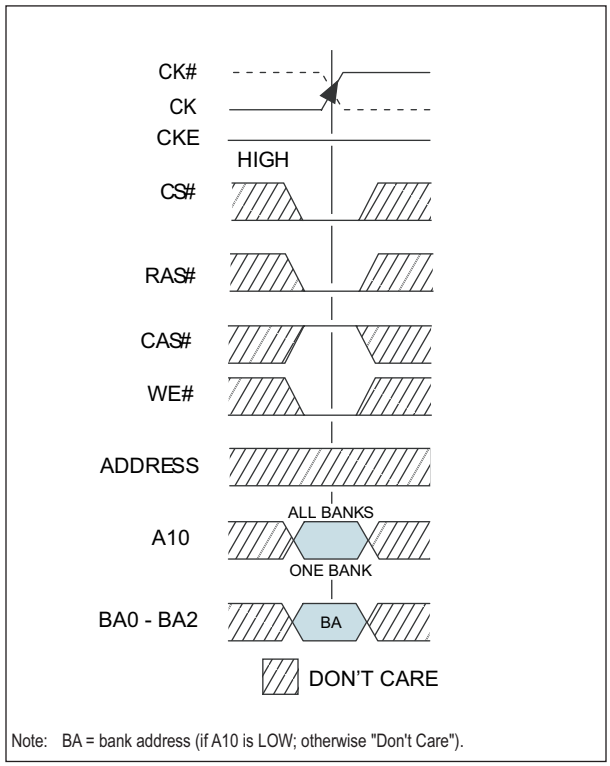
The SELF REFRESH command can be used to retain data in the DDR2 SDRAM, even if the rest of the system is powered down. When in the self refresh mode, the DDR2 SDRAM retains data without external clocking. All power supply inputs (including V_{REF}) must be maintained at valid levels upon entry/exit and during SELF REFRESH operation.

The SELF REFRESH command is initiated like a REFRESH command except CKE is LOW. The DLL is automatically disabled upon entering self refresh and is automatically enabled upon exiting self refresh (200 clock cycles must then occur before a READ command can be issued). The differential clock should remain stable and meet ^{t}CKE specifications at least 1 x ^{t}CK after entering self refresh mode. All command and address input signals except CKE are “Don’t Care” during self refresh.

The procedure for exiting self refresh requires a sequence of commands. First, the differential clock must be stable and meet ^{t}CK specifications at least 1 x ^{t}CK prior to CKE going back HIGH. Once CKE is HIGH (^{t}CLE(MIN) has been satisfied with four clock registrations), the DDR2 SDRAM must have NOP or DESELECT commands issued for ^{t}XSNR because time is required for the completion of any internal refresh in progress. A simple algorithm for meeting both refresh and DLL requirements is to apply NOP or DESELECT commands for 200 clock cycles before applying any other command.

Note: Self refresh not available at military temperature..

FIGURE 13 – PRECHARGE COMMAND



Note: BA = bank address (if A10 is LOW; otherwise "Don't Care").

DC OPERATING CONDITIONS

All voltages referenced to V_{SS}

Parameter	Symbol	Min	Typical	Max	Unit	Notes
Supply voltage	V_{CC}	1 .7	1 .8	1 .9	V	1
I/O Supply voltage	V_{CCQ}	1 .7	1 .8	1 .9	V	4
I/O Reference voltage	V_{REF}	0.49 x V_{CCQ}	0.50 x V_{CCQ}	0.51 x V_{CCQ}	V	2
I/O Termination voltage	V_{TT}	V_{REF}-0.04	V_{REF}	V_{REF} + 0.04	V	3

Notes:

1. V_{CC} V_{CCQ} must track each other. V_{CCQ} must be less than or equal to V_{CC}.
2. V_{REF} is expected to equal V_{CCQ}/2 of the transmitting device and to track variations in the DC level of the same. Peak-to-peak noise on V_{REF} may not exceed ±1 percent of the DC value. Peak-to-peak AC noise on V_{REF} may not exceed ±2 percent of V_{REF}. This measurement is to be taken at the nearest V_{REF} bypass capacitor.
3. V_{TT} is not applied directly to the device. V_{TT} is a system supply for signal termination resistors, is expected to be set equal to V_{REF} and must track variations in the DC level of V_{REF}.
4. V_{CCQ} tracks with V_{CC} track with V_{CC}.

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter		MIN	MAX	U nit
V_{CC}	Voltage on V_{CC} pin relative to V_{SS}		-1.0	2.3	V
V_{CCQ}	Voltage on V_{CCQ} pin relative to V_{SS}		-0.5	2.3	V
V_{IN}, V_{OUT}	Voltage on any pin relative to V_{SS}		-0.5	2.3	V
T_{STG}	Storage temperature		-55	125	°C
I_L	Input leakage current; Any input 0V<V_{IN}<V_{CC}; V_{REF} input 0V<V_{IN}<0.95V; Other pins not under test = 0V	Command/Address, RAS#, CAS#, WE#, CS#, CKE	-25	25	µA
		CK, CK#	-10	10	µA
		DM	-5	5	µA
I_{OZ}	Output leakage current; 0V<V_{OUT}<V_{CCQ}; DQs and ODT are disable	DQ, DQS, DQS#	-5	5	µA
I_{VREF}	V_{REF} leakage current; V_{REF} = Valid V_{REF} level		-10	10	µA

INPUT/OUTPUT CAPACITANCE

T_A = 25°C, f = 1MHz, V_{CC} = V_{CCQ} = 1.8V

Parameter	Symbol	Max	Unit
Input capacitance (A0 - A12, BA0 - BA2 ,CS#, RAS#,CAS#,WE#, CKE, ODT)	C_{IN1}	TBD	pF
Input capacitance CK, CK#	C_{IN2}	TBD	pF
Input capacitance DM, DQS, DQS#	C_{IN3}	TBD	pF
Input capacitance DQ0 - 71	C_{OUT}	TBD	pF

INPUT DC LOGIC LEVEL

All voltages referenced to V_{SS}

Parameter	Symbol	Min	Max	Unit
Input High (Logic 1) Voltage	V_{IH}(DC)	V_{REF} + 0.1 25	V_{CCQ} + 0.300	V
Input Low (Logic 0) Voltage	V_{IL}(DC)	-0.300	V_{REF} - 0.125	V

INPUT AC LOGIC LEVEL

All voltages referenced to V_{SS}

Parameter	Symbol	Min	Max	Unit
AC Input High (Logic 1) Voltage DDR2-400 & DDR2-533	V_{IH}(AC)	V_{REF} + 0.250	—	V
AC Input High (Logic 1) Voltage DDR2-667	V_{IH}(AC)	V_{REF} + 0.200	—	V
AC Input Low (Logic 0) Voltage DDR2-400 & DDR2-533	V_{IL}(AC)	—	V_{REF} - 0.250	V
AC Input Low (Logic 0) Voltage DDR2-667	V_{IL}(AC)	—	V_{REF} - 0.200	V

DDR2 I_{CC} SPECIFICATIONS AND CONDITIONS

VCC = 1.8V ±0.1V; -55°C ≤ T_A ≤ 125°C

Symbol	Proposed Conditions		533 CL4	400 CL3	Units
I_{CC0}	Operating one bank active-precharge current; $t_{CK} = t_{CK}(I_{CC})$, $t_{RC} = t_{RC}(I_{CC})$, $t_{RAS} = t_{RAS}min(I_{CC})$; CKE is HIGH, CS# is HIGH between valid commands; Address bus inputs are SWITCHING; Data bus inputs are SWITCHING		675	550	mA
I_{CC1}	Operating one bank active-read-precharge current; I_{OUT} = 0mA; BL = 4, CL = CL(I_{CC}), AL = 0; $t_{CK} = t_{CK}(I_{CC})$, $t_{RC} = t_{RC}(I_{CC})$, $t_{RAS} = t_{RAS}min(I_{CC})$, $t_{RCD} = t_{RCD}(I_{CC})$; CKE is HIGH, CS# is HIGH between valid commands; Address bus inputs are SWITCHING; Data pattern is same as I_{DAD6W}		650	600	mA
I_{CC2P}	Precharge power-down current; All banks idle; $t_{CK} = t_{CK}(I_{CC})$; CKE is LOW; Other control and address bus inputs are STABLE; Data bus inputs are FLOATING		35	35	mA
I_{CC2Q}	Precharge quiet standby current; All banks idle; $t_{CK} = t_{CK}(I_{CC})$; CKE is HIGH, CS# is HIGH; Other control and address bus inputs are STABLE; Data bus inputs are FLOATING		325	225	mA
I_{CC2N}	Precharge standby current; All banks idle; $t_{CK} = t_{CK}(I_{CC})$; CKE is HIGH, CS# is HIGH; Other control and address bus inputs are SWITCHING; Data bus inputs are SWITCHING		350	250	mA
I_{CC3P}	Active power-down current; All banks open; $t_{CK} = t_{CK}(I_{CC})$; CKE is LOW; Other control and address bus inputs are STABLE; Data bus inputs are FLOATING	Fast PDN Exit MRS(12) = 0	200	150	mA
		Slow PDN Exit MRS(12) = 1	50	50	mA
I_{CC3N}	Active standby current; All banks open; $t_{CK} = t_{CK}(I_{CC})$, $t_{RAS} = t_{RASMAX}(I_{CC})$, $t_{RP} = t_{RP}(I_{CC})$; CKE is HIGH, CS# is HIGH between valid commands; Other control and address bus inputs are SWITCHING; Data bus inputs are SWITCHING		375	300	mA
I_{CC4W}	Operating burst write current; All banks open, Continuous burst writes; BL = 4, CL = CL(I_{CC}), AL = 0; $t_{CK} = t_{CK}(I_{CC})$, $t_{RAS} = t_{RASMAX}(I_{CC})$, $t_{RP} = t_{RP}(I_{CC})$; CKE is HIGH, CS# is HIGH between valid commands; Address bus inputs are SWITCHING; Data bus inputs are SWITCHING		1,000	900	mA
I_{CC4R}	Operating burst read current; All banks open, Continuous burst reads, I_{OUT} = 0mA; BL = 4, CL = CL(I_{CC}), AL = 0; $t_{CK} = t_{CK}(I_{CC})$, $t_{RAS} = t_{RASMAX}(I_{CC})$, $t_{RP} = t_{RP}(I_{CC})$; CKE is HIGH, CS# is HIGH between valid commands; Address bus inputs are SWITCHING; Data pattern is same as I_{DAD6W}		1,300	1,250	mA
I_{CC5}	Burst auto refresh current; $t_{CK} = t_{CK}(I_{CC})$; Refresh command at every $t_{RFC}(I_{CC})$ interval; CKE is HIGH, CS# is HIGH between valid commands; Other control and address bus inputs are SWITCHING; Data bus inputs are SWITCHING		1,350	1,250	mA
I_{CC6}	Self refresh current; CK and CK# at 0V; CKE 0.2V; Other control and address bus inputs are FLOATING; Data bus inputs are FLOATING	Normal	35	35	mA
I_{CC7}	Operating bank interleave read current; All bank interleaving reads, I_{OUT} = 0mA; BL = 4, CL = CL(I_{CC}), AL = $t_{RC}D(I_{CC})$-1*$t_{CK}(I_{CC})$; $t_{CK} = t_{CK}(I_{CC})$, $t_{RC} = t_{RC}(I_{CC})$, $t_{RRD} = t_{RRD}(I_{CC})$, t_{RCD} = 1*$t_{CK}(I_{CC})$; CKE is HIGH, CS# is HIGH between valid commands; Address bus inputs are STABLE during DESELECTs; Data pattern is same as I_{DAD6R}; Refer to the following page for detailed timing conditions		1,750	1,650	mA

AC TIMING PARAMETERS

-55°C ≤ T_A < +125°C; V_{CCQ} = + 1.8V ± 0.1V, V_{CC} = +1.8V ± 0.1V

Parameter			Symbol	533Mbs CL4		400Mbs CL3		Unit
				Min	Max	Min	Max	
Clock	Clock cycle time	CL=4	$^tCK(4)$	3,750	8,000	5,000	8,000	ps
		CL=3	$^tCK(3)$	5,000	8,000	5,000	8,000	ps
	CK high-level width		^tCH	0.48	0.52	0.48	0.52	t_{CK}
	CK low-level width		^tCL	0.48	0.52	0.48	0.52	t_{CK}
	Half clock period		^tHP	MIN (t_{CH}, t_{CL})		MIN (t_{CH}, t_{CL})		ps
Clock (absolute)	Absolute ^tCK		$^tCK_{abs}$	$^tCK_{AVG}$ (MIN)+ $^tJIT_{PER}$ (MIN)	$^tCK_{AVG}$ (MAX)+ $^tJIT_{PER}$ (MAX)	$^tCK_{AVG}$ (MIN)+ $^tJIT_{PER}$ (MIN)	$^tCK_{AVG}$ (MAX)+ $^tJIT_{PER}$ (MAX)	ps
	Absolute CK high-level width		$^tCH_{abs}$	$^tCK_{AVG}$ (MIN)* $^tCH_{AVG}$ (MIN)+ $^tJIT_{DTY}$ (MIN)	$^tCK_{AVG}$ (MAX)* $^tCH_{AVG}$ (MAX)+ $^tJIT_{DTY}$ (MAX)	$^tCK_{AVG}$ (MIN)* $^tCH_{AVG}$ (MIN)+ $^tJIT_{DTY}$ (MIN)	$^tCK_{AVG}$ (MAX)* $^tCH_{AVG}$ (MAX)+ $^tJIT_{DTY}$ (MAX)	ps
	Absolute CK low-level width		$^tCL_{abs}$	$^tCK_{AVG}$ (MIN)* $^tCL_{AVG}$ (MIN)+ $^tJIT_{DTY}$ (MIN)	$^tCK_{AVG}$ (MAX)* $^tCL_{AVG}$ (MAX)+ $^tJIT_{DTY}$ (MAX)	$^tCK_{AVG}$ (MIN)* $^tCL_{AVG}$ (MIN)+ $^tJIT_{DTY}$ (MIN)	$^tCK_{AVG}$ (MAX)* $^tCL_{AVG}$ (MAX)+ $^tJIT_{DTY}$ (MAX)	ps
Clock Jitter	Clock jitter - period		$^tJIT_{PER}$	-125	125	-125	125	ps
	Clock jitter - half period		$^tJIT_{DUTY}$	-125	125	-125	125	ps
	Clock jitter - cycle to cycle		$^tJIT_{CC}$	250		250		ps
	Cumulative jitter error, 2 cycles		$^tERR_{2per}$	-175	175	-175	175	ps
	Cumulative jitter error, 3 cycles		$^tERR_{3per}$	-225	225	-225	225	ps
	Cumulative jitter error, 4 cycles		$^tERR_{4per}$	-250	250	-250	250	ps
	Cumulative jitter error, 5 cycles		$^tERR_{5per}$	-250	250	-250	250	ps
	Cumulative jitter error, 6-10 cycles		$^tERR_{6\text{-}10per}$	-350	350	-350	350	ps
	Cumulative jitter error, 11-50 cycles		$^tERR_{11\text{-}50per}$	-450	450	-450	450	ps

AC TIMING PARAMETERS (continued)

-55°C ≤ T_A < +125°C; V_{CCQ} = + 1.8V ± 0.1V, V_{CC} = +1.8V ± 0.1V

Parameter		Symbol	533Mbs CL4		400Mbs CL3		Unit
			Min	Max	Min	Max	
Data	DQ hold skew factor	^tQHS	-	400	-	450	ps
	DQ output access time from CK/CK#	^tAC	-500	+500	-600	+600	ps
	Data-out high impedance window from CK/CK#	^tHZ		$t_{AC(MAX)}$		$t_{AC(MAX)}$	ps
	DQS Low-Z window from CK/CK#	$^tLZ_1$	$t_{AC(MN)}$	$t_{AC(MAX)}$	$t_{AC(MN)}$	$t_{AC(MAX)}$	ps
	DQ Low-Z window from CK/CK#	$^tLZ_2$	$2*t_{AC(MN)}$	$t_{AC(MAX)}$	$2*t_{AC(MN)}$	$t_{AC(MAX)}$	ps
	DQ and DM input setup time relative to DQS	^tDS_a	350		400		ps
		^tDH_a	350		400		ps
		^tDS_b	100		150		ps
		^tDH_b	225		275		ps
	DQ and DM input pulse width (for each input)	^tDIPW	0.35		0.35		ps
	Data hold skew factor	^tQHS		400		450	ps
	DQ-DQS hold, DQS to first DQ to go nonvalid, per access	^tQH	$t_{HP} - t_{QHS}$		$t_{HP} - t_{QHS}$		ps
	Data valid output window (DVW)	^tDVW	$t_{QH} - t_{DQSQ}$		$t_{QH} - t_{DQSQ}$		ns
Data Strobe	DQS input high pulse width	^tDQSH	0.35		0.35		t_{CK}
	DQS input low pulse width	^tDQSL	0.35		0.35		t_{CK}
	DQS output access time fromCK/CK#	^tDQSCK	-450	+450	-500	+500	ps
	DQS falling edge to CK rising - setup time	^tDSS	0.2		0.2		t_{CK}
	DQS falling edge from CK rising - hold time	^tDSH	0.2		0.2		t_{CK}
	DQS-DQ skew, DOS to last DQ valid, per group, per access	^tDQSQ		300		350	ps
	DQS read preamble	^tRPRE	0.9	1.1	0.9	1.1	t_{CK}
	DQS read postamble	^tRPST	0.4	0.6	0.4	0.6	t_{CK}
	DQS write preamble setup time	^tWPRES	0		0		ps
	DQS write preamble	^tWPRE	0.25		0.25		t_{CK}
	DQS write postamble	^tWPST	0.4	0.6	0.4	0.6	t_{CK}
	Positive DQS latching edge to associated clock edge	^tDQSS	-0.25	0.25	-0.25	0.25	t_{CK}
	Write command to first DQS latching transition		WL-T_{DQSS}	WL+T_{DQSS}	WL-T_{DQSS}	WL+T_{DQSS}	t_{CK}

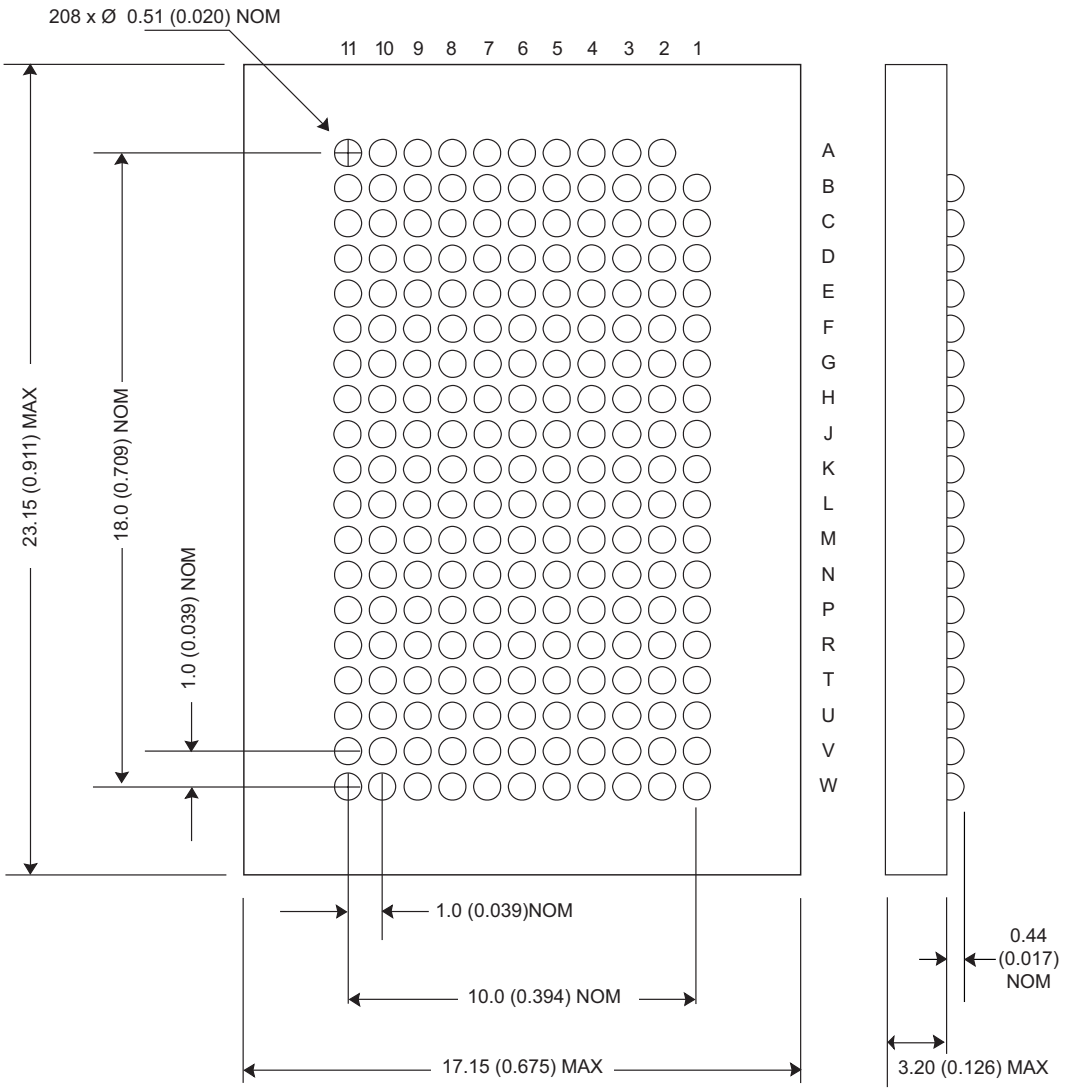
AC TIMING PARAMETERS (continued)

-55°C ≤ T_A < +125°C; V_{CCQ} = + 1.8V ± 0.1V, V_{CC} = +1.8V ± 0.1V

Parameter		Symbol	533Mbs CL4		400Mbs CL3		Unit
			Min	Max	Min	Max	
Command and Address	Address and control input pulse width for each input	^tIPW	0.6		0.6		t_{CK}
	Address and control input setup time	^tIS_a	500		600		ps
		^tIS_b	250		350		ps
	Address and control input hold time	^tIH_a	500		600		ps
		^tIH_b	375		475		ps
	CAS# to CAS# command delay	^tCCD	2		2		ps
	ACTIVE to ACTIVE (same bank) command	^tRC	55		55		ns
	ACTIVE bank a to ACTIVE bank b command	^tRRD	10		10		ns
	ACTIVE to READ or WRITE delay	^tRCD	15		15		ns
	Four Bank Activate period	^tFAW	50		50		ns
	ACTIVE to PRECHARGE command	^tRAS	40	70,000	40	70,000	ns
	Internal READ to precharge command delay	^tRTP	7.5		7.5		ns
	Write recovery time	^tWR	15		15		ns
	Auto precharge write recovery + precharge time	^tDAL	$t_{WR} + t_{RP}$		$t_{WR} + t_{RP}$		ns
	Internal WRITE to READ command delay	^tWTR	7.5		10		ns
	PRECHARGE command period	^tRP	15		15		ns
	PRECHARGE ALL command period	^tRPA	$t_{RP} + t_{CK}$		$t_{RP} + t_{CK}$		ns
	LOAD MODE command cycle time	^tMRD	2		2		t_{CK}
Self Refresh	CKE low to CK, CK# uncertainty	^tDELAY	$t_{IS} + t_{IH} + t_{CK}$		$t_{IS} + t_{IH} + t_{CK}$		ns
	REFRESH to Active or Refresh to Refresh command interval	^tRFC	127.5	70,000	127.5	70,000	ns
	Average periodic refresh interval (commercial)	^tREFI		7.8		7.8	µs
	Average periodic refresh interval (industrial)	$^tREFI_{IT}$		3.9		3.9	µs
	Exit self refresh to non-READ command	^tXSNR	$t_{RPC(MIN)} + 10$		$t_{RFC(MIN)} + 10$		ns
	Exit self refresh to READ	^tXSRD	200		200		t_{CK}
	Exit self refresh timing reference	^tISXR	t_{IS}		t_{IS}		ps
ODT	ODT tum-on delay	^tAOND	2	2	2	2	t_{CK}
	ODT turn-on	^tACN	$t_{AC(MIN)}$	$t_{AC(MAX)} + 1000$	$t_{AC(MIN)}$	$t_{AC(MAX)} + 1000$	ps
	ODT turn-off delay	^tAOFD	2.5	2.5	2.5	2.5	t_{CK}
	ODT tum-off	^tAOF	$t_{AC(MIN)}$	$t_{AC(MAX)} + 600$	$t_{AC(MIN)}$	$t_{AC(MAX)} + 600$	ps
	ODT tum-on (power-down mode)	^tAONPD	$t_{AC(MIN)} + 2000$	$2 \times t_{CK} + t_{AC(MAX)} + 1000$	$t_{AC(MIN)} + 2000$	$2 \times t_{CK} + t_{AC(MAX)} + 1000$	ps
	ODT turn-off (power-down mode)	^tAOFPD	$t_{AC(MIN)} + 2000$	$2 \times t_{CK} + t_{AC(MAX)} + 1000$	$t_{AC(MIN)} + 2000$	$2 \times t_{CK} + t_{AC(MAX)} + 1000$	ps
	ODT to power-down entry latency	^tANPD	3		3		t_{CK}
	ODT power-down exit latency	^tAXPD	8		8		t_{CK}
	ODT enable from MRS command	^tMOD	12		12		ns
Power-Down	Exit active power-down to READ command, MR[bit12=0]	^tXARD	2		2		t_{CK}
	Exit active power-down to READ command, MR[bit12=1]	^tXARDS	6-AL		6-AL		t_{CK}
	Exit precharge power-down to any non-READ command	^tXP	2		2		t_{CK}
	CKE minimum high/low time	^tCKE	3		3		t_{CK}

PACKAGE DIMENSION: 208 PLASTIC BALL GRID ARRAY (PBGA)

BOTTOM VIEW



All linear dimensions are millimeters and parenthetically in inches

ORDERING INFORMATION

W 3H 64M 72 E - XXX SB X

WHITE ELECTRONIC DESIGNS CORP.

DDR2 SDRAM

CONFIGURATION, 64M x 72

1.8V Power Supply

DATA RATE (Mbs)
400 = 400Mbs
533 = 533Mbs
667 = 667Mbs
Blank = No data rate specified for ES product(1)

PACKAGE:
ES = Non Qualified Product (1)
SB = 208 Plastic Ball Grid Array (PBGA)

DEVICE GRADE:
M = Military -55°C to +125°C
I = Industrial -40°C to +85°C
C = Commercial 0°C to +70°C
Blank = No temperature specified for ES product(1)

Note 1: W3H64M72E-ESSB is the only available product until completion of qualification.

Document Title

64M x 72 DDR2 SDRAM 208 PBGA Multi-Chip Package

Revision History

Rev #	History	Release Date	Status
Rev 0	Initial Release	December 2005	Advanced
Rev 1	Changes (All pages) 1.1 Add additional technical data	March 2006	Advanced