

3875081 G E SOLID STATE
Silicon Controlled Rectifiers

01E 17666 D

F-2.5-15

File Number 96

2N681-2N692

25-A Silicon Controlled Rectifiers

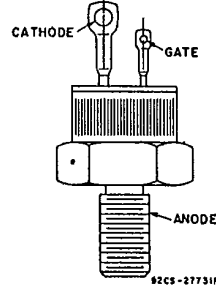
For Power-Control and Power-Switching Application

Features:

- High di/dt capability
- Low on-state voltage at high current levels
- Low thermal resistance

The RCA2N681-2N692 are all-diffused silicon controlled rectifiers (reverse-blocking triode thyristors) designed for switching ac and dc currents. These devices can switch from the off-state to the on-state when both the anode and gate voltages are positive. Negative anode voltages make these devices revert to the blocking state. These SCR's employ a hermetic JEDEC TO-208AA package.

TERMINAL DESIGNATIONS



JEDEC TO-208AA

MAXIMUM RATINGS, Absolute-Maximum Values:

	2N681	2N682	2N683	2N684	2N685	2N686	2N687	2N688	2N689	2N690	2N691	2N692	
V_{RSM} Δ	35	75	150	225	300	350	400	500	600	720	840	960	
V_{RSM} Δ	25	50	100	150	200	250	300	400	500	600	700	800	
V_{RSM} Δ	25	50	100	150	200	250	300	400	500	600	700	800	
I_{TSM} ($\theta = 180^\circ$); $T_C = 65^\circ C$												25	A
I_{TSM} ($\theta = 180^\circ$); $T_C = 65^\circ C$												16	A
I_{SM} : For one full cycle of applied principal voltage												150	A
60Hz Δ												140	A
50Hz Δ												140	A
For more than one full cycle of applied principal voltage												See Fig. 2	
di/dt:													
$V_D = V_{RSM}$, $I_{GT} = 200$ mA, $t_r = 0.5 \mu s$												200	A/ μs
$I^2 t$ (at T_C shown for I_{TSM}):													
$t = 10$ ms												100	A ² s
$t = 1$ ms												46	A ² s
P_{GM}												5	W
P_{GM}												0.5	W
I_{GM}												2	A
V_{GM}												10	V
V_{GM}												5	V
T_{STG}												-65 to 150	$^\circ C$
T_C												-65 to 125	$^\circ C$
T_r													
During soldering for 10 s maximum (terminal and case)												225	$^\circ C$
r_l : Recommended												35	in-lb
.....												0.4	kgf-m
Maximum (DO NOT EXCEED)												50	in-lb
.....												0.57	kgf-m

*In accordance with JEDEC registration data
 Δ These values do not apply if there is a positive gate signal. Gate must be open or negatively biased
 Δ At $I_{TSM} = 25$ A and $T_C = 65^\circ C$
 Δ Any product gate current and gate voltage which results in gate power less than the maximum is permitted.
 Δ For temperature measurement reference point, see Dimensional Outline.

2N681-2N692

ELECTRICAL CHARACTERISTICS, At Maximum Ratings Unless Otherwise Specified and at Indicated Case Temperature (T_c)

CHARACTERISTIC	LIMITS			UNITS
	2N681-2N690			
	MIN.	TYP.	MAX.	
* I_{DRM} or I_{RRM} $V_D = V_{DRM}$ or $V_R = V_{RRM}$, $T_C = 125^\circ\text{C}$: 2N681, 2N682, 2N683, 2N684 2N685 2N686 2N687 2N688 2N689 2N690 2N691 2N692	—	—	6.5 6 5.5 5 4 3 2.5 2	mA
* v_T : $i_T = 50\text{ A (peak)}$, $T_C = 25^\circ\text{C}$	—	—	2	V
v_T (AV): $I_T = I_T$ (RMS) = $T_C = 65^\circ\text{C}$	—	—	0.86	V
i_{HO} : $T_C = 125^\circ\text{C}$	—	15	—	mA
I_{GT} : $T_C = 125^\circ$ $V_D = 12\text{ V (dc)}$, $R_L = 50\Omega$, $T_C = -65^\circ\text{C}$	—	—	25 80*	mA
V_{GT} : $V_D = 12\text{ V (dc)}$, $R_L = 50\Omega$, $T_C = -65$ to 125°C $= 125^\circ$	—	—	3 —	V
$R_{\theta JC}$	—	—	2	$^\circ\text{C/W}$

*In accordance with JEDEC registration data.

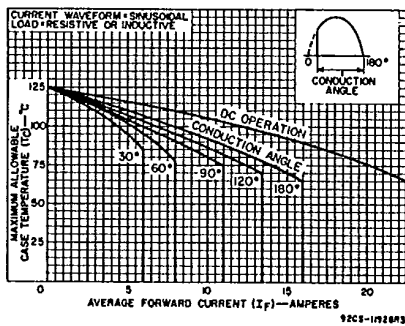


Fig. 1 — Maximum allowable case temperature vs. on-state current for 2N681-2N692.

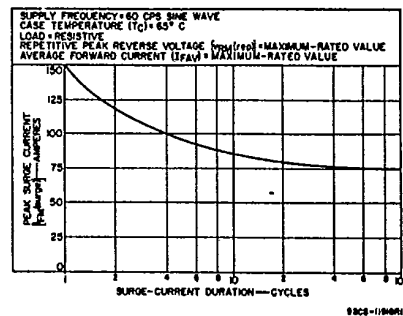


Fig. 2 — Peak surge on-state current vs. surge duration for 2N681-2N692.

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01E 17668 DT-25-15

2N681-2N692

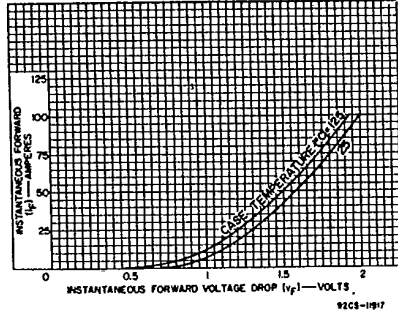


Fig. 3 — Typical on-state current vs. instantaneous on-state voltage for 2N681-2N692.

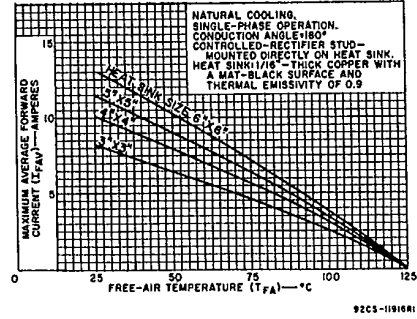


Fig. 4 — Average on-state forward current vs. ambient temperature for 2N681-2N692.