Voltage Detector IC Series

Low Voltage Free Delay Time Setting CMOS Voltage Detector IC Series

BU42□□G, BU42□□F, BU42□□FVE, BU43□□G, BU43□□F, BU43□□FVE series

No.09006EBT02

● Description

ROHM CMOS reset IC series with adjustable output delay is a high-accuracy low current consumption reset IC series with a built-in delay circuit. The lineup was established with two output types (Nch open drain and CMOS output) and detection voltages range from 0.9V to 4.8V in increments of 0.1V, so that the series may be selected according to the application at hand.

● Features

1) Detection voltage from 0.9V to 4.8V in 0.1V increments
2) Highly accurate detection voltage: ±1.0%
3) Ultra-low current consumption
4) Nch open drain output (BU42□□G/F/FVE)and CMOS output (BU43□□G/F/FVE)
5) Small surface package SSOP5: BU42□□G, BU43□□G
   SOP4: BU42□□F, BU43□□F
   VSOF5: BU42□□FVE, BU43□□FVE

● Applications

All electronics devices that use microcontrollers and logic circuits.

● Selection Guide

Part Number : BU4 □ □ □ □

① ② ③

No.	Specifications	Description
①	Output Circuit Format	2:Open Drain Output, 3:CMOS Output
②	Detection Voltage	Example V_{DET}: Represented as 0.1V steps in the range from 0.9V to 4.8V (Displayed as 0.9 in the case of 0.9V)
③	Package	G:SSOP5(SMP5C2)/ F:SOP4/ FVE:VSOF5(EMP5)

● Lineup

Making	Detection voltage	Part Number	Making	Detection voltage	Part Number	Making	Detection voltage	Part Number	Making	Detection voltage	Part Number
ZR	4.8V	BU4248	YV	2.8V	BU4228	1H	4.8V	BU4348	0M	2.8V	BU4328
ZQ	4.7V	BU4247	YU	2.7V	BU4227	1G	4.7V	BU4347	0L	2.7V	BU4327
ZP	4.6V	BU4246	YT	2.6V	BU4226	1F	4.6V	BU4346	0K	2.6V	BU4326
ZN	4.5V	BU4245	YS	2.5V	BU4225	1E	4.5V	BU4345	0J	2.5V	BU4325
ZM	4.4V	BU4244	YR	2.4V	BU4224	1D	4.4V	BU4344	0H	2.4V	BU4324
ZL	4.3V	BU4243	YQ	2.3V	BU4223	1C	4.3V	BU4343	0G	2.3V	BU4323
ZK	4.2V	BU4242	YP	2.2V	BU4222	1B	4.2V	BU4342	0F	2.2V	BU4322
ZJ	4.1V	BU4241	YN	2.1V	BU4221	1A	4.1V	BU4341	0E	2.1V	BU4321
ZH	4.0V	BU4240	YM	2.0V	BU4220	0Z	4.0V	BU4340	0D	2.0V	BU4320
ZG	3.9V	BU4239	YL	1.9V	BU4219	0Y	3.9V	BU4339	0C	1.9V	BU4319
ZF	3.8V	BU4238	YK	1.8V	BU4218	0X	3.8V	BU4338	0B	1.8V	BU4318
ZE	3.7V	BU4237	YJ	1.7V	BU4217	0W	3.7V	BU4337	0A	1.7V	BU4317
ZD	3.6V	BU4236	YH	1.6V	BU4216	0V	3.6V	BU4336	ZZ	1.6V	BU4316
ZC	3.5V	BU4235	YG	1.5V	BU4215	0U	3.5V	BU4335	ZY	1.5V	BU4315
ZB	3.4V	BU4234	YF	1.4V	BU4214	0T	3.4V	BU4334	ZX	1.4V	BU4314
ZA	3.3V	BU4233	YE	1.3V	BU4213	0S	3.3V	BU4333	ZW	1.3V	BU4313
YZ	3.2V	BU4232	YD	1.2V	BU4212	0R	3.2V	BU4332	ZV	1.2V	BU4312
YY	3.1V	BU4231	YC	1.1V	BU4211	0Q	3.1V	BU4331	ZU	1.1V	BU4311
YX	3.0V	BU4230	YB	1.0V	BU4210	0P	3.0V	BU4330	ZT	1.0V	BU4310
YW	2.9V	BU4229	YA	0.9V	BU4209	0N	2.9V	BU4329	ZS	0.9V	BU4309

● **Absolute maximum ratings (Ta=25°C)**

Parameter		Symbol	Limits	Unit
Power Supply Voltage		VDD-GND	-0.3 ~ +7	V
Output Voltage	Nch Open Drain Output	VOUT	GND-0.3 ~ +7	V
	CMOS Output		GND-0.3 ~ VDD+0.3	
Power Dissipation	SSOP5 *1*4	Pd	540	mW
	SOP4 *2*4		400	
	VSOF5 *3*4		210	
Operating Temperature		Topr	-40 ~ +125	°C
Ambient Storage Temperature		Tstg	-55 ~ +125	°C

*1 When used at temperatures higher than Ta=25°C, the power is reduced by 5.4mW per 1°C above 25°C.
*2 When used at temperatures higher than Ta=25°C, the power is reduced by 4.0mW per 1°C above 25°C.
*3 When used at temperatures higher than Ta=25°C, the power is reduced by 2.1mW per 1°C above 25°C.
*4 When a ROHM standard circuit board (70mm×70mm×1.6mm, glass epoxy board)is mounted.

● **Electrical characteristics (Unless Otherwise Specified Ta=-40 to 105°C)**

Parameter	Symbol	Condition		Limit Min.	Limit Typ.	Limit Max.	Unit
Detection Voltage	V_{DET}	V_{DD}=H→L, Ta=25°C, R_L=470kΩ		V_{DET}(T) ×0.99	V_{DET}(T)	V_{DET}(T) ×1.01	V
Circuit Current when ON	I_{DD1}	V_{DD}=V_{DET}-0.2V	V_{DET} =0.9-1.3V	-	0.15	0.88	μA
			V_{DET} =1.4-2.1V	-	0.20	1.05	
			V_{DET} =2.2-2.7V	-	0.25	1.23	
			V_{DET} =2.8-3.3V	-	0.30	1.40	
			V_{DET} =3.4-4.2V	-	0.35	1.58	
			V_{DET} =4.3-4.8V	-	0.40	1.75	
Circuit Current when OFF	I_{DD2}	V_{DD}=V_{DET}+2.0V	V_{DET} =0.9-1.3V	-	0.30	1.40	μA
			V_{DET} =1.4-2.1V	-	0.35	1.58	
			V_{DET} =2.2-2.7V	-	0.40	1.75	
			V_{DET} =2.8-3.3V	-	0.45	1.93	
			V_{DET} =3.4-4.2V	-	0.50	2.10	
			V_{DET} =4.3-4.8V	-	0.55	2.28	
Operating Voltage Range	V_{OPL}	V_{OL}≤0.4V, Ta=25~125°C, R_L=470kΩ		0.70	-	-	V
		V_{OL}≤0.4V, Ta=-40~25°C, R_L=470kΩ		0.90	-	-	
'High' Output Current (Pch)	I_{OH}	V_{DS}=0.5V V_{DD}=6.0V VDET=4.0-4.8V		2.0	4.0	-	mA
'Low' Output Current (Nch)	I_{OL}	V_{DS}=0.05V V_{DD}=0.85V		20	100	-	μA
		V_{DS}=0.5V V_{DD}=1.5V V_{DET}=1.7-4.8V		1.0	3.3	-	mA
		V_{DS}=0.5V V_{DD}=2.4V V_{DET}=2.7-4.8V		3.6	6.5	-	
Leak Current when OFF	Ileak	V_{DD}=V_{DS}=7V Ta=-40~85°C		-	0	0.1	μA
		V_{DD}=V_{DS}=7V Ta=85~125°C		-	0	1	
'High' Output Current (Pch)	I_{OH}	V_{DS}=0.5V V_{DD}=4.8V V_{DET}=0.9-3.9V		1.7	3.4	-	mA
		V_{DS}=0.5V V_{DD}=6.0V V_{DET}=4.0-4.8V		2.0	4.0	-	
CT pin Threshold Voltage	V_{CTH}	V_{DD}=V_{DET}×1.1, V_{DET}=0.9-2.5V Ta=25°C R_L=470kΩ		V_{DD} ×0.35	V_{DD} ×0.45	V_{DD} ×0.55	V
		V_{DD}=V_{DET}×1.1, V_{DET}=2.6-4.8V Ta=25°C R_L=470kΩ		V_{DD} ×0.40	V_{DD} ×0.50	V_{DD} ×0.60	
Output Delay Resistance	R_{CT}	V_{DD}=V_{DET}×1.1 V_{CT}=0.5V Ta=25°C *1		9	10	11	MΩ
CT pin Output Current	I_{CT}	V_{CT}=0.1V V_{DD}=0.85V		5	40	-	μA
		V_{CT}=0.5V V_{DD}=1.5V V_{DET}=1.7-4.8V		200	400	-	
Detection Voltage Temperature coefficient	$V_{DET}/\Delta T$	Ta=-40°C ~125°C		-	±30	-	ppm/°C
Hysteresis Voltage	ΔV_{DET}	V_{DD}=L→H→L Ta=-40~125°C R_L=470kΩ	V_{DET}≤1.0V	V_{DET} ×0.03	V_{DET} ×0.05	V_{DET} ×0.08	V
			V_{DET}≤1.1V	V_{DET} ×0.03	V_{DET} ×0.05	V_{DET} ×0.07	

*1: Designed guarantee. (Outgoing inspection is not done all products.)
V_{DET}(T) : Standard Detection Voltage（0.9V to 4.8V, 0.1V step）
R_L: Pull-up resistor to be connected between V_{OUT} and power supply.

● Block Diagrams

BU42□□G/F/FVE

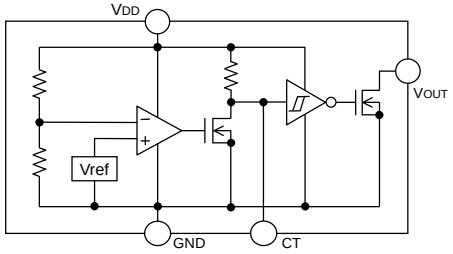


Fig.1

BU43□□G/F/FVE

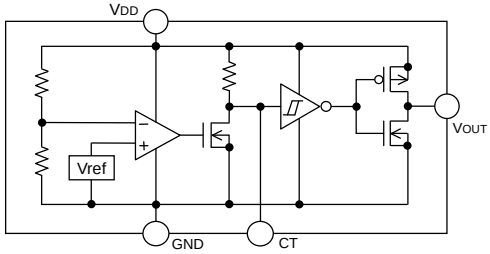
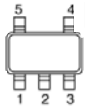


Fig.2

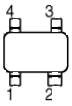
TOP VIEW



SSOP5

PIN No.	Symbol	Function
1	VOUT	Reset output
2	VDD	Power supply voltage
3	GND	GND
4	N.C.	Unconnected terminal
5	CT	Capacitor connection terminal for output delay time

TOP VIEW



SOP4

PIN No.	Symbol	Function
1	GND	GND
2	VDD	Power supply voltage
3	CT	Capacitor connection terminal for output delay time
4	VOUT	Reset output

TOP VIEW

VSOF5

PIN No.	Symbol	Function
1	VOUT	Reset output
2	SUB	Substrate*
3	CT	Capacitor connection terminal for output delay time
4	VDD	Power supply voltage
5	GND	GND

*Connect the substrate to VDD

● **Reference Data (Unless specified otherwise, Ta=25°C)**

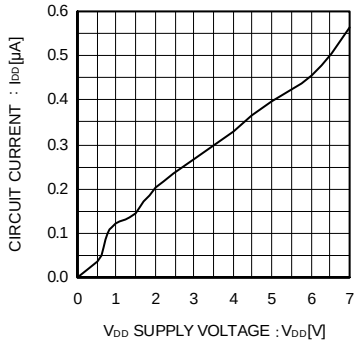


Fig.3 Circuit Current

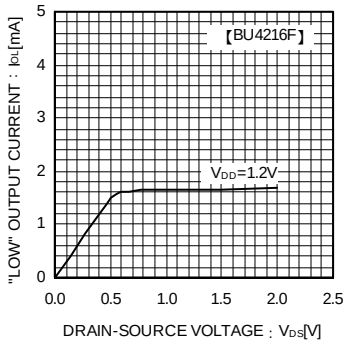


Fig.4 “LOW” Output Current

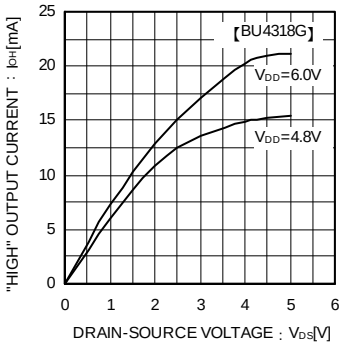


Fig.5 “High” Output Current

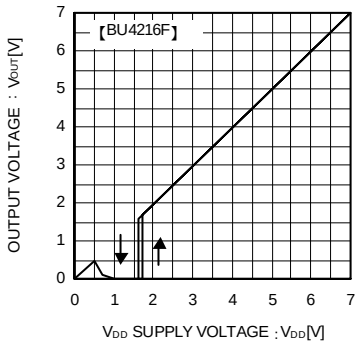


Fig.6 I/O Characteristics

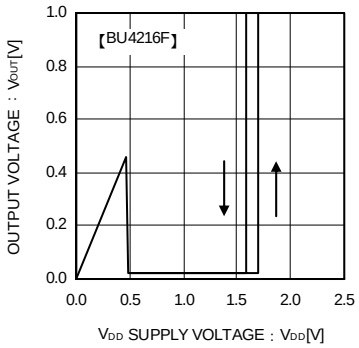


Fig.7 Operating Limit Voltage

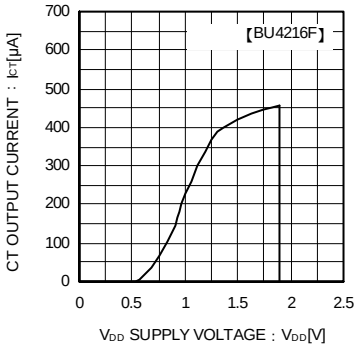


Fig.8 Ct Terminal Current

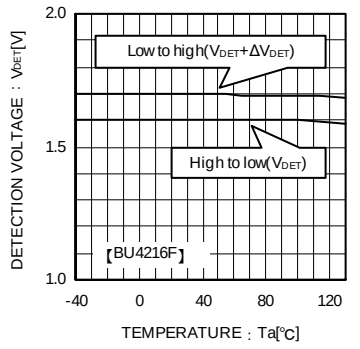


Fig.9 Detecting Voltage
Release Voltage

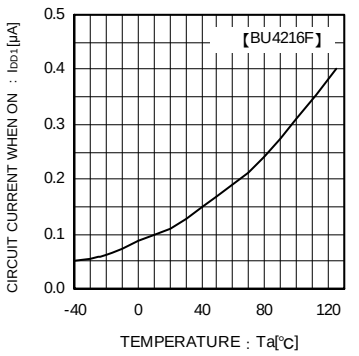


Fig.10 Circuit Current when ON

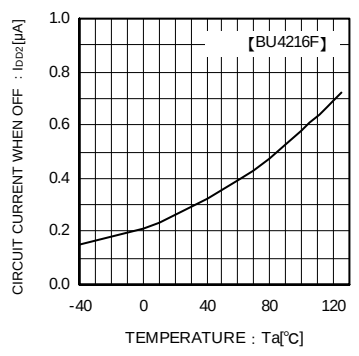


Fig.11 Circuit Current when OFF

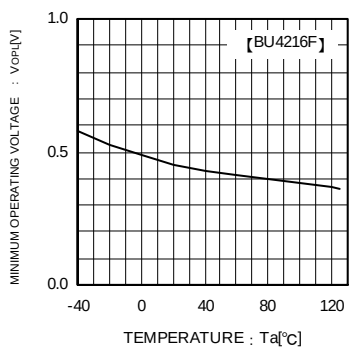


Fig.12 Operating Limit Voltage

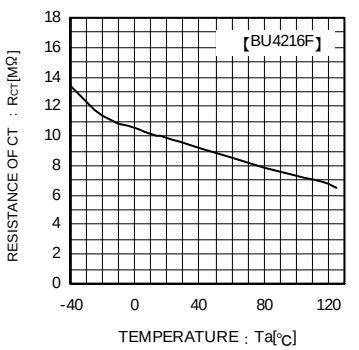


Fig.13 Ct Terminal Circuit Resistance

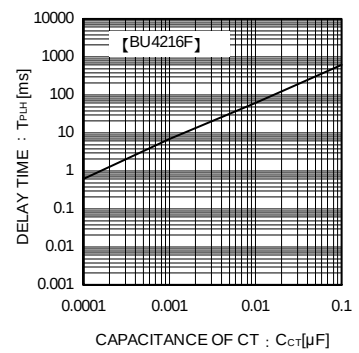


Fig.14 Delay Time (TPLH) and
CT Terminal External Capacitance

● **Setting of Detector Delay Time**

This detector IC can be set delay time at the rise of V_{DD} by the capacitor connected to CT terminal.

Delay time at the rise of V_{DD} T_{PLH}:Time until when Vout rise to 1/2 of V_{DD} after V_{DD} rise up and beyond the release voltage($V_{DET}+\Delta V_{DET}$)

$$T_{PLH}=-C_{CT}\times R_{CT}\times \ln\left(\frac{V_{DD}-V_{CTH}}{V_{DD}}\right)$$

C_{CT}: CT pin Externally Attached Capacitance
V_{CTH}: CT pin Threshold Voltage（P.2 V_{CTH} refer.）
R_{CT}: CT pin Internal Impedance（P.2 R_{CT} refer.）
Ln: Natural Logarithm

● **Reference Data of Falling Time (T_{PHL}) Output**

Examples of Falling Time (T_{PHL}) Output

Part Number	T_{PHL} [μs]
BU4245G	275.7
BU4345G	359.3

*This data is for reference only.

The figures will vary with the application, so please confirm actual operating conditions before use.

● **Explanation of Operation**

For both the open drain type(Fig.15)and the CMOS output type(Fig.16), the detection and release voltages are used as threshold voltages. When the voltage applied to the Vdd pins reaches the applicable threshold voltage, the Vout terminal voltage switches from either “High” to “Low” or from “Low” to “High”. BU42□□G/F/FVE and BU43□□G/F/FVE have delay time function which set T_{PLH} (Output “Low”→”High”) using an external capacitor (C_{CT}). Because the BU42□□G/F/FVE series uses an open drain output type, it is possible to connect a pull-up resistor to V_{DD} or another power supply [The output “High” voltage (V_{OUT}) in this case becomes V_{DD} or the voltage of the other power supply].

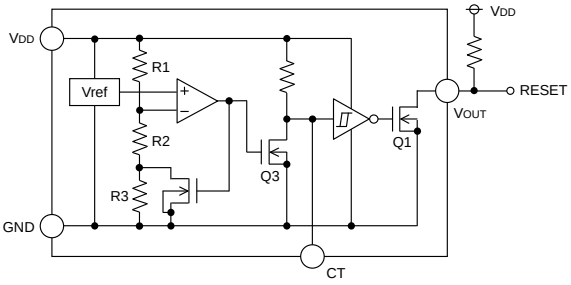


Fig.15 (BU42□□ type internal block diagram)

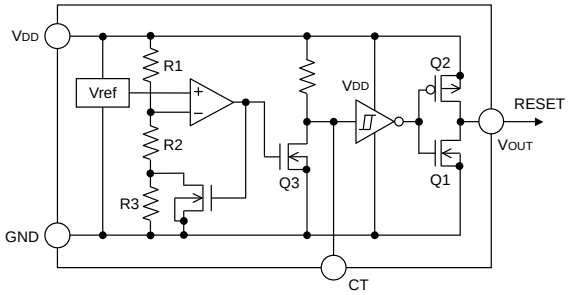


Fig.16 (BU43□□ type internal block diagram)

● **Timing Waveforms**

Example: the following shows the relationship between the input voltage V_{DD}, the CT Terminal Voltage V_{CT} and the output voltage V_{OUT} when the input power supply voltage V_{DD} is made to sweep up and sweep down (The circuits are those in Fig.15 and 16).

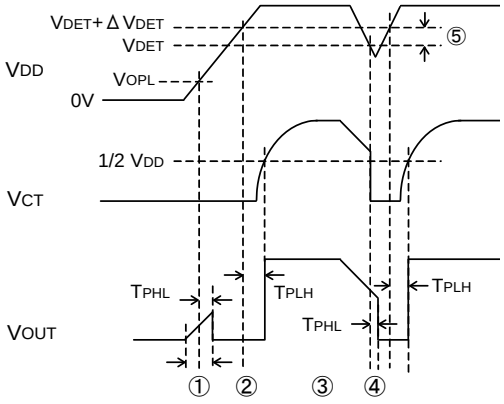


Fig.17

① When the power supply is turned on, the output is unsettled from after over the operating limit voltage (V_{OPL}) until T_{PHL}. There fore it is possible that the reset signal is not outputted when the rise time of VDD is faster than T_{PHL}.

② When V_{DD} is greater than V_{OPL} but less than the reset release voltage ($V_{DET}+\Delta V_{DET}$), the CT terminal (V_{CT}) and output (V_{OUT}) voltages will switch to L.

③ If V_{DD} exceeds the reset release voltage ($V_{DET}+V_{DET}$), then V_{OUT} switches from L to H (with a delay to the CT terminal).

④ If V_{DD} drops below the detection voltage (V_{DET}) when the power supply is powered down or when there is a power supply fluctuation, V_{OUT} switches to L (with a delay of T_{PHL}).

⑤ The potential difference between the detection voltage and the release voltage is known as the hysteresis width (V_{DET}). The system is designed such that the output does not flip-flop with power supply fluctuations within this hysteresis width, preventing malfunctions due to noise.

● **Circuit Applications**

1) Examples of a common power supply detection reset circuit

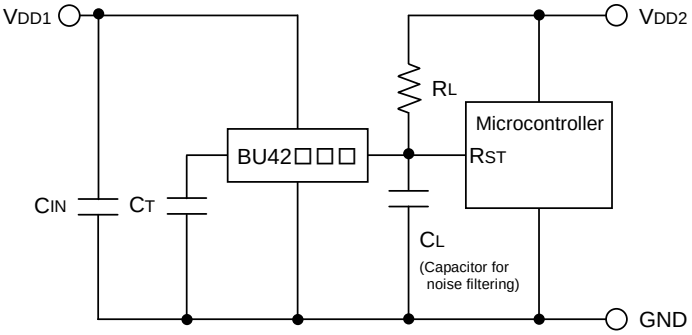


Fig.18 Open collector Output type

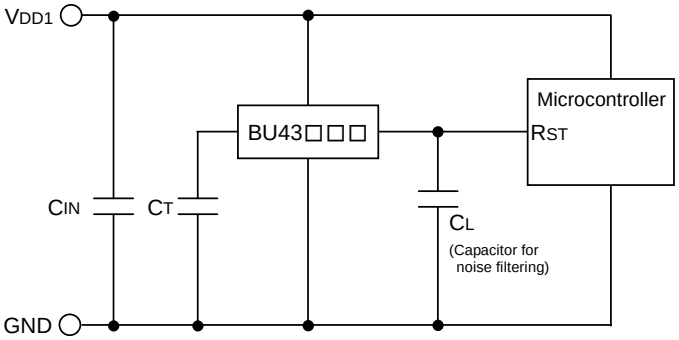


Fig.19 CMOS Output type

Application examples of BU42□□G/F/FVE series (Open Drain output type) and BU43□□G/F/FVE series (CMOS output type) are shown below.

CASE1:The power supply of the microcontroller (Vdd2) differs from the power supply of the reset detection (Vdd1).

Use the Open Drain Output Type (BU42□□G/FVE) attached a load resistance (RL) between the output and Vdd2. (As shown Fig.18)

CASE2:The power supply of the microcontroller (Vdd1) is same as the power supply of the reset detection (Vdd1).

Use CMOS output type (BU43□□G/FVE) or Open Drain Output Type (BU42□□G/FVE) attached a load resistance (RL) between the output and Vdd1. (As shown Fig.19)

When a capacitance CL for noise filtering is connected to the Vout pin (the reset signal input terminal of the microcontroller), please take into account the waveform of the rise and fall of the output voltage (Vout).

2) Examples of the power supply with resistor dividers

In applications where the power supply input terminal (VDD) of an IC with resistor dividers, it is possible that a through current will momentarily flow into the circuit when the output logic switches, resulting in malfunctions (such as output oscillatory state).

(Through-current is a current that momentarily flows from the power supply (VDD) to ground (GND) when the output level switches from “High” to “Low” or vice versa.)

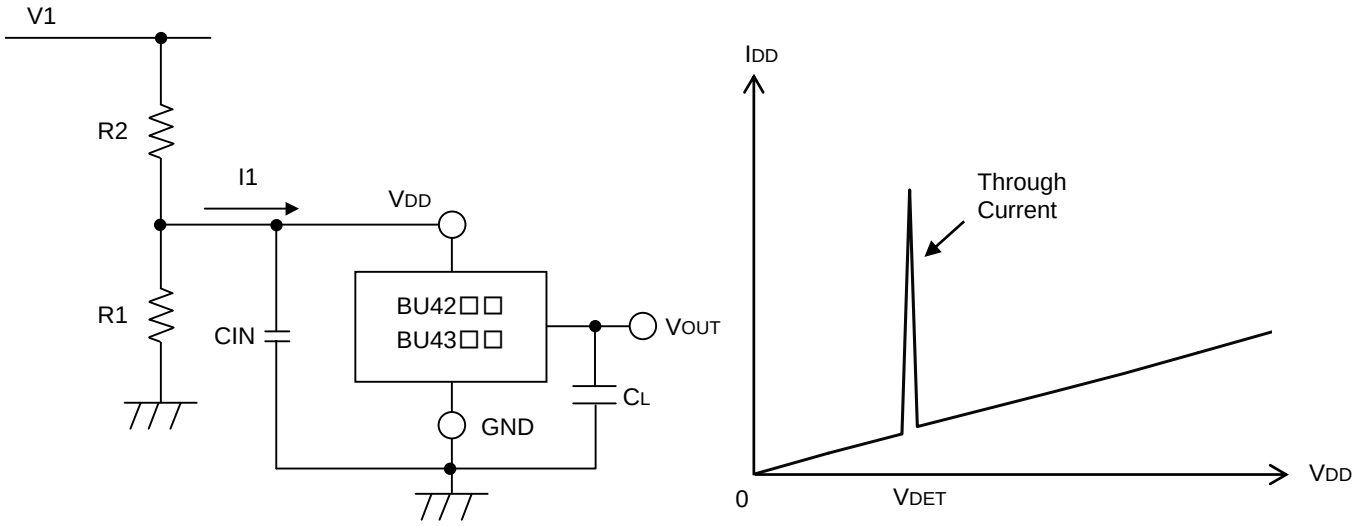


Fig.20

A voltage drop of [the through-current (I1)] × [input resistor (R2)] is caused by the through current, and the input voltage to descends, when the output switches from “Low” to “High”. When the input voltage decreases and falls below the detection voltage, the output voltage switches from “High” to “Low”. At this time, the through-current stops flowing through output “Low”, and the voltage drop is eliminated. As a result, the output switches from “Low” to “High”, which again causes the through current to flow and the voltage drop. This process is repeated, resulting in oscillation.

Consider the use of BU42□□ when the power supply input it with resistor dividers.

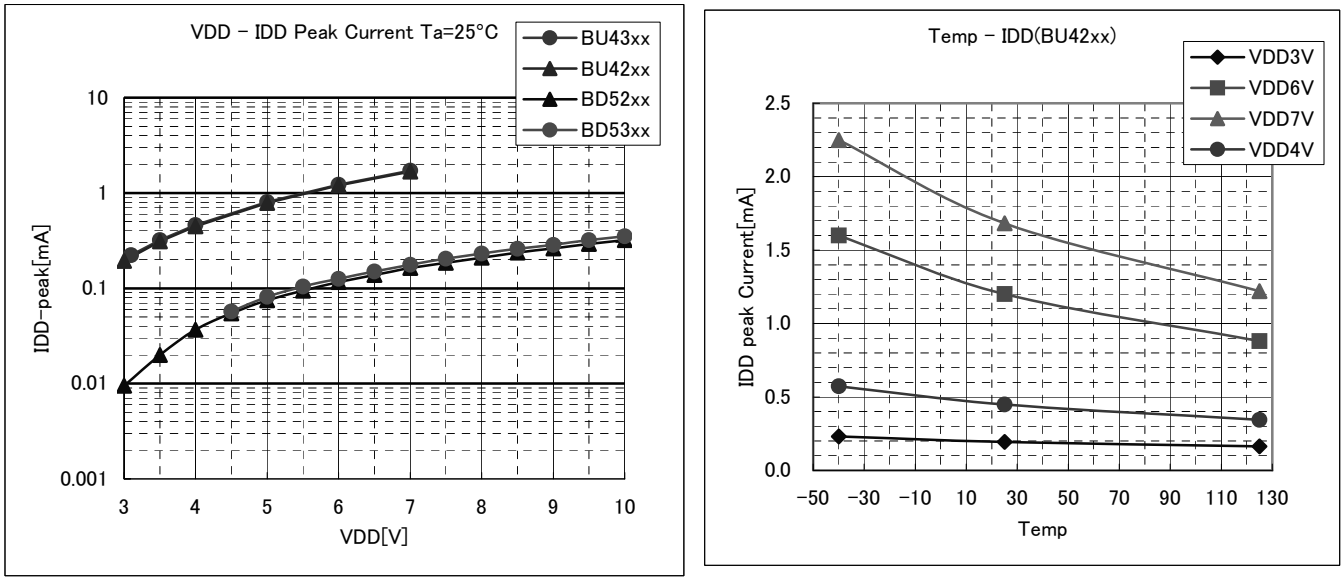


Fig.21 Current Consumption vs. Power Supply Voltage

*This data is for reference only.

The figures will vary with the application, so please confirm actual operating conditions before use.

● **Operation Notes**

1 . Absolute maximum range

Absolute Maximum Ratings are those values beyond which the life of a device may be destroyed. We cannot be defined the failure mode, such as short mode or open mode. Therefore a physical security countermeasure, like fuse, is to be given when a specific mode to be beyond absolute maximum ratings is considered.

2 . GND potential

GND terminal should be a lowest voltage potential every state.
Please make sure all pins that are over ground even if include transient feature.

3 . Electrical Characteristics

Be sure to check the electrical characteristics, that are one the tentative specification will be changed by temperature, supply voltage, and external circuit.

4 . Bypass Capacitor for Noise Rejection

Please put into the to reject noise between V_{DD} pin and GND with 1uF over and between V_{OUT} pin and GND with 1000pF.
If extremely big capacitor is used, transient response might be late. Please confirm sufficiently for the point.

5 . Short Circuit between Terminal and Soldering

Don't short-circuit between Output pin and V_{DD} pin, Output pin and GND pin, or V_{DD} pin and GND pin. When soldering the IC on circuit board please is unusually cautious about the orientation and the position of the IC. When the orientation is mistaken the IC may be destroyed.

6 . Electromagnetic Field

Mal-function may happen when the device is used in the strong electromagnetic field.

7 . The V_{DD} line inpedance might cause oscillation because of the detection current.

8 . A V_{DD} -GND capacitor (as close connection as possible) should be used in high V_{DD} line impedance condition.

9 . Lower than the mininum input voltage makes the V_{OUT} high impedance, and it must be V_{DD} in pull up (V_{DD}) condition.

10. Case of needless Delay time, recommended to insert more 470kΩ resister between V_{DD} and CT.

11. Recommended value of RL Resistar is over 50kΩ (VDET=1.5~4.8V),
over 100kΩ (VDET=0.9~1.4V).

12. This IC has extremely high impedance terminals. Small leak current due to the uncleanness of PCB surface might cause unexpected operations. Application values in these conditions should be selected carefully. If 10MΩ leakage is assumed between the CT terminal and the GND terminal, 1MΩ connection between the CT terminal and the V_{DD} terminal would be recommended. Also, if the leakage is assumed between the V_{OUT} terminal and the GND terminal, the pull up resistor should be less than 1/10 of the assumed leak resistance.
The value of R_{CT} depends on the external resistor that is connected to CT terminal, so please consider the delay time that is decided by $\tau \times RCT \times CCT$ changes.

13. Delay time (tPLH)

tPLH = τ × R_{CT} × C_{CT} (sec)

τ: time constant

R_{CT} : 10MΩ (typ.) (built-in resistor)

C_{CT} : capacitor connected C_T pin.

Recommended value of C_{CT} capacitor is over 100pF.

The reference value

$(\tau \times R_{CT}) \times 10^6$

V_{DET} = 0.9 to 2.5V

Ta = 25°C (min. = 5.1×10^6 typ.= 6.0×10^6 max = 6.9×10^6)

Ta = -25 to 125°C (min. = 3.3×10^6 typ. = 6.0×10^6 max = 8.7×10^6)

V_{DET} = 2.6 to 4.8V

Ta = 25°C (min. = 5.9×10^6 typ.= 6.9×10^6 max = 7.9×10^6)

Ta = -25 to 125°C (min. = 3.8×10^6 typ.= 6.9×10^6 max = 10.0×10^6)

14. External parameters

The recommended parameter range for C_T is 100pF~0.1μF. For R_L, the recommended range is 50kΩ~1MΩ. There are many factors (board layout, etc) that can affect characteristics. Please verify and confirm using practical applications.

15. CT pin discharge

Due to the capabilities of the CT pin discharge transistor, the CT pin may not completely discharge when a short input pulse is applied, and in this case the delay time may not be controlled. Please verify the actual operation.

16. Power on reset operation

Please note that the power on reset output varies with the Vcc rise up time. Please verify the actual operation.

17. Precautions for board inspection

Connecting low-impedance capacitors to run inspections with the board may produce stress on the IC.
Therefore, be certain to use proper discharge procedure before each process of the test operation.
To prevent electrostatic accumulation and discharge in the assembly process, thoroughly ground yourself and any equipment that could sustain ESD damage, and continue observing ESD-prevention procedures in all handing, transfer and storage operations. Before attempting to connect components to the test setup, make certain that the power supply is OFF. Likewise, be sure the power supply is OFF before removing any component connected to the test setup.

18. When the power supply, is turned on because of in certain cases, momentary Rash-current flow into the IC at the logic unsettled, the couple capacitance, GND pattern of width and leading line must be considered.

● **Part Number Selection**

B	U	4	2		0	9		G		T	R

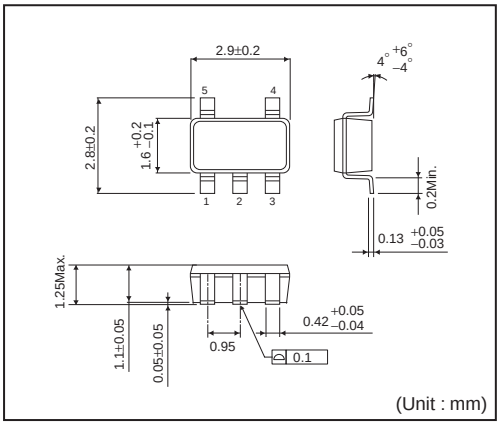
BU42: Adjustable Delay Time CMOS Reset IC Open Drain Type Output Type
BU43: Adjustable Delay Time CMOS Reset IC CMOS Output Type

Detection voltage
09 : 0.9V (0.1V step)
48 : 4.8V

Package
G: SSOP5
F: SOP4
FVE: VSOF5

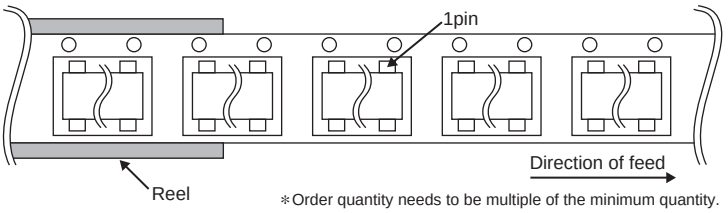
Taping Specifications
Embossed Taping

SSOP5



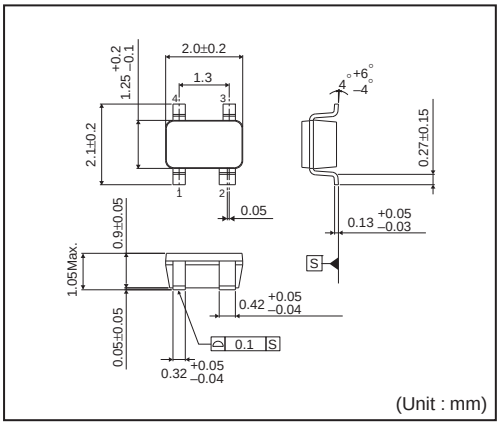
<Tape and Reel information>

Tape	Embossed carrier tape
Quantity	3000pcs
Direction of feed	TR (The direction is the 1pin of product is at the upper right when you hold reel on the left hand and you pull out the tape on the right hand)



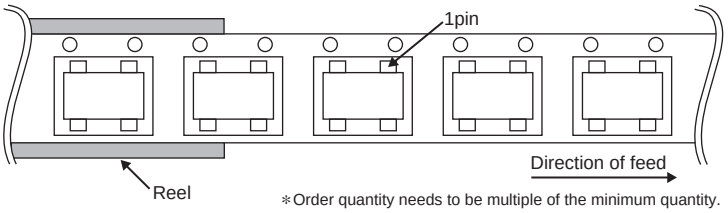
∗Order quantity needs to be multiple of the minimum quantity.

SOP4



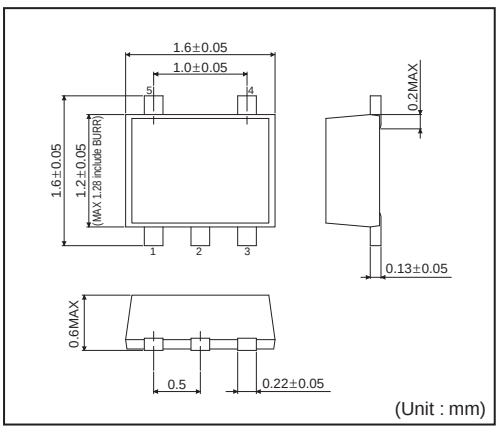
<Tape and Reel information>

Tape	Embossed carrier tape
Quantity	3000pcs
Direction of feed	TR (The direction is the 1pin of product is at the upper right when you hold reel on the left hand and you pull out the tape on the right hand)



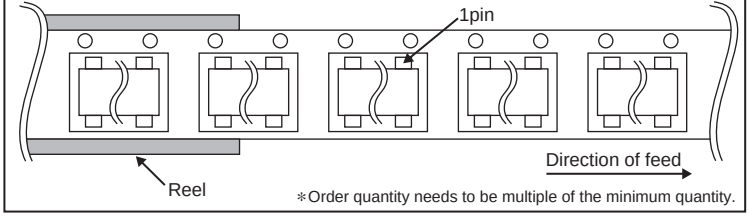
∗Order quantity needs to be multiple of the minimum quantity.

VSOF5



<Tape and Reel information>

Tape	Embossed carrier tape
Quantity	3000pcs
Direction of feed	TR (The direction is the 1pin of product is at the upper right when you hold reel on the left hand and you pull out the tape on the right hand)



∗Order quantity needs to be multiple of the minimum quantity.

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