PAS6337 CMOS VGA DIGITAL IMAGE SENSOR

General Description

The PAS6337 is a highly integrated CMOS active-pixel image sensor that has output of 640 x 480 pixels. It embedded the new FinePixel™ sensor technology to perform the excellent image quality. PAS6337 outputs YUV/YCrCb 4:2:2 or RGB565/555/444 data through the MIPI interface. It is available in CSP-22L package.

The PAS6337 can be programmed to set the exposure time for different luminance condition via I2C™ serial control bus. By programming the internal register set, it performs on-chip frame rate adjustment and programmable gain control.

Features

- **Resolution: 640 x 480 pixels, 1/9" Lens**
- **Bayer-RGB color filter array**
- **Output format :**
  - **YUV/YCrCb 4:2:2**
  - **RGB565/555/444**
- **Continuous variable frame time & exposure time**
- **I2C™ Interface**
- **Support 1.8V/2.8V I/O**
- **Power consumption : operating typical 25mA @ 2.8V (VGA YUV 30fps output, without loading), power-down typical 10uA @ 2.8V**
- **Automatic Background Compensation**
- **Black sun cancellation**
- **DSP function :**
  - **AEC & AGC**
  - **AWB**
  - **Gamma**
  - **Color matrix**
  - **Sharpness**
  - **De-noise**
  - **Color saturation**
  - **Defect compensation**
  - **Lens shading compensation**
  - **Decimation & WOI**
  - **Gesture detection**
- **PLL**
- **Module size : 5.0mm * 5.0mm**
- **MIPI interface (max. 500Mbps)**
- **Support WLL (Wafer Level Lens)**

Key Specification

Resolution		**640 (H) x 480 (V)**
Power	**Analog**	**2.8V typ.**
	I/O	**1.8V/2.8V**
	Core	**1.8V typ.**
Optical format		**1/9" Lens**
Pixel Size		**2.5um * 2.5um**
Lens Chief Ray Angle		**23 degree**
Sensitivity		**1900 mV/Lux-Sec**
Color filter		**RGB Bayer Pattern**
Exposure Time		**~ Frame time to Line time**
Scan Mode		**Progressive**
S/N Ratio		**39 dB**
Dynamic range		**69 dB**
Package		**CSP-22L**

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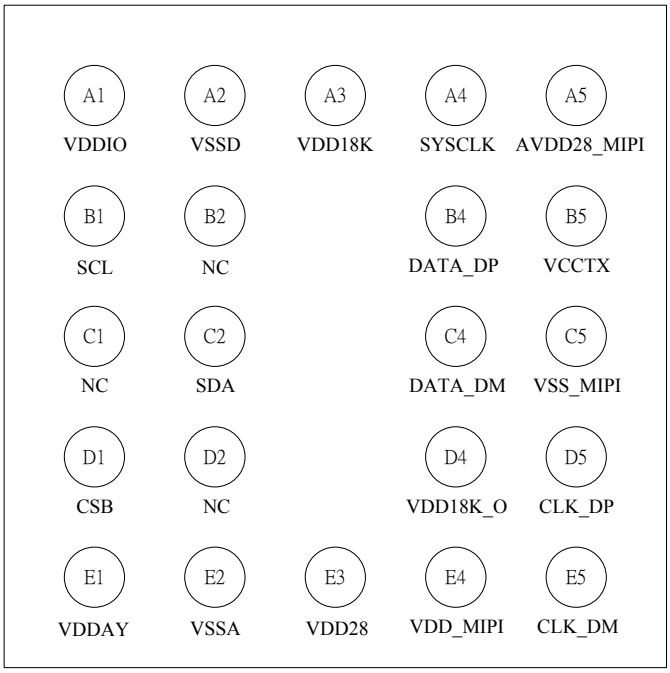
1. Pin Assignment



PAS6337

~TOP VIEW~

Pin No.	Name	Type	Description
A1	VDDIO	PWR	I/O power, 2.8V/1.8V
A2	VSSD	GND	Digital ground
A3	VDD18K	PWR	Digital core power, 1.8V
A4	SYSCLK	IN	External clock input
A5	AVDD28_MIPI	PWR	Main power, 2.8V
B1	SCL	IN	I2C clock input
B2	NC	- -	- -
B4	DATA_DP	OUT	MIPI data [+]
B5	VCCTX	Ref	Voltage reference
C1	NC	- -	- -
C2	SDA	I/O	I2C data
C4	DATA_DM	OUT	MIPI data [-]
C5	VSS_MIPI	GND	MIPI ground
D1	CSB	IN	Power down mode enable, active high
D2	NC	- -	- -
D4	VDD18_O	PWR	Digital core power, 1.8V
D5	CLK_DP	OUT	MIPI clock [+]
E1	VDDAY	Ref	Voltage reference
E2	VSSA	GND	Analog ground
E3	VDD28	PWR	Main power, 2.8V
E4	VDD_MIPI	PWR	Digital core power, 1.8V
E5	CLK_DM	OUT	MIPI clock [-]

2. Specifications

Absolute Maximum Ratings

Operating Temperature		-30 ~ 85℃
Stable Image Temperature		0 ~ 50℃
Ambient Storage Temperature		-40 ~ 125℃
Supply Voltage (with respect to ground)	V_{DDM}	3.6V
	V_{DDD}	3.0V
	V_{DDIO}	3.6V
All Input / Output Voltage (with respect to ground)		3.6V
Lead-free temperature, Surface-mount process		245℃
ESD rating, Human Body model		2000V

DC Electrical Characteristics (Ta = 0℃ ~ 70℃)

Symbol	Parameter	Min.	Typ.	Max.	Unit
Type : POWER					
V_{DDM}	DC supply voltage – Main	2.6	2.8	3.0	V
V_{DDD}	DC supply voltage – Digital core		1.8		V
V_{DDIO}	DC supply voltage – I/O	1.7	2.8	3.0	V
I_{DD}	Operating Current (VGA YUV 30fps / 2.8v)		25		mA
I_{PWDN}	Power Down Current (VGA YUV 30fps / 2.8v)		10		µA
Type : IN & I/O					
V_{IH}	Input Voltage HIGH	$0.7*V_{DDIO}$			V
V_{IL}	Input Voltage LOW			$0.3*V_{DDIO}$	V
Type : OUT & I/O					
V_{OH}	Output Voltage HIGH	$0.9*V_{DDIO}$			V
V_{OL}	Output Voltage LOW			$0.1*V_{DDIO}$	V

AC Operating Condition

Symbol	Parameter	Min.	Typ.	Max.	Unit
f_{sysclk}	System clock frequency		24		MHz
t_{sysclk_dc}	System clock duty cycle	45	50	55	%

Sensor Characteristics

Parameter	Typ.	Unit
Sensitivity	1900	mV/Lux-Sec
Signal to Noise Ratio	39	dB
Dynamic Range	69	dB

3. I2C™ Bus

PAS6337 supports I2C bus transfer protocol and acts as slave device. The 7-bits unique slave address is "1000000" and supports receiving / transmitting speed as maximum 400KHz.

I2C Bus Overview

- Only two wires SDA (serial data) and SCL (serial clock) carry information between the devices connected to the I2C bus. Normally both SDA and SCL lines are open collector structure and pulled high by external pull-up resistors.
- Only the master can initiates a transfer (start), generates clock signals, and terminates a transfer (stop).
- Start and stop condition : A high to low transition of the SDA line while SCL is high defines a start condition. A low to high transition of the SDA line while SCL is high defines a stop condition. Please refer to Figure 2.1.
- Valid data : The data on the SDA line must be stable during the high period of the SCL clock. Within each byte, MSB is always transferred first. Read / Write control bit is the LSB of the first byte. Please refer to Figure 2.2.
- Both the master and slave can transmit and receive data from the bus.
- Acknowledge : The receiving device should pull down the SDA line during high period of the SCL clock line when a complete byte was transferred by transmitter. In the case of a master received data from a slave, the master does not generate an acknowledgment on the last byte to indicate the end of a master read cycle.

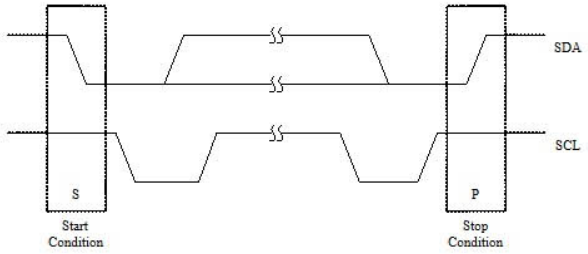


Figure 2.1 Start and Stop conditions

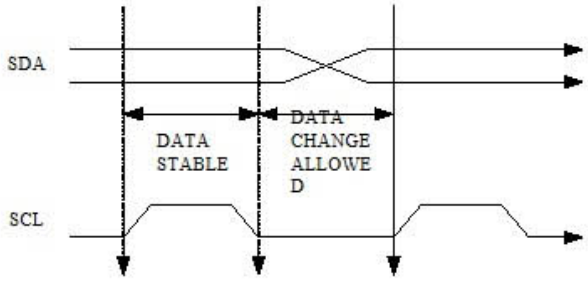
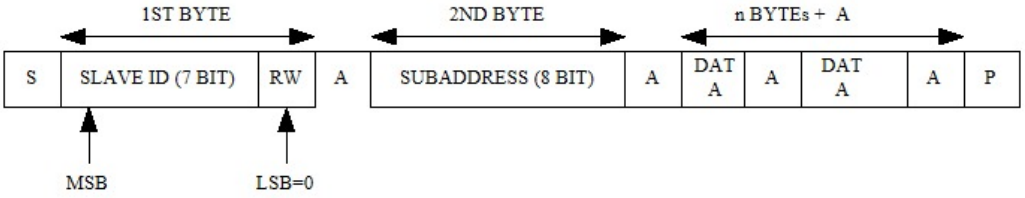


Figure 2.2 Valid Data

Data Transfer Format

Master transmits data to salve (write cycle)

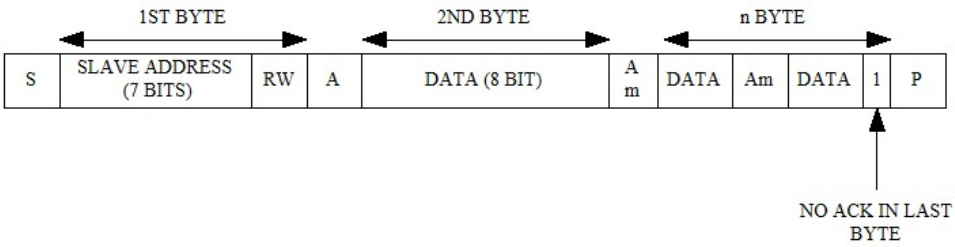
- S : Start.
- A : Acknowledge by salve.
- P : Stop.
- RW : The LSB of 1ST byte to decide whether current cycle is read or write cycle. RW = 1 – Read cycle, RW = 0 – Write cycle.
- SUBADDRESS : The address values of PAS6337 internal control registers. (Please refer to PAS6337 register description)



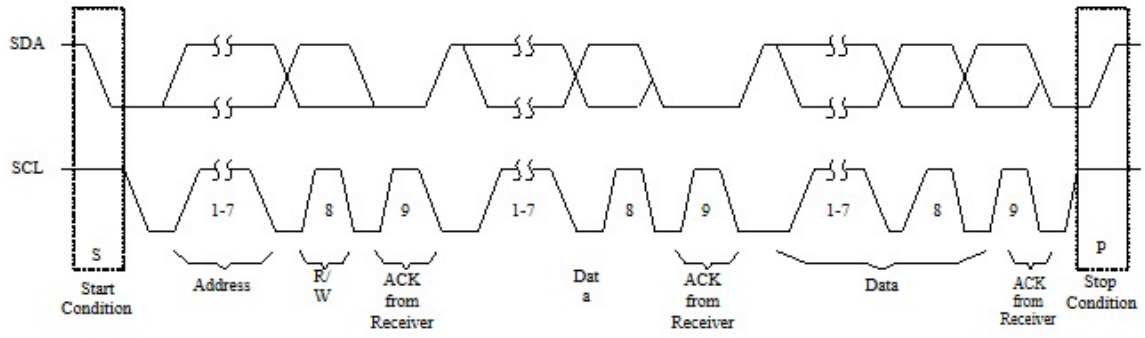
During write cycle, the master generates start condition and then places the 1st byte data that are combined slave address (7 bits) with a read / write control bit to SDA line. After slave (PAS6337) issues acknowledgment, the master places 2nd byte (Sub Address) data on SDA line. Again follow the PAS6337 acknowledgment, the master places the 8 bits data on SDA line and transmit to PAS6337 control register (address was assigned by 2nd byte). After PAS6337 issues acknowledgment, the master can generate a stop condition to end of this write cycle. In the condition of multi-byte write, the PAS6337 sub-address is automatically increment after each DATA byte transferred. The data and A cycles is repeat until last byte write. Every control registers value inside PAS6337 can be programming via this way.

Slave transmits data to master (read cycle)

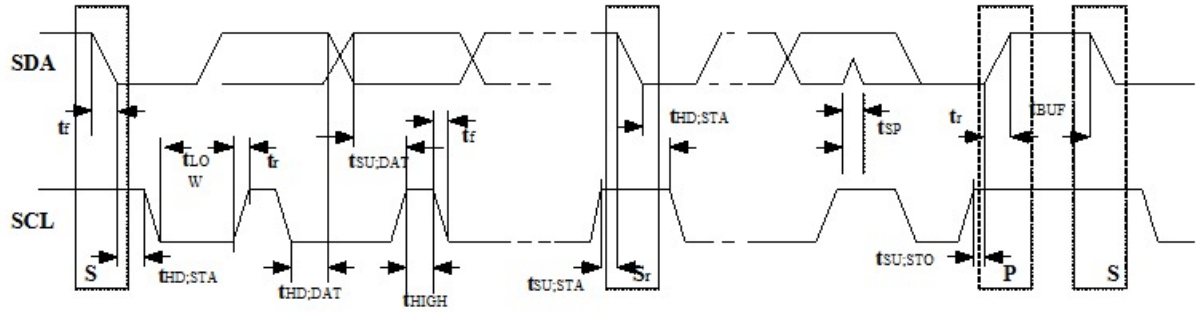
- The sub-address was taken from previous write cycle.
- The sub-address is automatically increment after each byte read.
- Am : Acknowledge by master.
- Note there is no acknowledgment from master after last byte read.



During read cycle, the master generates start condition and then place the 1st byte data that are combined slave address (7 bits) with a read / write control bit to SDA line. After issue acknowledgment, 8 bits DATA was also placed on SDA line by PAS6337. The 8 bits data was read from PAS6337 internal control register that address was assigned by previous write cycle. Follow the master acknowledgment, the PAS6337 place the next 8 bits data (address is increment automatically) on SDA line and then transmit to master serially. The DATA and Am cycles is repeat until the last byte read. After last byte read, Am is no longer generated by master but instead by keep SDA line high. The slave (PAS6337) must releases SDA line to master to generate STOP condition.



I2C™ Bus Timing



I2C™ Bus Timing Specification

Parameter	Symbol	Standard Mode		Unit
		Min.	Max	
SCL clock frequency.	f_{scl}	10	400	KHz
Hold time (repeated) Start condition. After this period, the first clock pulse is generated.	$t_{HD:STA}$	4.0	-	µs
Low period of the SCL clock.	t_{LOW}	4.7	-	µs
High period of the SCL clock.	t_{HIGH}	0.75	-	µs
Set-up time for a repeated START condition.	$t_{SU;STA}$	4.7	-	µs
Data hold time. For I2C-bus device.	$t_{HD;DAT}$	0	3.45	µs
Data set-up time.	$t_{SU;DAT}$	250	-	ns
Rise time of both SDA and SCL signals.	t_r	30	N.D.	ns (notel)
Fall time of both SDA and SCL signals.	t_f	30	N.D.	ns (notel)
Set-up time for STOP condition.	$t_{SU;STO}$	4.0	-	µs
Bus free time between a STOP and START.	t_{BUF}	4.7	-	µs
Capacitive load for each bus line.	C_b	1	15	pF
Noise margin at LOW level for each connected device. (Including hysteresis)	V_{nL}	0.1 VDD	-	V
Noise margin at HIGH level for each connected device. (including hysteresis)	V_{nH}	0.2 VDD	-	V

Note : It depends on the “high” period time of SCL.

4. Registers

Register Table

Bank	Address		Bits	Register Name	Default Value	Notes
	Hex	Dec				
0	0	0	[7:0]	PartID[15:8]	0x63	Part ID
0	1	1	[7:0]	PartID[7:0]	0x35	Part ID
0	2	2	[3:0]	VersionID[3:0]	0x00	VersionID
0	3	3	[3:0]	SubID[3:0]	0x0a	SubID
0	4	4	[0]	R_AE_stage_indoor_Sel	0x0	AE indoor stage select 0:11 , 1:12
0	F	15	[7:0]	R_AWB_Window_X[7:0]	0x90	AWB window width (by4)
0	11	17	[7:0]	R_AWB_Window_Y[7:0]	0x64	AWB window height (by4)
0	13	19	[7:0]	R_lpf_min[7:0]	0xf6	Lpf minimum value for AE
0	14	20	[7:4]	R_ny_min[3:0]	0x21	Ny minimum value for AE
0	14	20	[2:0]	R_lpf_min[10:8]	0x21	Lpf minimum value for AE
0	19	25	[7:0]	R_AWB_DGnR_LB_by2[7:0]	0x40	AWB digital gain lower bound for R
0	1A	26	[7:0]	R_AWB_DGnR_UB_by2[7:0]	0x68	AWB digital gain upper bound for B
0	1B	27	[7:0]	R_AWB_DGnB_LB_by2[7:0]	0x46	AWB digital gain lower bound for B
0	1C	28	[7:0]	R_AWB_DGnB_UB_by2[7:0]	0x6e	AWB digital gain upper bound for R
0	1F	31	[4]	R_DeNoiseEn	0x93	DeNoise Enable
0	20	32	[7:0]	R_DeNoise_Str__G[7:0]	0x03	Denoise Strength (for color G)
0	21	33	[7:0]	R_DeNoise_H_LB_G[7:0]	0x04	Denoise H LB (for color G)
0	22	34	[7:0]	R_DeNoise_H_UB_G[7:0]	0x16	Denoise H UB (for color G)
0	23	35	[7:0]	R_DeNoise_Str__RB[7:0]	0x04	Denoise Strength (for color R/B)
0	24	36	[7:0]	R_DeNoise_H_LB_RB[7:0]	0x04	Denoise H LB (for color R/B)
0	25	37	[7:0]	R_DeNoise_H_UB_RB[7:0]	0x24	Denoise H UB (for color R/B)
0	29	41	[0]	R_ISP_Gamma_EnH	0x01	ISP gamma correction enable
0	2B	43	[7:0]	R_ISP_Y01	0x19	ISP Gamma Y1
0	2C	44	[7:0]	R_ISP_Y02	0x2f	ISP Gamma Y2
0	2D	45	[7:0]	R_ISP_Y03	0x53	ISP Gamma Y3
0	2E	46	[7:0]	R_ISP_Y04	0x62	ISP Gamma Y4
0	2F	47	[7:0]	R_ISP_Y05	0x6f	ISP Gamma Y5
0	30	48	[7:0]	R_ISP_Y06	0x7c	ISP Gamma Y6
0	31	49	[7:0]	R_ISP_Y07	0x87	ISP Gamma Y7
0	32	50	[7:0]	R_ISP_Y08	0x9a	ISP Gamma Y8
0	33	51	[7:0]	R_ISP_Y09	0xaa	ISP Gamma Y9
0	34	52	[7:0]	R_ISP_Y10	0xb8	ISP Gamma Y10
0	35	53	[7:0]	R_ISP_Y11	0xc5	ISP Gamma Y11
0	36	54	[7:0]	R_ISP_Y12	0xd8	ISP Gamma Y12
0	37	55	[7:0]	R_ISP_Y13	0xe8	ISP Gamma Y13
0	38	56	[7:0]	R_ISP_Y14	0xf5	ISP Gamma Y14
0	47	71	[1:0]	R_AWB_Speed[1:0]	0x34	AWB adjust speed. The more, the slower 0: 1 x 1: 1/2 x 2: 1/4 x 3: 1/8 x
0	49	73	[7:0]	R_AWB_SumRatio_B	0x80	AWB B sum ratio = 128/X
0	4A	74	[7:0]	R_AWB_SumRatio_R	0x80	AWB R sum ratio = 128/X
0	4D	77	[7:0]	R_AWB_CbThdL[7:0]	0x64	AWB region test Cb Low threshold -128 ~ +127 (2's complement)
0	4E	78	[7:0]	R_AWB_CrThdL[7:0]	0x87	AWB region test Cr Low threshold -128 ~ +127 (2's complement)

0	4F	79	[7:0]	R_AWB_CbCrThdL[7:0]	0x00	AWB region test Cb+Cr Low threshold -128 ~ +127 (2's complement)
0	50	80	[7:0]	R_AWB_CbThdH[7:0]	0x75	AWB region test Cb High threshold -128 ~ +127 (2's complement)
0	51	81	[7:0]	R_AWB_CrThdH[7:0]	0x96	AWB region test Cr High threshold -128 ~ +127 (2's complement)
0	52	82	[7:0]	R_AWB_CbCrThdH[7:0]	0xff	AWB region test Cb+Cr High threshold -128 ~ +127 (2's complement)
0	53	83	[7:0]	R_Ylow	0x1e	Low bound of "light-pixel"Y in AWB
0	54	84	[7:0]	R_Yhigh	0xff	High bound of "light-pixel"Y in AWB
0	57	87	[3:0]	R_AWB_LockRange__In[3:0]	0x02	AWB Lockrange In (NL)
0	58	88	[5:0]	R_AWB_LockRange_Out[5:0]	0x04	AWB Lockrange Out (NL)
0	59	89	[5:0]	R_AWB_LockRange__In_LL[5:0]	0x04	AWB Lockrange In (LL)
0	5A	90	[5:0]	R_AWB_LockRange_Out_LL[5:0]	0x06	AWB Lockrange Out (LL)
0	5B	91	[2:0]	R_AWB_MinStep_th[2:0]	0x00	AWB mininum step size 0:1, 1:2, 2:4, 3:8, 4:16, 5:32, 6:64, 7:128
0	5F	95	[7:0]	R_AE_LockRange_Out_LB[7:0]	0x14	AE Lockrange Out LB
0	64	100	[7:0]	R_AE_LockRange_Out_UB[7:0]	0x14	AE Lockrange Out UB
0	65	101	[7:4]	R_AE_LockRange__In[3:0]	0x41	AE Lockrange In
0	66	102	[4]	R_AE_EnH	0x00	AE enable
0	66	102	[0]	R_freq_60	0x01	Set de-flicker frequency 0/1: 50/60Hz
0	67	103	[7:0]	R_SysClk_freq[7:0]	0x97	Input_frequency/2048
0	68	104	[6:0]	R_SysClk_freq[14:8]	0x31	Input_frequency/2048
0	6B	107	[4:0]	R_AE_minStage[4:0]	0x07	Minimum AE stage
0	6C	108	[4:0]	R_AE_maxStage[4:0]	0x1c	Maximum AE stage (AE_maxStage<=31), Update flag
0	6D	109	[7:0]	R_AG_stage_UB	0x3f	AG_stage upper bound at max AE_stage, Update flag
0	6F	111	[7:0]	R_Ytar8bit	0x82	0~255, Target luminance of AE
0	71	113	[0]	Set_Force_WrSensorAEWB_Params_Once	0x00	1=wr once
0	72	114	[0]	R_AWB_EnH	0x00	Auto-white balance enable
0	72	114	[4]	R_AWB_Gain_rst	0x01	AWB gain gain reset
0	81	129	[5:4]	R_AE_Speed	0x00	AE speed, the more, the slower 0: 1 x 1: 1/2 x 2: 1/4 x 3: 1/8 x
0	81	129	[2:0]	R_AE_MinStep_th[2:0]	0x00	AE Minimun step threshold select 0:8, 1:10, 2:12, 3:16, 4:24, 5:32, 6: 48, 7:64
0	8F	143	[7:0]	R_ImgEffect_c0	0x00	Image Effect parameter 0 (ISP_UpdateFlag=1, update)
0	90	144	[7:0]	R_ImgEffect_c1	0x00	Image Effect parameter 1 (ISP_UpdateFlag=1, update)
0	91	145	[7:0]	R_ImgEffect_c2	0x00	Image Effect parameter 2 (ISP_UpdateFlag=1, update)
0	93	147	[3:0]	R_ImgEffectMode	0x00	Image Effect mode 0: monochrome 1: negative 2: x-ray 3: Sepia/Cold/Warm/Sunset 6: Solarize 10: Pixelate (ISP_UpdateFlag=1, update)
0	94	148	[0]	R_ISP_ImgEffect_En	0x00	(ISP_UpdateFlag=1, update)
0	97	151	[4]	R_Shading_EnH	0x01	Lens shading enable
0	98	152	[1:0]	R_ASKIP_V[1:0]	0x00	Analog skip of vertical direction
0	98	152	[3:2]	R_ASKIP_H[1:0]	0x00	Analog skip of horizontal direction
0	98	152	[4]	R_VFLIP	0x00	Vertical flip

0	98	152	[5]	R_HFLIP	0x00	Horizontal flip
0	99	153	[6:0]	R_OffsetX_R[6:0]	0x00	Horizontal distances between shading center and sensor array center of R-channel, MSB:sign bit, -63~+63
0	9A	154	[6:0]	R_OffsetY_R[6:0]	0x00	Vertical distances between shading center and sensor array center of R-channel, MSB:sign bit, -63~+63
0	9B	155	[6:0]	R_OffsetX_G[6:0]	0x00	Horizontal distances between shading center and sensor array center of G-channel, MSB:sign bit, -63~+63
0	9C	156	[6:0]	R_OffsetY_G[6:0]	0x00	Vertical distances between shading center and sensor array center of G-channel, MSB:sign bit, -63~+63
0	9D	157	[6:0]	R_OffsetX_B[6:0]	0x00	Horizontal distances between shading center and sensor array center of B-channel, MSB:sign bit, -63~+63
0	9E	158	[6:0]	R_OffsetY_B[6:0]	0x00	Vertical distances between shading center and sensor array center of B-channel, MSB:sign bit, -63~+63
0	9F	159	[6:0]	R_LSC_R1[6:0]	0x00	Quartic parameter of R-channel
0	A0	160	[6:0]	R_LSC_G1[6:0]	0x00	Quartic parameter of G-channel
0	A1	161	[6:0]	R_LSC_B1[6:0]	0x00	Quartic parameter of B-channel
0	A2	162	[6:0]	R_LSC_R2[6:0]	0x50	Square parameter of R-channel
0	A3	163	[6:0]	R_LSC_G2[6:0]	0x50	Square parameter of G-channel
0	A4	164	[6:0]	R_LSC_B2[6:0]	0x50	Square parameter of B-channel
0	A5	165	[2:0]	R_LSFT_1[2:0]	0x04	Parameter of LensShading
0	A6	166	[1:0]	R_LSFT_2[1:0]	0x00	Parameter of LensShading
0	A7	167	[1:0]	R_LSFT_3[1:0]	0x21	Parameter of LensShading
0	A7	167	[5:4]	R_LSFT_4[1:0]	0x21	Parameter of LensShading
0	EF	239	[2:0]	R_RegBankSel	0x00	Register Bank Select 0: ISP1 Register Bank (default) 1: Sensor Register Bank 2: ISP2 Register Bank 3: MIPI regbank
2	7	7	[7:0]	R_ImgEffect_Y_offset[7:0]	0x80	2'complement (ISP2_UpdateFlag=1, update)
2	8	8	[7:0]	R_ImgEffect_U_offset[7:0]	0x00	2'complement (ISP2_UpdateFlag=1, update)
2	9	9	[7:0]	R_ImgEffect_V_offset[7:0]	0x00	2'complement (ISP2_UpdateFlag=1, update)
2	A	10	[0]	R_ISP_ImgEffect_1_En	0x00	(ISP2_UpdateFlag=1, update)
2	C	12	[7:0]	R_AUTO_Contrast_UB	0x50	Contrast strength UB
2	D	13	[7:0]	R_AUTO_Contrast_LB	0x40	Contrast strength LB
2	22	34	[3]	R_Defect_EnH	0x01	Defect Enable
2	22	34	[7]	R_ISP_Edge_En0	0x01	ISP edge enhancement enable
2	2C	44	[5:0]	R_Edge_UB[5:0]	0x20	ISP edge enhancement value upper bound
2	2D	45	[5:0]	R_Edge_LB[5:0]	0x19	ISP edge enhancement value lower bound
2	2E	46	[5:0]	R_EdgeThdLB[5:0]	0x10	ISP edgethd LB
2	2F	47	[4:0]	R_AE_stage_LL[4:0]	0x13	AE_stage > R_AE_stage_LL =>Low Light
2	30	48	[4:0]	R_AE_stage_NL[4:0]	0x11	AE_stage < R_AE_stage_NL =>Normal Light
2	35	53	[4:0]	R_Gamma_Strength_NL[4:0]	0x10	Gamma Strength @ NL
2	36	54	[4:0]	R_Gamma_Strength_Delta[4:0]	0x08	Increment when AE/AG stage change
2	36	54	[5]	R_Manual_Gamma_Strength	0x00	Fix setting to NL
2	37	55	[4:0]	R_Gamma_Strength_LL[4:0]	0x08	Gamma Strength @ LL
2	38	56	[4:0]	R_AE_Middle_Stage[4:0]	0x0f	Apply Middle Gain when AE_stage >= R_AE_Middle_Stage
2	38	56	[7]	R_AE_Middle_Gain_En	0x01	AE Middle Gain Enable
2	39	57	[6:0]	R_AE_Middle_Gain[6:0]	0x10	max 63 (non-frame-rate mode)
2	3E	62	[5:0]	R_CCMbSign[5:0]	0x33	CCM matrix coefficient
2	3F	63	[6:0]	R_CCMb0_0[6:0]	0x13	CCM matrix coefficient(Q1.6)
2	40	64	[6:0]	R_CCMb0_1[6:0]	0x25	CCM matrix coefficient(Q1.6)
2	41	65	[6:0]	R_CCMb0_2[6:0]	0x07	CCM matrix coefficient(Q1.6)
2	42	66	[6:0]	R_CCMb1_0[6:0]	0x0c	CCM matrix coefficient(Q0.7)

2	43	67	[6:0]	R_CCMb1_1[6:0]	0x29	CCM matrix coefficient(Q0.7)
2	44	68	[6:0]	R_CCMb1_2[6:0]	0x35	CCM matrix coefficient(Q0.7)
2	45	69	[6:0]	R_CCMb2_0[6:0]	0x35	CCM matrix coefficient(Q0.7)
2	46	70	[6:0]	R_CCMb2_1[6:0]	0x34	CCM matrix coefficient(Q0.7)
2	47	71	[6:0]	R_CCMb2_2[6:0]	0x01	CCM matrix coefficient(Q0.7)
2	48	72	[4:0]	R_AE_Middle_Stage2[4:0]	0x30	AE_Middle_Gain2 select region
2	49	73	[4:0]	R_AE_Middle_Stage3[4:0]	0x52	AE_Middle_Gain3 select region
2	55	85	[4]	R_Manual_EdgeRatio	0x00	Fix setting to normal light
2	56	86	[4:0]	R_EdgeRatio_Delta[4:0]	0x08	Increment when AE/AG state change
2	57	87	[4:0]	R_EdgeRatio_LL[4:0]	0x04	Edge ratio @Low Light
2	58	88	[4:0]	R_EdgeRatio_NL[4:0]	0x0a	Edge ratio @Normal Light
2	59	89	[4]	R_Manual_Edge_th	0x00	Fix setting to normal light
2	5A	90	[4:0]	R_Edge_th_Delta[4:0]	0x08	Increment when AE/AG state change
2	5B	91	[4:0]	R_Edge_th_LL[4:0]	0x0a	Edge threshold @ Low Light
2	5C	92	[4:0]	R_Edge_th_NL[4:0]	0x08	Edge threshold @ Normal Light
2	5D	93	[0]	R_Saturation_Fast	0x01	1: fast change, +-Delta 0: slow change, +-(1/Delta)
2	5D	93	[1]	R_Saturation_2X	0x00	Color Saturation double
2	5D	93	[4]	R_Manual_Saturation	0x00	Fix setting to normal light
2	5E	94	[4:0]	R_Saturation_Delta[4:0]	0x01	Increment when AE/AG state change
2	5F	95	[4:0]	R_Saturation_LL[4:0]	0x0b	Color Saturation @ Low Light
2	60	96	[4:0]	R_Saturation_NL[4:0]	0x16	Color Saturation @ Normal Light
2	61	97	[0]	R_Shading_CP_Fast	0x00	1: fast change, +-Delta 0: slow change, +-(1/Delta)
2	61	97	[4]	R_Manual_Shading_CP	0x00	Manual Shading percentage
2	62	98	[4:0]	R_Shading_CP_Delta[4:0]	0x02	Increment when AE/AG state change
2	63	99	[3:0]	R_Shading_CP_NL[3:0]	0x0f	Shading compensation percentage @Normal Light
2	63	99	[7:4]	R_Shading_CP_LL[3:0]	0x00	Shading compensation percentage @Low Light
2	64	100	[0]	R_Contrast_En	0x01	Contrast Enable
2	69	105	[7:0]	R_Brightness_LL[7:0]	0x00	Brightness @ Low Light
2	6A	106	[7:0]	R_Brightness_NL[7:0]	0x00	Brightness @ Normal Light
2	7E	126	[6:0]	R_AE_Middle_Gain2[6:0]	0x00	max 63 (non-frame-rate mode)
2	7F	127	[6:0]	R_AE_Middle_Gain3[6:0]	0x8a	max 63 (non-frame-rate mode)
2	BE	190	[0]	R_RGB_Dithering	0x00	RGB565/555/444 Dithering
2	BF	191	[1]	R_UV_Swap	0x00	U V Swap
2	BF	191	[2]	R_HLByte_Swap	0x01	Pxdata High/Low byte swap YUV mode : YC swap RGB565/555/444 mode : High/low byte swap Processd Raw mode : must set to "0"
2	C0	192	[3:0]	R_RGB565_mode[3:0]	0x00	RGB565_mode
2	C0	192	[5:4]	R_Format_Sel	0x00	Output Data format select 0:YUV 1:RGB565 2:RGB555 3:RGB444 (ISP2_UpdateFlag=1, update)
2	C1	193	[0]	R_Vsync_INV	0x01	Vsync inverse
2	C1	193	[1]	R_Hsync_INV	0x01	Hsync inverse
2	C1	193	[2]	R_Pxclk_INV	0x00	Pxclk inverse
2	C1	193	[3]	R_Pxclk_Gated_InHVSync	0x00	Testmode: Gate PXCLK in hsync/vsync
2	C1	193	[4]	R_SenVsync_En	0x00	OV Sensor Timing
2	C1	193	[5]	R_HsyncInVsync	0x00	hsync toggle when vsync high
2	C2	194	[6:4]	R_PxclkO_dly	0x00	Pxclk Delay Cell Select
2	C2	194	[2:0]	R_HsyncO_dly	0x00	Hsync Delay Cell Select

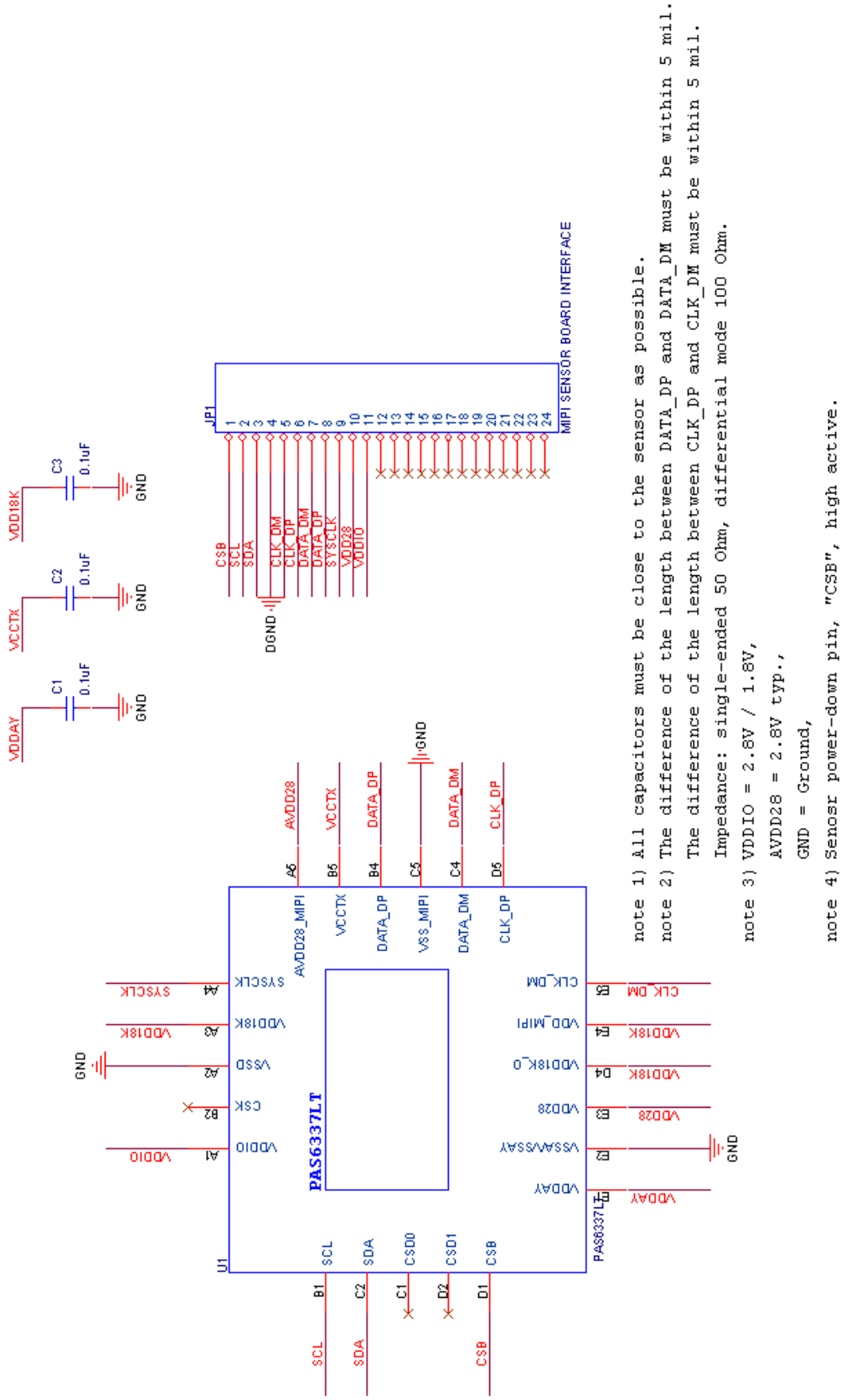
2	CF	207	[7:0]	R_Y_MIN[7:0]	0x00	Y output Min
2	D0	208	[7:0]	R_Y_MAX[7:0]	0xff	Y output Max
2	D1	209	[7:0]	R_C_MIN[7:0]	0x00	C output Min
2	D2	210	[7:0]	R_C_MAX[7:0]	0xff	C output Max
3	0	0	[7:0]	PartID[7:0]	0x52	PJS152
3	1	1	[7:0]	PartID[15:8]	0x01	PJS152
3	2	2	[3:0]	VersionID[3:0]	0x0	Version 0
3	3	3	[0]	R_Dummy_Byte_Append	0	CSI2 dummy byre append
3	4	4	[7:0]	R_Line_Per_Frame[7:0]	0xe0	CSI2 V_size (defule: 480)
3	5	5	[7:0]	R_Line_Per_Frame[15:8]	0x01	CSI2 V_size (defule: 480)
3	6	6	[2:0]	R_Data_Format[2:0]	0x00	CSI2 data format (defaule: YUV422)
3	7	7	[7:0]	R_Pixels_Per_Line[7:0]	0x80	CSI2 H_size (defule: 640)
3	8	8	[7:0]	R_Pixels_Per_Line[15:8]	0x02	CSI2 H_size (defule: 640)
3	9	9	[7:0]	R_TxDataReq_TxDataValid_Period[7:0]	0x00	CSI2 TxDataReq to TxDataValid period
3	A	10	[7:0]	R_TxData_Valid_End_Period[7:0]	0x01	CSI2 TxData Valid End period
3	B	11	[7:0]	R_TxData_Split_Req_Period[7:0]	0x01	CSI2 TxData Split Request period
3	C	12	[7:0]	R_TxDataReq_PhyClk_LPS_Period[7:0]	0x03	CSI2 TxDataReq to PhyClk LPS period
3	D	13	[7:0]	R_TX_Sram_Start_Read_Offset[7:0]	0xa1	CSI TX sram start read threshold
3	E	14	[0]	R_TX_Sram_Start_Read_Offset[8]	0x00	CSI TX sram start read threshold
3	F	15	[0]	R_CSI2_Enable	0x00	CSI enable
3	10	16	[2:0]	R_CsiTx_LaneN[2:0]	0x01	CSI data lane number
3	11	17	[0]	R_PhyClk_NonStop	0	Vsync phy clock enable
3	12	18	[4]	R_Clk_ULPM_En	0	Clock ultra low power mode enable
3	12	18	[0]	R_ULPM_En	0	Ultra low power mode enable
3	13	19	[0]	R_BuiltIn_SenMod	0x00	MIPI built-in sensor mode
3	14	20	[7:0]	R_sync_byte[7:0]	0xb8	MIPI PHY sync byte
3	15	21	[7:0]	R_LPX_prd[7:0]	0x03	MIPI LPX period
3	16	22	[7:0]	R_LpPrep_prd[7:0]	0x02	MIPI LP prepare period
3	17	23	[7:0]	R_HsPrep_prd[7:0]	0x02	MIPI HS prepare period
3	18	24	[7:0]	R_HsEoT_prd[7:0]	0x00	MIPI HS end of transmission period
3	19	25	[7:0]	R_LpEoT_prd[7:0]	0x00	MIPI LP end of transmission period
3	1A	26	[7:0]	R_ckln_LpPrep_prd[7:0]	0x01	MIPI clock LP prepare period
3	1B	27	[7:0]	R_ckln_HsPrep_prd[7:0]	0x02	MIPI clock HS prepare period
3	1C	28	[7:0]	R_ckln_HsEoT_prd[7:0]	0x01	MIPI clock HS end of transmission period
3	1D	29	[7:0]	R_ckln_LpEoT_prd[7:0]	0x02	MIPI clock LP end of transmission period
3	1E	30	[7:0]	R_ckln_zero_prd[7:0]	0x08	MIPI clock zero period
3	1F	31	[7:0]	R_Dummy_0[7:0]	0x00	Dummy register 0
3	20	32	[7:0]	R_Dummy_1[7:0]	0x00	Dummy register 1
3	21	33	[7:0]	R_ULPM_Wakeup	0x1e	MIPI ULPM wackup time
3	22	34	[7:0]	R_Clk_ULPM_Wakeup	0x1e	MIPI clock ULPM wakeup time
3	23	35	[0]	R_Nov_Sync_En	0x01	MIPI TS_nov sync enable
3	24	36	[7:0]	R_Clk_Pre_Preiod[7:0]	0x04	MIPI clock pre preiod
3	2A	42	[7:0]	R_LPF[7:0]	0x08	Sensor model LPF
3	2B	43	[4:0]	R_LPF[12:8]	0x02	Sensor model LPF
3	2C	44	[7:0]	R_LTime[7:0]	0xa4	Sensor model LTime
3	2D	45	[5:0]	R_LTime[13:8]	0x06	Sensor model Ltime
3	2E	46	[7:0]	R_HSize[7:0]	0x00	Sensor model Hsize
3	2F	47	[5:0]	R_HSize[13:8]	0x05	Sensor model Hsize
3	30	48	[7:0]	R_VSize[7:0]	0xe0	Sensor model Vsize

3	31	49	[4:0]	R_VSize[12:8]	0x01	Sensor model Vsize
3	32	50	[0]	R_CSI_DEBUG_MODE	0	CSI debug mode enable
3	33	51	[0]	R_Skip_CSI_Header	0	CSI skip header enable
3	34	52	[7:0]	R_test_byte_1[7:0]	0x00	CSI test byte 1
3	35	53	[7:0]	R_test_byte_2[7:0]	0x00	CSI test byte 2
3	36	54	[7:0]	R_test_byte_3[7:0]	0x00	CSI test byte 3
3	37	55	[7:0]	R_test_byte_4[7:0]	0x00	CSI test byte 4
3	38	56	[7:0]	R_RowCntInit_div32[7:0]	0x0e	Sensor model row initial
3	39	57	[7:0]	R_Cmd_Np[7:0]	0x01	MIPI clock np
3	3A	58	[7:0]	R_Phyclk_Split_Req_Period[7:0]	0x01	MIPI phy clock spilt period
3	3B	59	[0]	R_Cmd_Gated_MIPI_Clk	1	MIPI clock gated on
3	3C	60	[0]	R_MIPI_IO_Off	0	MIPI IO tri-state
3	3D	61	[0]	R_Fast_HsEoT_En	1	MIPI HsEoT fast enable
3	3E	62	[0]	R_MIPI_FastUpdate	0	MIPI fast update pll related register
3	3F	63	[0]	T_pll_filter_en	0	pll charge pump filter enable
3	40	64	[5:0]	T_pll_m[5:0]	0x18	Reference clock divider, it is 6 bit , so maximum division is 64
3	41	65	[5:0]	T_pll_n[5:0]	0x32	VCO clock divider, it is 6 bit , so maximum division is 64
3	42	66	[0]	T_pll_enh	1	"0": power down PLL; "1": PLL normal operation
3	43	67	[0]	T_clkd16_EnH	0	"0": power down CLKD16, and CLKD16="0"; "1": VCO clock divided by 16 for testing PLL
3	44	68	[0]	T_pllvco_div3_en	0	"0": vco@416M mode, first divider N=2; "1": vco@624M mode, first divider N=3
3	45	69	[3:0]	T_pll_c1[3:0]	0x08	pll C1 selection. Unit Cap=1pF.
3	46	70	[3:0]	T_pll_c2[3:0]	0x07	pll C1 selection. Unit Cap=10pF.
3	47	71	[2:0]	T_pll_r2[2:0]	0x01	pll R2 selection. 0: 60k; 1: 70k; 2: 80k;3: 90k; 4: 100k; 5: 120k; 6: 150k; 7: 240k;
3	48	72	[2:0]	T_pll_icp[2:0]	0x03	pll charge pump current selection. 1~8uA,unit current=1uA.
3	49	73	[1:0]	T_pll_kvco[1:0]	0x02	pll vco kvco selection.
3	4A	74	[0]	T_mipi_iop_boost	0	mipi ref.gen op boost.
3	4B	75	[4:0]	T_mipi_iref_trim[4:0]	0x10	mipi iref gen triming.
3	4C	76	[0]	T_mipi_bitclk_phase	0	mipi clk lane phase selection.
3	4D	77	[1:0]	T_mipi_clkphase_hs[1:0]	0x00	mipi clk lane phase selection.
3	4E	78	[0]	T_mipi_hs_en	0	mipi high speed enable. "1": mipi speed = vco max. frequency, "0": mipi speed = 208MHz
3	4F	79	[0]	T_mipi_test_EnH	0	mipi test mode enable.
3	50	80	[0]	T_mipi_refgen_enh	1	mipi ref.gen enable.
3	51	81	[0]	T_mipi_test_loop	0	mipi test mode: test loop enable.
3	52	82	[0]	T_mipi_test_txd	0	mipi test mode: txd input enable.
3	53	83	[2:0]	T_mipi_vtx_trim[2:0]	0x04	mipi vtx triming.
3	54	84	[3:0]	T_mipi_zdn_hs[3:0]	0x05	mipi hs mode output_n impedance.
3	55	85	[1:0]	T_mipi_zdn_lp[1:0]	0x01	mipi LP mode output_n impedance.
3	56	86	[3:0]	T_mipi_zup_hs[3:0]	0x05	mipi hs mode output_p impedance.
3	57	87	[1:0]	T_mipi_zup_lp[1:0]	0x01	mipi LP mode output_p impedance.
3	58	88	[3:0]	T_mipi_dmy[3:0]	0x08	mipi dummy register
3	59	89	[0]	T_pll_cp_boost	0	pll charge pump current boost 2.5x
3	5A	90	[3:0]	R_GPIO_sel[3:0]	0	GPIO select mode
3	61	97	[0]	R_Chksum_En	0	Checksum enable
3	62	98	[7:0]	R_golden_SENIF_I[7:0]	0x00	Sensor interface golden checksum
3	63	99	[7:0]	R_golden_SENIF_I[15:8]	0x40	Sensor interface golden checksum
3	64	100	[7:0]	R_golden_CSI_O[7:0]	0xe0	CSI output golden checksum
3	65	101	[7:0]	R_golden_CSI_O[15:8]	0xd2	CSI output golden checksum

3	66	102	[7:0]	R_golden_CSI_O[23:16]	0xd7	CSI output golden checksum
3	67	103	[7:0]	R_golden_CSI_O[31:24]	0xcf	CSI output golden checksum
3	68	104	[7:0]	R_golden_TX0[7:0]	0x40	D-PHY output golden checksum
3	69	105	[7:0]	R_golden_TX0[15:8]	0xa3	D-PHY output golden checksum
3	70	112	[0]	R_BIST_MIPI_Start	0	MIPI MBIST start
3	71	113	[3:0]	R_BIST_MIPI_mode[3:0]	0x0	MIPI MBIST mode
3	72	114	[3:0]	R_BIST_MIPI_Sel[3:0]	0x0	MIPI MBIST select
3	73	115	[2]	BIST_MIPI_error	0	MIPI MBIST error
3	73	115	[1]	BIST_MIPI_ok	0	MIPI MBIST ok
3	73	115	[0]	BIST_MIPI_end	0	MIPI MBIST end
3	74	116	[7:0]	BIST_MIPI_error_A[7:0]	0x00	MIPI MBIST error address
3	75	117	[7:0]	BIST_MIPI_error_map[7:0]	0x00	MIPI MBIST error bit map
3	76	118	[7:0]	BIST_MIPI_error_map[15:8]	0x00	MIPI MBIST error bit map
3	77	119	[7:0]	BIST_MIPI_error_map[23:16]	0x00	MIPI MBIST error bit map
3	78	120	[7:0]	BIST_MIPI_error_map[31:24]	0x00	MIPI MBIST error bit map
3	79	121	[7:0]	BIST_MIPI_error_map[39:32]	0x00	MIPI MBIST error bit map
3	7A	122	[7:0]	BIST_MIPI_error_map[47:40]	0x00	MIPI MBIST error bit map
3	7B	123	[7:0]	BIST_MIPI_error_map[55:48]	0x00	MIPI MBIST error bit map
3	7C	124	[7:0]	BIST_MIPI_error_map[63:56]	0x00	MIPI MBIST error bit map
3	82	130	[1]	TX_Sram_Empty_Error_Flag	0x00	CSI sram empty error flag
3	82	130	[0]	TX_Sram_Full_Error_Flag	0x00	CSI sram full error flag
3	83	131	[2]	Mismch_TX0	0x00	D-PHY output mismatch flag
3	83	131	[1]	Mismch_CSI_O	0x00	CSI output mismatch flag
3	83	131	[0]	Mismch_SENIF_I	0x00	Sensor interface mismatch flag
3	87	135	[7:0]	Cksum_SENIF_I[7:0]	0x00	sensor interface input checksum
3	88	136	[7:0]	Cksum_SENIF_I[15:8]	0x00	sensor interface input checksum
3	89	137	[7:0]	Cksum_CSI_O[7:0]	0x00	CSI output checksum
3	8A	138	[7:0]	Cksum_CSI_O[15:8]	0x00	CSI output checksum
3	8B	139	[7:0]	Cksum_CSI_O[23:16]	0x00	CSI output checksum
3	8C	140	[7:0]	Cksum_CSI_O[31:24]	0x00	CSI output checksum
3	8E	142	[7:0]	Cksum_TX0[7:0]	0x00	D-PHY output checksum
3	8F	143	[7:0]	Cksum_TX0[15:8]	0x00	D-PHY output checksum
3	90	144	[3:0]	R_MIPI_SRAM_DS[3:0]	0x04	SRAM DS
3	ED	237	[0]	MIPI_update	0	Sync update pll related register
3	F1	241	[0]	MIPI_SWRstn	0	MIPI software reset
3	F2	242	[0]	RegBank_SWRstn	0	MIPI regbank software reset

5. Reference Circuit Schematic

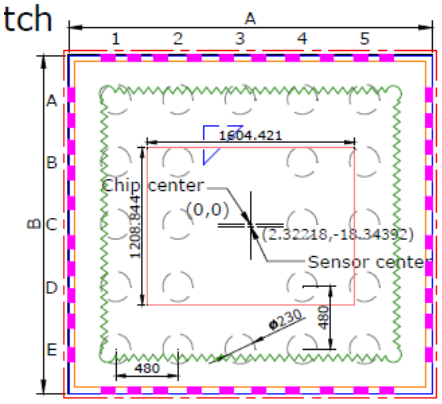
VDDIO = 1.8V / 2.8V



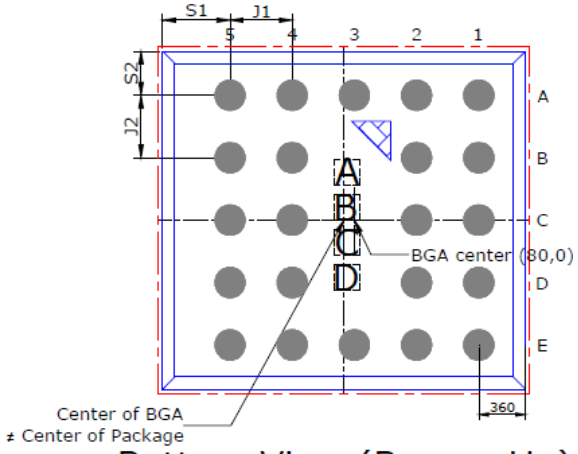
6. Package Information

	Symbol	Nominal	Min.	Max.
		μm		
Package Body Dimension X	**A**	2800	2775	2825
Package Body Dimension Y	**B**	2598.4	2573.4	2623.4
Package Height	**C**	750	690	810
Ball Height	**C1**	120	90	150
Package Body Thickness	**C2**	630	585	675
Thickness of Glass surface to wafer	**C3**	445	425	465
Ball Diameter	**D**	230	200	260
Total Pin Count	**N**	22		
Pin Count X axis	**N1**	5		
Pin Count Y axis	**N2**	5		
Pins Pitch X axis	**J1**	480		
Pins Pitch Y axis	**J2**	480		
Edge to Pin Center Distance along X	**S1**	520	490	550
Edge to Pin Center Distance along Y	**S2**	339.2	309.2	369.2

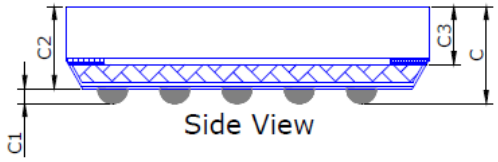
tch



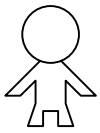
Top View (Bumps Down)



Bottom View (Bumps Up)



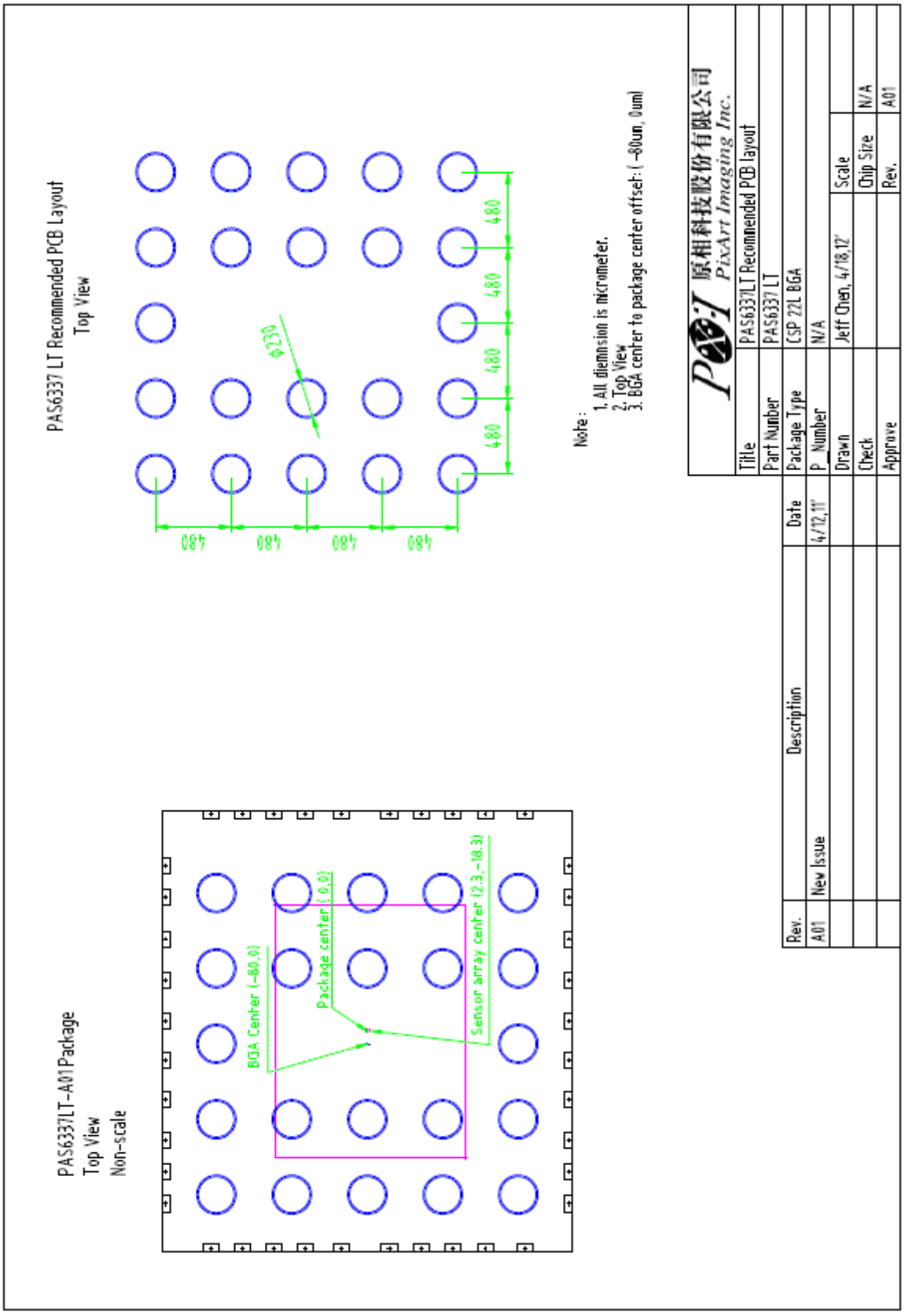
Side View



*Note

The formation of image is the result formed by package Top view(A1 : left-up) and general Lens(invert and mirror the image).

Recommended PCB Layout



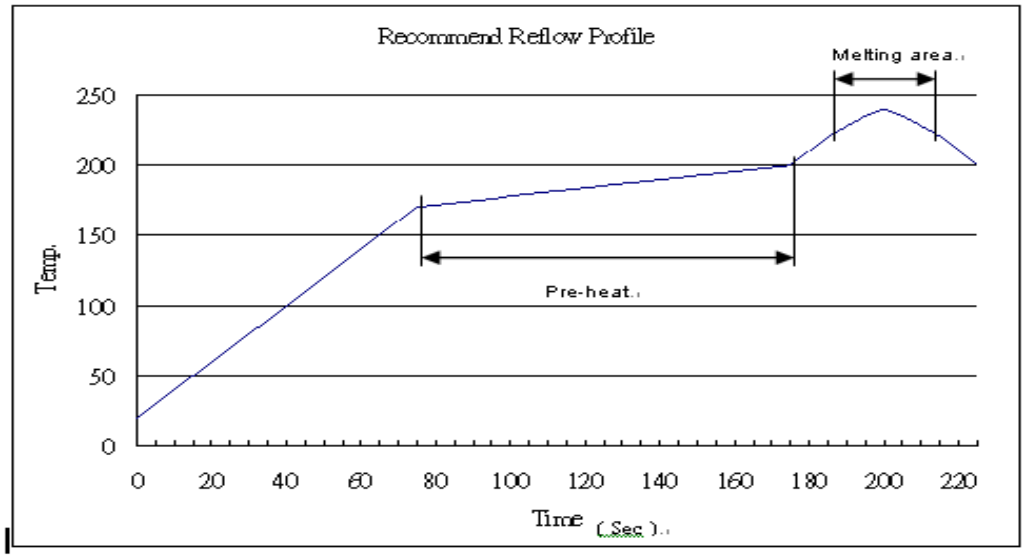
Recommended Guideline for PCB Assembly

1.1 Recommended vender and type for Pb-free solder paste

1. Almit LFM-48W TM-HP
2. Senju M705-GRN360-K

1.2 IR Reflow Soldering Profile:

Temperature profile is the most important control in reflow soldering. It must be fine tuned to establish a robust process. The typical recommended IR reflow profile is showed in figure 8 below.



IR Reflow Profile

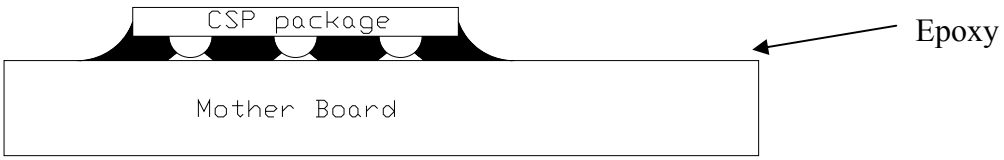
Reflow Profile :

1. Average Ramp-up Rate (30°C to preheat zone): 1.5~ 2.5 Degree C/ Sec
2. Preheat zone:
   - 2.1 Temp ramp from 170~ 200 degree C
   - 2.2 Exposure time: 90 +/- 30 sec
3. Melting zone:
   - 3.1 Melting area temp > 220 degree C for at least 30 ~ 50 sec
   - 3.2 Peak temperature : 245 degree C.

1.3 Others:

1.3.1 Epoxy under-filled process is required post IC mounting process.

⊙ Dispense Epoxy



Epoxy Under-filled